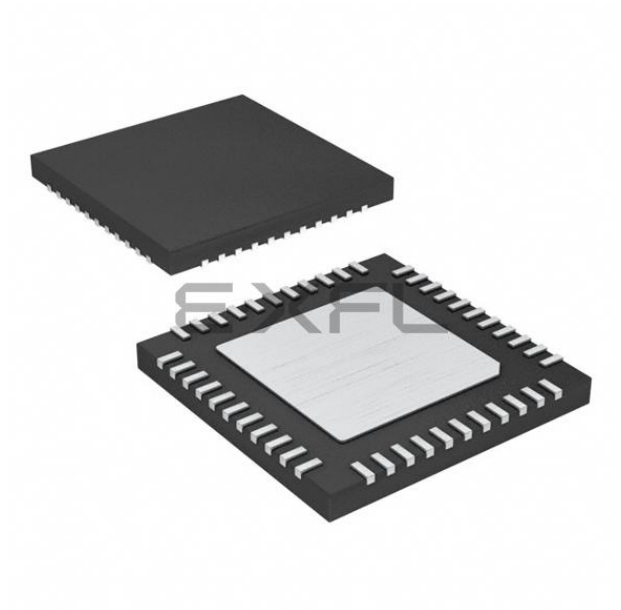
Analog Devices Inc./Maxim Integrated - MAXQ612X-2552+ Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	MAXQ20S
Core Size	16-Bit
Speed	12MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, Infrared, Power-Fail, POR, WDT
Number of I/O	56
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-WFQFN Exposed Pad
Supplier Device Package	44-TQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/maxq612x-2552

ABSOLUTE MAXIMUM RATINGS

Voltage Range on V_{DD} with Respect to GND .....-0.3V to +3.6V
Voltage Range on Any Lead with
Respect to GND Except V_{BUS}..... -0.3V to (V_{DD} + 0.5V)
Voltage Range on V_{BUS} with Respect to GND....-0.3V to +6.0V
Continuous Output Current
Any Single I/O Pin.....25mA
All I/O Pins Combined.....25mA
Voltage Range on DP, DM with
Respect to GND.....-0.3V to (V_{BUS} + 0.3V)
Operating Temperature Range..... 0°C to +70°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(V_{DD} = V_{RST} to 3.6V, T_A = 0°C to +70°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}			V_{RST}		3.6	V
1.8V Internal Regulator	V_{REG18}			1.62	1.8	1.98	V
Power-Fail Warning Voltage for Supply	V_{PFW}	Monitors V_{DD} (Notes 2, 3, 4)		1.75	1.8	1.85	V
Power-Fail Reset Voltage	V_{RST}	Monitors V_{DD} (Note 5)		1.64	1.67	1.70	V
POR Voltage	V_{POR}	Monitors V_{DD}		1.0		1.42	V
RAM Data-Retention Voltage	V_{DRV}	(Note 6)		1.0			V
Active Current	I_{DD_1}	Sysclk = 12MHz			4.8	5.5	mA
	I_{DD_2}	Sysclk = 1MHz (Note 6)			0.52	0.8	
Stop-Mode Current	I_{S1}	Power-Fail Off (Note 7)	T_A = +25°C		0.3	3	µA
			T_A = +70°C		2.8	13	
	I_{S2}	Power-Fail On	T_A = +25°C		24	30	
			T_A = +70°C		30	40	
Current Consumption During Power Fail	I_{PFR}	(Notes 6, 8, 9)		[(3 x I_{S2}) + ((PCI - 3) x (I_{S1} + I_{NANO}))]/ PCI			µA
Current Consumption During POR	I_{POR}	(Note 10)			100		nA
Stop-Mode Resume Time	t_{ON}				375 + 8192 t_{HFXIN}		µs
Power-Fail Monitor Startup Time	t_{PFM_ON}	(Note 6)				150	µs
Power-Fail Warning Detection Time	t_{PFW}	(Notes 6, 11)		10			µs
Input Low Voltage for IRTX, IRRX, $\overline{RESET}$, and All Port Pins	V_{IL}			V_{GND}		0.3 x V_{DD}	V
Input High Voltage for IRTX, IRRX, $\overline{RESET}$, and All Port Pins	V_{IH}			0.7 x V_{DD}		V_{DD}	V

RECOMMENDED OPERATING CONDITIONS (continued)

(V_{DD} = V_{RST} to 3.6V, T_A = 0°C to +70°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Hysteresis (Schmitt)	V_{IHYS}			300		mV
Input Low Voltage for HFXIN	V_{IL_HFXIN}	External driven clock and not feedback connected crystal oscillator	V_{GND}		0.3 x V_{DD}	V
Input High Voltage for HFXIN	V_{IH_HFXIN}	External driven clock and not feedback connected crystal oscillator	0.7 x V_{DD}		V_{DD}	V
IRRX Input Filter Pulse-Width Reject	t_{IRRX_R}				50	ns
IRRX Input Filter Pulse-Width Accept	t_{IRRX_A}		300			ns
Output Low Voltage for IRTX	V_{OL_IRTX}	V_{DD} = 3.6V, I_{OL} = 25mA (Note 6)			1.0	V
		V_{DD} = 2.35V, I_{OL} = 10mA (Note 6)			1.0	
		V_{DD} = 1.85V, I_{OL} = 4.5mA			1.0	
Output Low Voltage for $\overline{RESET}$ and All Port Pins (Note 12)	V_{OL}	V_{DD} = 3.6V, I_{OL} = 11mA (Note 6)		0.4	0.5	V
		V_{DD} = 2.35V, I_{OL} = 8mA (Note 6)		0.4	0.5	
		V_{DD} = 1.85V, I_{OL} = 4.5mA		0.4	0.5	
Output High Voltage for IRTX and All Port Pins	V_{OH}	I_{OH} = -2mA	V_{DDIO} - 0.5		V_{DDIO}	V
Input/Output Pin Capacitance for All Port Pins Except DP, DM	C_{IO}	(Note 6)			15	pF
Input Leakage Current	I_L	Internal pullup disabled	-100		+100	nA
Input Pullup Resistor for $\overline{RESET}$, IRTX, IRRX, P0 to P6	R_{PU}	V_{DD} = 3V, V_{OL} = V_{DD}/2 (Note 6)	16	25	39	kΩ
		V_{DD} = 2V, V_{OL} = V_{DD}/2	17	27	41	
		V_{DD} = 3.0V, V_{OL} = 0.4V (Note 6)	16	28	39	
		V_{DD} = 2.0V, V_{OL} = 0.4V (Note 6)	17	30	41	
GPIO Supply Output High Voltage	V_{DDIOH}	V_{DDIOH} current is the sum of V_{DDIO} current and I_{OH} of all GPIO, I_{OH} = 10mA	V_{DD} - 0.4		V_{DD}	V
EXTERNAL CRYSTAL/RESONATOR						
Crystal/Resonator	f_{HFXIN}	(Note 13)	1		12	MHz
Crystal/Resonator Period	t_{HFXIN}			1/f_{HFXIN}		ns
Crystal/Resonator Warmup Time	t_{XTAL_RDY}	From initial oscillation		8192 x t_{HFXIN}		ms
Oscillator Feedback Resistor	R_{OSCF}	(Note 6)	0.5	1.0	1.5	MΩ
Crystal ESR		(Note 6)			60	Ω
EXTERNAL CLOCK INPUT						
External Clock Frequency	f_{XCLK}	(Note 13)	DC		12	MHz
External Clock Period	t_{XCLK}			1/f_{XCLK}		ns
External Clock Duty Cycle	t_{XCLK_DUTY}		45		55	%
System Clock Frequency	f_{CK}			f_{HFXIN}		MHz
		HFXOUT = GND		f_{XCLK}		

RECOMMENDED OPERATING CONDITIONS (continued)

(V_{DD} = V_{RST} to 3.6V, T_A = 0°C to +70°C.) (Note 1)

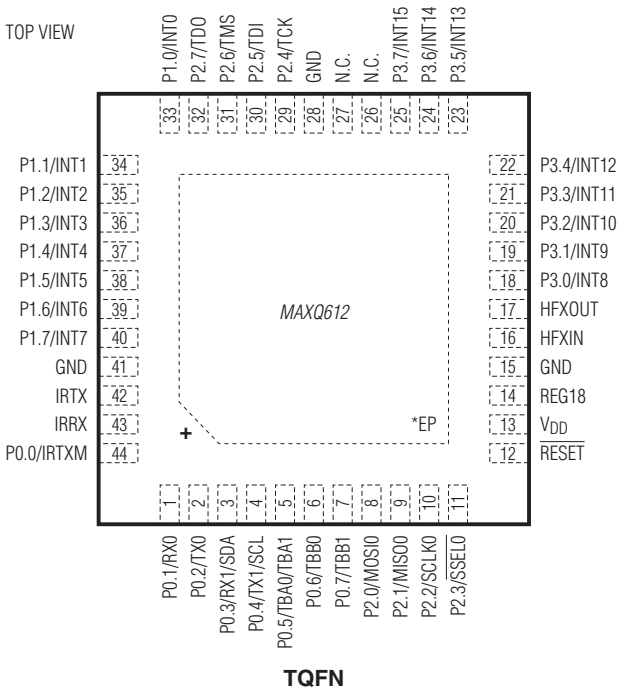
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
System Clock Period	t_{CK}			$1/f_{CK}$		ns
NANOPOWER RING						
Nanopower Ring Frequency	f_{NANO}	T_A = +25°C	3	13	20	kHz
		T_A = +25°C, V_{DD} = POR voltage (Note 6)	1.7	2.4		
Nanopower Ring Duty Cycle	t_{NANO}	(Note 6)	40		60	%
Nanopower Ring Current	I_{NANO}	Typical at V_{DD} = 1.64V, T_A = +25°C (Note 6)		40	400	nA
WAKE-UP TIMER						
Wake-Up Timer Interval	t_{WAKEUP}		$1/f_{NANO}$		$65,535/f_{NANO}$	s
FLASH MEMORY						
System Clock During Flash Programming/Erase	$f_{FPSYSCLK}$		1			MHz
Flash Erase Time	t_{ME}	Mass erase	20		40	ms
	t_{ERASE}	Page erase	20		40	
Flash Programming Time per Word	t_{PROG}	(Note 14)	20		100	µs
Write/Erase Cycles			20,000			Cycles
Data Retention		T_A = +25°C	100			Years
USB						
USB Supply Voltage	V_{BUS}	(Note 15)	4.5	5.0	5.5	V
V_{BUS} Supply Current (Note 16)	I_{VBUS}	Transmitting on DP and DM at 12Mbps, C_L = 50pF on DP and DM to GND, FRCVDD = 0			13.5	mA
		Transmitting on DP and DM at 12Mbps, C_L = 50pF on DP and DM to GND, FRCVDD = 1			3.5	mA
V_{BUS} Supply Current During Idle (Note 16)	I_{VBUSID}	DP = high, DM = low, FRCVDD = 0 (Note 6)			6	mA
		DP = high, DM = low, FRCVDD = 1			0.2	mA
V_{BUS} Suspend Supply Current	$I_{VBUSSUS}$				500	µA
Single-Ended Input High Voltage DP, DM	V_{IHD}		2.0			V
Single-Ended Input Low Voltage DP, DM	V_{ILD}				0.8	V
Output Low Voltage DP, DM	V_{OLD}	R_L = 1.5kΩ from DP to 3.6V			0.3	V
Output High Voltage DP, DM	V_{OHD}	R_L = 15kΩ from DP and DM to GND	2.8			V
Differential Input Sensitivity DP, DM	V_{DI}	DP to DM	0.2			V
Common-Mode Voltage Range	V_{CM}	Includes V_{DI} range	0.8		2.5	V

RECOMMENDED OPERATING CONDITIONS (continued)

(V_{DD} = V_{RST} to 3.6V, T_A = 0°C to +70°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Single-Ended Receiver Threshold	V_{SE}		0.8		2.0	V
Single-Ended Receiver Hysteresis	V_{SEH}			200		mV
Differential Output Signal Cross-Point Voltage	V_{CRS}	C_L = 50pF (Note 6)	1.3		2.0	V
DP, DM Off-State Input Impedance	R_{LZ}		300			kΩ
Driver Output Impedance	R_{DRV}	Steady-state drive	28		44	Ω
DP Pullup Resistor	R_{PU}	Idle	0.9		1.575	kΩ
		Receiving	1.425		3.090	
USB TIMING						
DP, DM Rise Time (Transmit)	t_R	C_L = 50pF	4		20	ns
DP, DM Fall Time (Transmit)	t_F	C_L = 50pF	4		20	ns
Rise/Fall Time Matching (Transmit)	t_R/t_F	C_L = 50pF (Note 6)	90		110	%
IR						
Carrier Frequency	f_{IR}				$f_{CK}/2$	Hz
SPI (Note 6)						
SPI Master Operating Frequency	$1/t_{MCK}$				$f_{CK}/2$	MHz
SPI Slave Operating Frequency	$1/t_{SCK}$				$f_{CK}/4$	MHz
SPI I/O Rise/Fall Time	t_{SPI_RF}	C_L = 15pF, pullup = 560Ω	8		24	ns
SCLK_ Output Pulse-Width High/Low	t_{MCH}, t_{MCL}		$t_{MCK}/2$ - t_{SPI_RF}			ns
MOSI_ Output Hold Time After SCLK_ Sample Edge	t_{MOH}		$t_{MCK}/2$ - t_{SPI_RF}			ns
MOSI_ Output Valid to Sample Edge	t_{MOV}		$t_{MCK}/2$ - t_{SPI_RF}			ns
MISO_ Input Valid to SCLK_ Sample Edge Rise/Fall Setup	t_{MIS}		25			ns
MISO_ Input to SCLK_ Sample Edge Rise/Fall Hold	t_{MIH}		0			ns
SCLK_ Inactive to MOSI_ Inactive	t_{MLH}		$t_{MCK}/2$ - t_{SPI_RF}			ns
SCLK_ Input Pulse-Width High/Low	t_{SCH}, t_{SCL}			$t_{SCK}/2$		ns
$\overline{SSEL}$_ Active to First Shift Edge	t_{SSE}		t_{SPI_RF}			ns

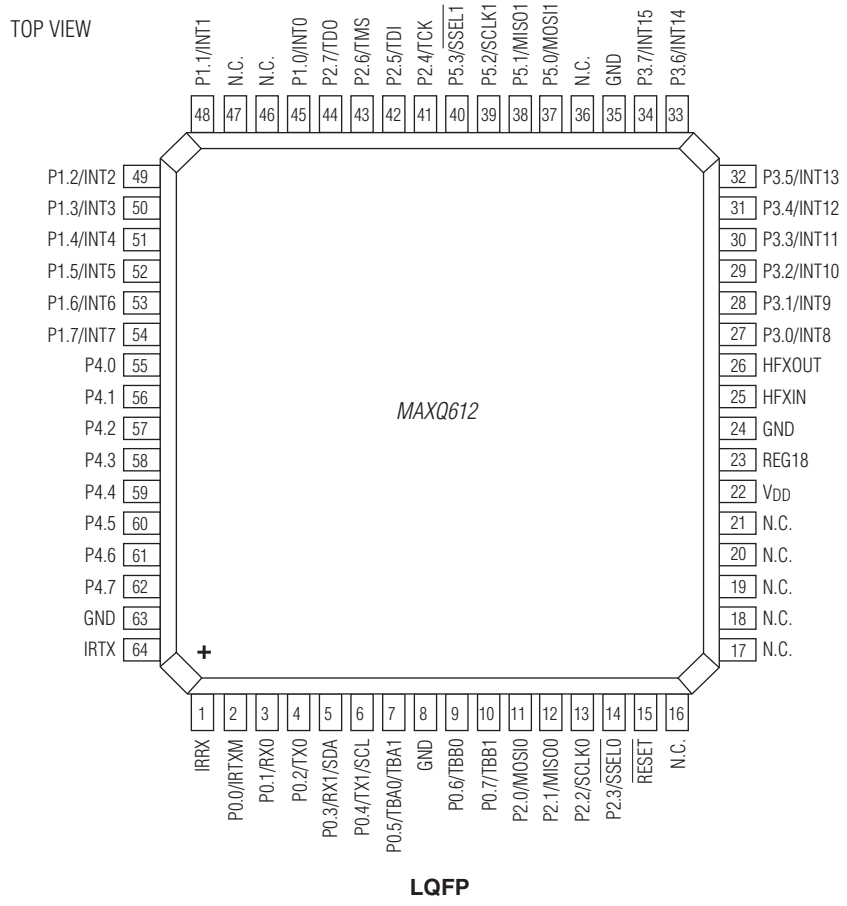
Pin Configurations



TQFN

*EXPOSED PAD.

Pin Configurations (continued)



LQFP

Pin Descriptions—TQFN, LQFP (continued)

PIN			NAME	FUNCTION
MAXQ612 TQFN-EP	MAXQ612 LQFP	MAXQ622 LQFP		
RESET PINS				
12	15	15	$\overline{\text{RESET}}$	Digital, Active-Low, Reset Input/Output. The CPU is held in reset when this pin is low and begins executing from the reset vector when released. The pin includes pullup current source and should be driven by an open-drain, external source capable of sinking in excess of 4mA. This pin is driven low as an output when an internal reset condition occurs.
CLOCK PINS				
16	25	25	HFXIN	High-Frequency Crystal Input. Connect an external crystal or resonator between HFXIN and HFXOUT as the high-frequency system clock. Alternatively, HFXIN is the input for an external, high-frequency clock source when HFXOUT is shorted to ground during POR.
17	26	26	HFXOUT	
USB FUNCTION PINS				
—	—	19	V_{BUS}	USB V_{BUS} Supply Voltage. Connect V_{BUS} to a positive 5.0V power supply. Bypass V_{BUS} to ground with a 1.0µF ceramic capacitor as close to the V_{BUS} pin as possible.
—	—	16	DP	USB D+ Signal. This bidirectional pin carries the positive differential data or single-ended data. Connect this pin to a USB “B” connector. This pin is weakly pulled high internally when the USB is disabled.
—	—	18	DM	USB D- Signal. This bidirectional pin carries the negative differential data or single-ended data. Connect this pin to a USB “B” connector. This pin is weakly pulled high internally when the USB is disabled.
—	—	20	V_{DDB}	USB Transceiver Supply Voltage. This is the power output of the internal voltage regulator that is used for the USB transceiver (3.3V) block. This pin is bypassed to ground with a 1.0µF capacitor as close as possible to the package. No external circuitry should be powered from this pin.
—	—	21	V_{DDIO}	Switched 3V Power Supply. This is the power output after selection between V_{BUS} and V_{DD}. Must be connected to an external ceramic chip capacitor. The capacitor must be placed as close to this pin as possible. No external devices other than the capacitor should be connected to this pin.
IR FUNCTION PINS				
42	64	64	IRTX	IR Transmit Output. Active-low IR transmit pin capable of sinking 25mA. This pin defaults to three-state input with the weak pullup disabled during all forms of reset. Software must configure this pin after release from reset to remove the three-state input condition.
43	1	1	IRRX	IR Receive Input

Pin Descriptions—TQFN, LQFP (continued)

<table>
<tr><th colspan="3">PIN</th><th rowspan="2">NAME</th><th rowspan="2">FUNCTION</th></tr>
<tr><th>MAXQ612 TQFN-EP</th><th>MAXQ612 LQFP</th><th>MAXQ622 LQFP</th></tr>
<tr><td colspan="6">GENERAL-PURPOSE I/O AND SPECIAL FUNCTION PINS</td></tr>
<tr><td rowspan="9">44, 1–7</td><td rowspan="9">2–7, 9, 10</td><td rowspan="9">2–7, 9, 10</td><td rowspan="9">P0.0–P0.7; IRTXM, RX0, TX0, RX1, TX1, SDA, SCL, TBA0, TBA1, TBB0, TBB1</td><td>General-Purpose, Digital, I/O, Type C Port. These port pins function as bidirectional I/O pins. All port pins default to three-state mode after a reset. All alternate functions must be enabled from software.
MAXQ612 TQFN-EP | MAXQ612 LQFP | MAXQ622 LQFP | PORT | SPECIAL FUNCTION
44 | 2 | 2 | P0.0 | IRTXM
1 | 3 | 3 | P0.1 | RX0
2 | 4 | 4 | P0.2 | TX0
3 | 5 | 5 | P0.3 | RX1/SDA
4 | 6 | 6 | P0.4 | TX1/SCL
5 | 7 | 7 | P0.5 | TBA0/TBA1
6 | 9 | 9 | P0.6 | TBB0
7 | 10 | 10 | P0.7 | TBB1</td></tr>
<tr><td rowspan="9">33–40</td><td rowspan="9">45, 48–54</td><td rowspan="9">45, 48–54</td><td rowspan="9">P1.0–P1.7; INT0–INT7</td><td>General-Purpose, Digital, I/O, Type D Port; External Edge-Selectable Interrupt. These port pins function as bidirectional I/O pins or as interrupts. All port pins default to three-state mode after a reset. All interrupt functions must be enabled from software.
MAXQ612 TQFN-EP | MAXQ612 LQFP | MAXQ622 LQFP | PORT | SPECIAL FUNCTION
33 | 45 | 45 | P1.0 | INT0
34 | 48 | 48 | P1.1 | INT1
35 | 49 | 49 | P1.2 | INT2
36 | 50 | 50 | P1.3 | INT3
37 | 51 | 51 | P1.4 | INT4
38 | 52 | 52 | P1.5 | INT5
39 | 53 | 53 | P1.6 | INT6
40 | 54 | 54 | P1.7 | INT7</td></tr>
</table>

Pin Descriptions—TQFN, LQFP (continued)

<table>
<tr><th colspan="3">PIN</th><th rowspan="2">NAME</th><th rowspan="2">FUNCTION</th></tr>
<tr><th>MAXQ612 TQFN-EP</th><th>MAXQ612 LQFP</th><th>MAXQ622 LQFP</th></tr>
<tr><td rowspan="10">—</td><td rowspan="10">55-62</td><td rowspan="10">55–62</td><td rowspan="10">P4.0–P4.7</td><td>General-Purpose, Digital, I/O, Type C Port. These port pins function as bidirectional I/O pins. All port pins default to three-state mode after a reset.</td></tr>
<tr><td><table>
<tr><th>MAXQ612 TQFN-EP</th><th>MAXQ612 LQFP</th><th>MAXQ622 LQFP</th><th>PORT</th><th>SPECIAL FUNCTION</th></tr>
<tr><td>—</td><td>55</td><td>55</td><td>P4.0</td><td>—</td></tr>
<tr><td>—</td><td>56</td><td>56</td><td>P4.1</td><td>—</td></tr>
<tr><td>—</td><td>57</td><td>57</td><td>P4.2</td><td>—</td></tr>
<tr><td>—</td><td>58</td><td>58</td><td>P4.3</td><td>—</td></tr>
<tr><td>—</td><td>59</td><td>59</td><td>P4.4</td><td>—</td></tr>
<tr><td>—</td><td>60</td><td>60</td><td>P4.5</td><td>—</td></tr>
<tr><td>—</td><td>61</td><td>61</td><td>P4.6</td><td>—</td></tr>
<tr><td>—</td><td>62</td><td>62</td><td>P4.7</td><td>—</td></tr>
</table></td></tr>
<tr><td rowspan="6">—</td><td rowspan="6">37–40</td><td rowspan="6">37–40</td><td rowspan="6">P5.0–P5.3; MOSI1, MISO1, SCLK1, $\overline{\text{SSEL1}}$</td><td>General-Purpose, Digital, I/O, Type C Port. These port pins function as bidirectional I/O pins. All port pins default to three-state mode after a reset. All alternate functions must be enabled from software. Enabling the pin's special function disables the general-purpose I/O on the pin.</td></tr>
<tr><td><table>
<tr><th>MAXQ612 TQFN-EP</th><th>MAXQ612 LQFP</th><th>MAXQ622 LQFP</th><th>PORT</th><th>SPECIAL FUNCTION</th></tr>
<tr><td>—</td><td>37</td><td>37</td><td>P5.0</td><td>MOSI1</td></tr>
<tr><td>—</td><td>38</td><td>38</td><td>P5.1</td><td>MISO1</td></tr>
<tr><td>—</td><td>39</td><td>39</td><td>P5.2</td><td>SCLK1</td></tr>
<tr><td>—</td><td>40</td><td>40</td><td>P5.3</td><td>$\overline{\text{SSEL1}}$</td></tr>
</table></td></tr>
<tr><td colspan="5">NO CONNECTION PINS</td></tr>
<tr><td>26, 27</td><td>16–21, 36, 46, 47</td><td>36, 46, 47</td><td>N.C.</td><td>No Connection. Reserved for future use. Leave these pins unconnected.</td></tr>
<tr><td colspan="5">EXPOSED PAD</td></tr>
<tr><td>—</td><td>—</td><td>—</td><td>EP</td><td>Exposed Pad (TQFN Only). Connect EP to the ground plane.</td></tr>
</table>

Pin Descriptions—Bare Die (continued)

<table>
<tr><th colspan="2">PIN</th><th rowspan="2">NAME</th><th rowspan="2">FUNCTION</th></tr>
<tr><th>MAXQ612</th><th>MAXQ622</th></tr>
<tr><td rowspan="11">16, 18, 19, 20, 50, 51, 53, 54</td><td rowspan="11">16, 18, 19, 20, 50, 51, 53, 54</td><td rowspan="11">P2.0–P2.7; MOSI0, MISO0, SCLK0, $\overline{SSEL0}$, TCK, TDI, TMS, TDO</td><td>General-Purpose, Digital, I/O, Type C Port. These port pins function as bidirectional I/O pins. P2.0 to P2.3 default to three-state mode after a reset. All alternate functions must be enabled from software. Enabling the pin's special function disables the general-purpose I/O on the pin.
The JTAG pins (P2.4 to P2.7) default to their JTAG function with weak pullups enabled after a reset. The JTAG function can be disabled using the TAP bit in the SC register.
P2.7 functions as the JTAG test-data output on reset and defaults to an input with a weak pullup. The output function of the test data is only enabled during the TAP's shift_IR or shift_DR states.</td></tr>
<tr><td>
<table>
<tr><th>MAXQ612</th><th>MAXQ622</th><th>PORT</th><th>SPECIAL FUNCTION</th></tr>
<tr><td>16</td><td>16</td><td>P2.0</td><td>MOSI0</td></tr>
<tr><td>18</td><td>18</td><td>P2.1</td><td>MISO0</td></tr>
<tr><td>19</td><td>19</td><td>P2.2</td><td>SCLK0</td></tr>
<tr><td>20</td><td>20</td><td>P2.3</td><td>$\overline{SSEL0}$</td></tr>
<tr><td>50</td><td>50</td><td>P2.4</td><td>TCK</td></tr>
<tr><td>51</td><td>51</td><td>P2.5</td><td>TDI</td></tr>
<tr><td>53</td><td>53</td><td>P2.6</td><td>TMS</td></tr>
<tr><td>54</td><td>54</td><td>P2.7</td><td>TDO</td></tr>
</table>
</td></tr>
<tr><td rowspan="11">33–37, 39, 40, 42</td><td rowspan="11">33–40</td><td rowspan="11">P3.0–P3.7; INT8–INT15</td><td>General-Purpose, Digital, I/O, Type D Port; External Edge-Selectable Interrupt. These port pins function as bidirectional I/O pins or as interrupts. All port pins default to three-state mode after a reset. All interrupt functions must be enabled from software.</td></tr>
<tr><td>
<table>
<tr><th>MAXQ612</th><th>MAXQ622</th><th>PORT</th><th>SPECIAL FUNCTION</th></tr>
<tr><td>33</td><td>33</td><td>P3.0</td><td>INT8</td></tr>
<tr><td>34</td><td>34</td><td>P3.1</td><td>INT9</td></tr>
<tr><td>35</td><td>35</td><td>P3.2</td><td>INT10</td></tr>
<tr><td>36</td><td>36</td><td>P3.3</td><td>INT11</td></tr>
<tr><td>37</td><td>37</td><td>P3.4</td><td>INT12</td></tr>
<tr><td>39</td><td>38</td><td>P3.5</td><td>INT13</td></tr>
<tr><td>40</td><td>39</td><td>P3.6</td><td>INT14</td></tr>
<tr><td>42</td><td>40</td><td>P3.7</td><td>INT15</td></tr>
</table>
</td></tr>
<tr><td rowspan="11">65–72</td><td rowspan="11">65–72</td><td rowspan="11">P4.0–P4.7</td><td>General-Purpose, Digital, I/O, Type C Port. These port pins function as bidirectional I/O pins. All port pins default to three-state mode after a reset.</td></tr>
<tr><td>
<table>
<tr><th>MAXQ612</th><th>MAXQ622</th><th>PORT</th><th>SPECIAL FUNCTION</th></tr>
<tr><td>65</td><td>65</td><td>P4.0</td><td>—</td></tr>
<tr><td>66</td><td>66</td><td>P4.1</td><td>—</td></tr>
<tr><td>67</td><td>67</td><td>P4.2</td><td>—</td></tr>
<tr><td>68</td><td>68</td><td>P4.3</td><td>—</td></tr>
<tr><td>69</td><td>69</td><td>P4.4</td><td>—</td></tr>
<tr><td>70</td><td>70</td><td>P4.5</td><td>—</td></tr>
<tr><td>71</td><td>71</td><td>P4.6</td><td>—</td></tr>
<tr><td>72</td><td>72</td><td>P4.7</td><td>—</td></tr>
</table>
</td></tr>
</table>

Pin Descriptions—Bare Die (continued)

<table>
<tr><th colspan="2">PIN</th><th rowspan="2">NAME</th><th colspan="4">FUNCTION</th></tr>
<tr><th>MAXQ612</th><th>MAXQ622</th></tr>
<tr><td rowspan="6">46–49</td><td rowspan="6">46–49</td><td rowspan="6">P5.0–P5.3; MOSI1, MISO1, SCLK1, $\overline{\text{SSEL1}}$</td><td colspan="4">General-Purpose, Digital, I/O, Type C Port. These port pins function as bidirectional I/O pins. All port pins default to three-state mode after a reset. All alternate functions must be enabled from software. Enabling the pin's special function disables the general-purpose I/O on the pin.</td></tr>
<tr><td>MAXQ612</td><td>MAXQ622</td><td>PORT</td><td>SPECIAL FUNCTION</td></tr>
<tr><td>46</td><td>46</td><td>P5.0</td><td>MOSI1</td></tr>
<tr><td>47</td><td>47</td><td>P5.1</td><td>MISO1</td></tr>
<tr><td>48</td><td>48</td><td>P5.2</td><td>SCLK1</td></tr>
<tr><td>49</td><td>49</td><td>P5.3</td><td>$\overline{\text{SSEL1}}$</td></tr>
<tr><td rowspan="9">12–15, 38, 41, 43, 44</td><td rowspan="9">12–15, 41–44</td><td rowspan="9">P6.0–P6.7</td><td colspan="4">General-Purpose, Digital, I/O, Type C Port. These port pins function as bidirectional I/O pins. All port pins default to three-state mode after a reset.</td></tr>
<tr><td>MAXQ612</td><td>MAXQ622</td><td>PORT</td><td>SPECIAL FUNCTION</td></tr>
<tr><td>12</td><td>12</td><td>P6.0</td><td>—</td></tr>
<tr><td>13</td><td>13</td><td>P6.1</td><td>—</td></tr>
<tr><td>14</td><td>14</td><td>P6.2</td><td>—</td></tr>
<tr><td>15</td><td>15</td><td>P6.3</td><td>—</td></tr>
<tr><td>38</td><td>41</td><td>P6.4</td><td>—</td></tr>
<tr><td>41</td><td>42</td><td>P6.5</td><td>—</td></tr>
<tr><td>43</td><td>43</td><td>P6.6</td><td>—</td></tr>
<tr><td>44</td><td>44</td><td>P6.7</td><td>—</td></tr>
<tr><td colspan="6">NO CONNECTION PINS</td></tr>
<tr><td>4, 11, 17, 22–27, 52, 57, 64</td><td>4, 11, 17, 52, 57, 64</td><td>N.C.</td><td colspan="4">No Connection. Reserved for future use. Leave these pins unconnected.</td></tr>
</table>

Detailed Description

The MAXQ612/MAXQ622 provide integrated, low-cost solutions that simplify the design of IR communications equipment such as universal remote controls. Standard features include the highly optimized, single-cycle, MAXQ, 16-bit RISC core; 128KB of flash memory; 6KB data RAM; soft stack; 16 general-purpose registers; and three data pointers. The MAXQ core has the industry's best MIPS/mA rating, allowing developers to achieve the same performance as competing microcontrollers at substantially lower clock rates. Lower active-mode current combined with the even lower MAXQ612/MAXQ622 stop-mode current results in increased battery life. IR application-specific peripherals include flexible timers for generating IR carrier frequencies and modulation. A high-current, 25mA, IR drive pin and output pins capable of sinking up to 5mA support IR applications. It also includes a USB slave interface compatible with existing host HID device drivers, I^2C, dual SPI, dual USARTs, up to 56 general-purpose I/O pins ideal for keypad matrix input, and a power-fail-detection circuit to notify.

Operating from DC to 12MHz, almost all instructions execute in a single clock cycle (83.3ns at 12MHz), enabling nearly 12MIPS true-code operation. When active device operation is not required, an ultra-low-power stop mode can be invoked from software, resulting in quiescent current consumption of less than 300nA typical and 3µA maximum. The combination of high-performance instructions and ultra-low

stop-mode current increases battery life over competing microcontrollers. An integrated POR circuit with brownout support resets the device to a known condition following a power-up cycle or brownout condition. Additionally, a power-fail warning flag is set, and a power-fail interrupt can be generated when the system voltage falls below the power-fail warning voltage, V_{PFW}. The power-fail warning feature allows the application to notify the user that the system supply is low and appropriate action should be taken.

Microprocessor

The MAXQ612/MAXQ622 are based on Maxim's MAXQ20 core, which is a low-power implementation of the new 16-bit MAXQ family of RISC cores. The core supports the Harvard memory architecture with separate internal 16-bit program and data address buses. A fixed 16-bit instruction word is standard, but data can be arranged in 8 or 16 bits. The MAXQ core is a pipelined processor with performance approaching 1MIPS per MHz. The 16-bit data path is implemented around register modules, and each register module contributes specific functions to the core. The accumulator module consists of sixteen 16-bit registers and is tightly coupled with the arithmetic logic unit (ALU). Program flow is supported by a configurable soft stack.

Execution of instructions is triggered by data transfer between functional register modules or between a functional register module and memory. Because data movement involves only source and destination modules, circuit switching activities are limited to active modules only. For power-conscious applications, this approach localizes power dissipation and minimizes switching noise. The modular architecture also provides a maximum of flexibility and reusability that are important for a microprocessor used in embedded applications.

The MAXQ instruction set is highly orthogonal. All arithmetical and logical operations can use any register in conjunction with the accumulator. Data movement is supported from any register to any other register. Memory is accessed through specific data-pointer registers with autoincrement/decrement support.

Memory

The microcontroller incorporates several memory types:

- 128KB program flash memory
- 6KB SRAM data memory
- 6KB utility ROM
- Soft stack

Memory Protection

The optional memory-protection feature separates code memory into three areas: system, user loader, and user application. Code in the system area can be kept confidential. Code in the user areas can be prevented from reading and writing system code. The user loader can also be protected from user application code.

Memory protection is implemented using privilege levels for code. Each area has an associated privilege level. RAM/ROM are assigned privilege levels as well. Refer to the *MAXQ622 User's Guide* for a more thorough explanation of the topic.

Stack Memory

A 16-bit-wide internal stack provides storage for program return addresses and can also be used for general-purpose data storage. The stack is used automatically by the processor when the CALL, RET, and RETI instructions are executed and when an interrupt is serviced. An application can also store values in the stack explicitly by using the PUSH, POP, and POPI instructions.

On reset, the stack pointer, SP, initializes to the top of the stack (BF0h). The CALL, PUSH, and interrupt-vectoring operations decrement SP, then store a value at the location pointed to by SP. The RET, RETI, POP, and POPI operations retrieve the value at SP and then increment SP.

Utility ROM

The utility ROM is a 6KB block of internal ROM memory that defaults to a starting address of 8000h. The utility

Table 1. Memory Areas and Associated Maximum Privilege Levels

AREA	PAGE ADDRESS	MAXIMUM PRIVILEGE LEVEL
System	0 to ULDR-1	High
User Loader	ULDR to UAPP-1	Medium
User Application	UAPP to top	Low
Utility ROM	N/A	High
Other (RAM)	N/A	Low

The IR timer is composed of a carrier generator and a carrier modulator. The carrier generation module uses the 16-bit IR carrier register (IRCA) to define the high and low time of the carrier through the IR carrier high byte (IRCAH) and IR carrier low byte (IRCAL). The carrier modulator uses the IR data bit (IRDATA) and IR modulator time register (IRMT) to determine whether the carrier or the idle condition is present on IRTX.

Carrier Generation Module

The IRCAH byte defines the carrier high time in terms of the number of IR input clocks, whereas the IRCAL byte defines the carrier low time.

- IR Input Clock (f_{IRCLK}) = $f_{SYS}/2^{IRDIV[1:0]}$
- Carrier Frequency ($f_{CARRIER}$) = f_{IRCLK}/(IRCAH + IRCAL + 2)
- Carrier High Time = IRCAH + 1
- Carrier Low Time = IRCAL + 1
- Carrier Duty Cycle = (IRCAH + 1)/(IRCAH + IRCAL + 2)

During transmission, the IRCA register is latched for each IRV downcount interval, and is sampled along with the IRTXPOL and IRDATA bits at the beginning of each new IRV downcount interval so that duty-cycle variation and frequency shifting is possible from one interval to the next. The starting/idle state and the carrier polarity of the IRTX pin can be configured when the IR timer is enabled.

IR Transmission

During IR transmission (IRMODE = 1), the carrier generator creates the appropriate carrier waveform, while the carrier modulator performs the modulation. The carrier modulation can be performed as a function of carrier cycles or IRCLK cycles dependent on the setting of the IRCFME bit. When IRCFME = 0, the IRV down counter is clocked by the carrier frequency and thus the modulation is a function of carrier cycles. When IRCFME = 1, the IRV down counter is clocked by IRCLK, allowing carrier modulation timing with IRCLK resolution.

The IRTXPOL bit defines the starting/idle state as well as the carrier polarity for the IRTX pin. If IRTXPOL = 1, the IRTX pin is set to a logic-high when the IR timer module is enabled. If IRTXPOL = 0, the IRTX pin is set to a logic-low when the IR timer is enabled.

A separate register bit, IR data (IRDATA), is used to determine whether the carrier generator output is output to the IRTX pin for the next IRMT carrier cycles. When IRDATA = 1, the carrier waveform (or inversion of this waveform if IRTXPOL = 1) is output on the IRTX pin during the next IRMT cycles. When IRDATA = 0, the idle condition, as defined by IRTXPOL, is output on the IRTX pin during the next IRMT cycles.

The IR timer acts as a down counter in transmit mode. An IR transmission starts when the IREN bit is set to 1 when IRMODE = 1; when the IRMODE bit is set to 1 when IREN = 1; or when IREN and IRMODE are both set to 1 in the same instruction. The IRMT and IRCA registers, along with the IRDATA and IRTXPOL bits, are sampled at the beginning of the transmit process and every time the IR timer value reload its value. When the IRV reaches 0000h value, on the next carrier clock, it does the following:

1) Reloads IRV with IRMT.
2) Samples IRCA, IRDATA, and IRTXPOL.
3) Generates IRTX accordingly.
4) Sets IRIF to 1.
5) Generates an interrupt to the CPU if enabled (IRIE = 1).

IR Transmit—Independent External Carrier and Modulator Outputs

The normal transmit mode modulates the carrier based upon the IRDATA bit. However, the user has the option to input the modulator (envelope) on an external pin if desired. The IRDATA bit is output directly to the IRTXM pin (if IRTXPOL = 0) on each IRV downcount interval boundary just as if it were being used to internally modulate the carrier frequency. If IRTXPOL = 1, the inverse of the IRDATA bit is output to the IRTXM pin on the IRV interval downcount boundaries. When the envelope mode is enabled, it is possible to output either the modulated (IRENV[1:0] = 01b) or unmodulated (INENV[1:0] = 10b) carrier to the IRTX pin.

IR Receive

When configured in receive mode (IRMODE = 0), the IR hardware supports the IRRX capture function. The IRRXSEL[1:0] bits define which edge(s) of the IRRX pin should trigger the IR timer capture function. Once started, the IR timer (IRV) starts up counting from 0000h when a qualified capture event as defined by IRRXSEL happens. The IRV register is, by default, counting carrier cycles as defined by the IRCA register. However, the IR carrier frequency detect (IRCFME) allows clocking of the IRV register directly with the IRCLK for finer resolution. When IRCFME = 0, the IRCA defined carrier is counted by IRV. When IRCFME = 1, the IRCLK clocks the IRV register.

On the next qualified event, it does the following:

1) Captures the IRRX pin state and transfers its value to IRDATA. If a falling edge occurs, IRDATA = 0. If a rising edge occurs, IRDATA = 1.

- Programmable 9th bit parity support
- Start/stop bit support

Serial Peripheral Interface (SPI)

The dual-integrated SPI interfaces provide independent serial communication channels that communicate synchronously with peripheral devices in a multiple master or multiple slave system. The interface allows access to a 4-wire, full-duplex serial bus, and can be operated in either master mode or slave mode. Collision detection is provided when two or more masters attempt a data transfer at the same time.

The maximum SPI master transfer rate is Sysclk/2. When operating as an SPI slave, the MAXQ612/MAXQ622 can support up to Sysclk/4 SPI transfer rate. Data is transferred as an 8-bit or 16-bit value, MSB first. In addition, the SPI module supports configuration of an active $\overline{SSEL}$ state through the slave active select. Separate pins and registers are used to differentiate between the two SPI ports.

I²C Bus

The microcontroller integrates an internal I²C bus master/slave for communication with a wide variety of other I²C–enabled peripherals. The I²C bus is a 2-wire, bidirectional bus using two bus lines—the serial data line (SDA) and the serial clock line (SCL)—and a ground line. Both the SDA and SDL lines must be driven as open-collector/drain outputs. External resistors are required as shown in Figure 1 to pull the lines to a logic-high state.

The device supports both the master and slave protocols. In the master mode, the device has ownership of the I²C bus, drives the clock, and generates the START and STOP signals. This allows it to send data to a slave or receive data from a slave as required. In slave mode, the device relies on an externally generated clock to drive SCL and responds to data and commands only when requested by the I²C master device.

USB Controller (MAXQ622 Only)

The integrated USB controller is compliant with the USB 2.0 specification, providing full-speed operation with the newest generation of USB peripherals. The USB controller functions as a full-speed USB peripheral device. Integrating the USB physical interface (PHY) allows direct connection to the USB cable, reducing board space and overall system cost. A system interrupt can be enabled to signal that the USB needs to be serviced. The CPU communicates to the USB controller module through the SFR interface. The microcontroller is seen by a USB host as a peripheral, characterized by the following endpoints:

- EP0: Bidirectional CONTROL endpoint with a 64-byte data storage.
- EP1-OUT: BULK (or INT) OUT endpoint. Double-buffered 64 bytes data storage.
- EP2-IN: BULK (or INT) IN endpoint. Double-buffered 64 bytes data storage.
- EP3-IN: BULK (or INT) IN endpoint. Single-buffered 64 bytes data storage.

The choice to use EP1, EP2, and EP3 as BULK or INTERRUPT endpoints is strictly a function of the endpoint descriptors that the USB controller returns to the USB host during enumeration.

The USB controller communicates to a total of 384 bytes of endpoint data memory (2 x 64 bytes for each data moving endpoint EP1 and EP2), 64 bytes for the CONTROL endpoint, and 64 bytes for endpoint EP3.

Double-buffering EP1 and EP2 improves throughput by allowing the CPU to read or load the next packet while the USB controller is moving the current packet over USB. EP3-IN is intended to serve as a large interrupt endpoint for various USB class specifications such as the Still Image Capture Device. It can also be used as a second BULK IN endpoint.

On-Chip Oscillator

An external quartz crystal or a ceramic resonator can be connected between HFXIN and HFXOUT, as illustrated in Figure 3.

To operate the core from an external clock, connect the clock source to the HFXIN pin and connect the HFXOUT

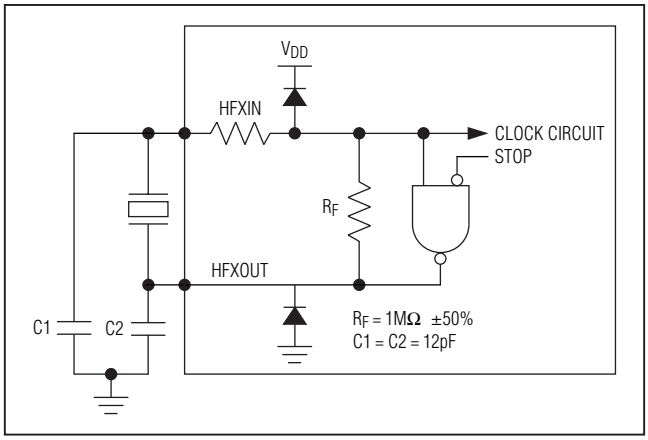


Figure 3. On-Chip Oscillator

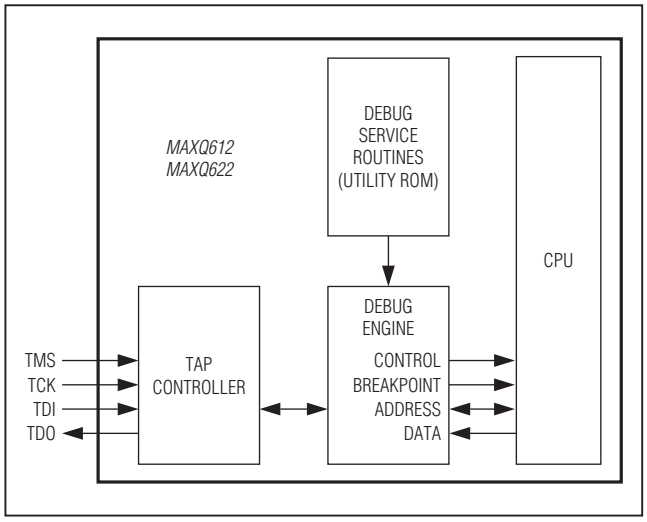


Figure 4. In-Circuit Debugger

master that can either be automatic test equipment or a component that interfaces to a higher level test bus as part of a complete system. The communication operates across a 4-wire serial interface from a dedicated TAP that is compatible with the JTAG IEEE Standard 1149. The TAP provides an independent serial channel to communicate synchronously with the host system.

To prevent unauthorized access of the protected memory regions through the JTAG interface, the debug engine prevents modification of the privilege registers and disallows all access to system memory, unless memory protection is disabled. In addition, all services (such as register display or modification) are denied when code is executing inside the system area.

Operating Modes

Power-Supply Selection

For maximum flexibility the microcontroller can be powered by either the USB (V_{BUS}) or V_{DD}. When a USB connection is made to a valid V_{BUS} power source, an internal voltage regulator generates a 3.3V supply voltage. When the internal voltage is at an adequate level, it automatically powers itself from the USB supply. This is especially beneficial in systems where the V_{DD} supply is from a battery. In either case, the chip is fully functional when operating from either the battery or the V_{BUS}.

The power monitor is attached to the switched supply, V_{DDIO}. This supply is equivalent to the higher of V_{DDB} or V_{DD}. This can be expressed as follows:

If (V_{DDB} > 3.0V or V_{DDB} > V_{DD})

then (V_{DDIO} = V_{DDB})

else (V_{DDIO} = V_{DD})

This means that if there is a power-fail event on V_{DD} and the device is not powered from V_{BUS}, it causes a power-fail interrupt (PFI) if enabled. If the device is powered by V_{BUS} and there is a supply on V_{DD}, then no power-fail event is triggered. If the device is powered by V_{BUS} and there is no supply on V_{DD} and V_{BUS} fails, the chip attempts to switch to V_{DD}, detects a power-fail event, and a PFI occurs. Some specific examples are given below:

- **Case 1: The device is powered from V_{DD} and the batteries are removed.** Power decays until the power-fail-reset trip point is hit, then the part goes into low-power mode.
- **Case 2: The device is set to be powered from V_{DD} only, it is connected to USB, and the batteries are removed.** Response is identical to Case 1.
- **Case 3: The device is set to be powered from either V_{DD} or V_{BUS}, it is connected to USB, and the batteries are removed.** Because the part is already powered from V_{BUS}, nothing changes. If the USB port is subsequently disconnected, power switches over to V_{DD}, the supply decays to the power-fail-reset trip point, and the part goes into low-power mode. As long as there is sufficient charge on the V_{DD} bypass capacitor, it supports the part in power-fail. The hold-up time is similar to the MAXQ610 since the USB port is powered only by V_{BUS}. Note that if the part is powered from V_{BUS} and no battery has been present for a long time (V_{DD} = 0), then upon USB port disconnection, the power collapses to ground in less than a second.

Stop Mode

The lowest power mode of operation is stop mode. In this mode, CPU state and memories are preserved, but the CPU is not actively running. Wake-up sources include external I/O interrupts, the power-fail warning interrupt, wake-up timer, or a power-fail reset. Any time the microcontroller is in a state where code does not need to be executed, the user software can put the microcontroller into stop mode. The nanopower ring oscillator is an internal ultra-low-power (400nA) 8kHz ring oscillator that can be used to drive a wake-up timer that exits stop mode. The wake-up timer is programmable by software in steps of 125µs up to approximately 8s.

The power-fail monitor is always on during normal operation. However, it can be selectively disabled during stop

Table 4. Power-Fail Warning Level Selection

PWCN.PFWARNCN[1:0]	PFW THRESHOLD (V)
00	1.8
01	1.9
10	2.55
11	2.75

mode to minimize power consumption. This feature is enabled using the power-fail monitor disable (PFD) bit in the PWCN register. The reset default state for the PFD bit is 1, which disables the power-fail monitor function during stop mode. If power-fail monitoring is disabled (PFD = 1) during stop mode, the circuitry responsible for generating a power-fail warning or reset is shut down and neither condition is detected. Thus, the $V_{DD} < V_{RST}$ condition does not invoke a reset state. However, in the event that V_{DD} falls below the POR level, a POR is generated. The power-fail monitor is enabled prior to stop mode exit and before code execution begins. If a power-fail warning condition ($V_{DD} < V_{PFW}$) is then detected, the power-fail interrupt flag is set on stop mode exit. If a power-fail reset condition is detected ($V_{DD} < V_{RST}$), the CPU goes into reset.

Power-Fail Warning

The power-fail monitor can assert an interrupt if the voltage falls below a configurable threshold between the operating voltage and the reset voltage. This, if enabled, can allow the firmware to perform housekeeping tasks if the voltage level decays below the warning threshold. The power-fail threshold value should only be changed when the power-fail warning interrupt is disabled (CKCN. PFIE = 0) to prevent unintended triggering of the power-fail warning condition.

The power-fail warning threshold is reset to 1.8V by a POR and is not affected by other resets. See Table 4.

Power-Fail Detection

Figures 5, 6, and 7 show the power-fail detection and response during normal and stop-mode operation.

If a reset is caused by a power-fail, the power-fail monitor can be set to one of the following intervals:

- Always on—continuous monitoring
- 2^{11} nanopower ring oscillator clocks (~256ms)
- 2^{12} nanopower ring oscillator clocks (~512ms)
- 2^{13} nanopower ring oscillator clocks (~1.024s)

In the case where the power-fail circuitry is periodically turned on, the power-fail detection is turned on for two

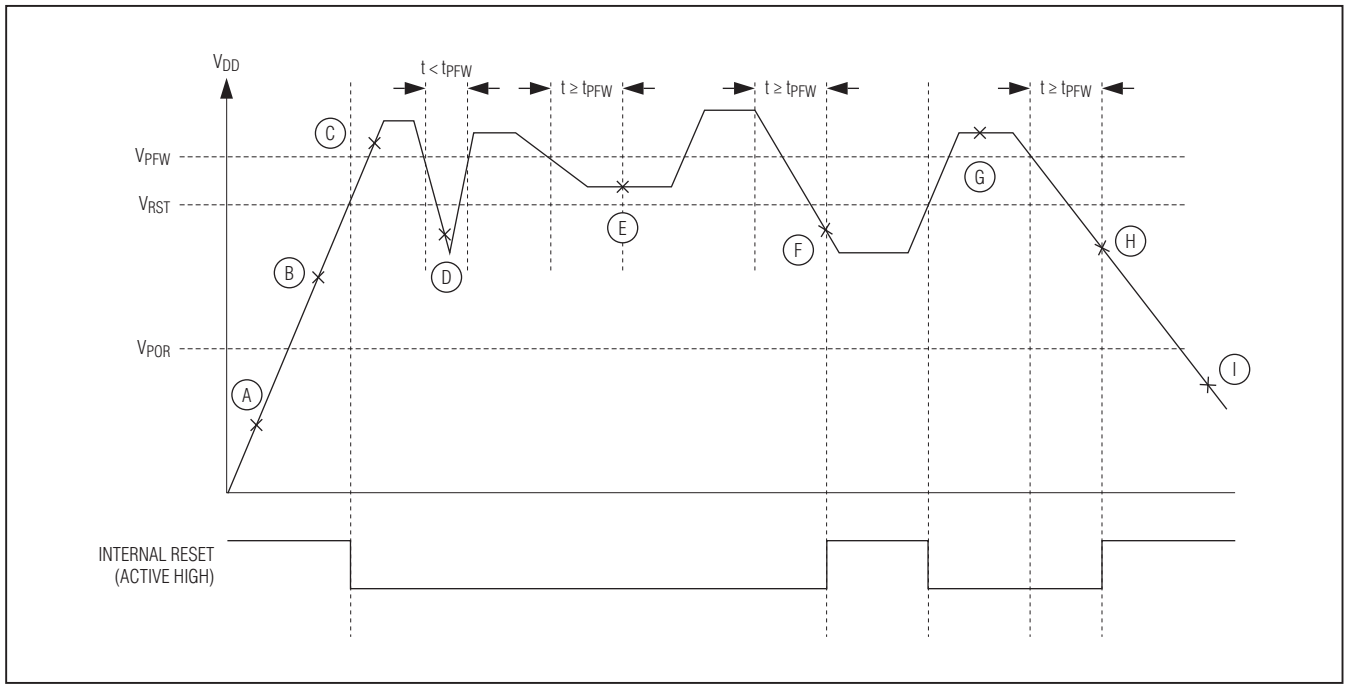


Figure 5. Power-Fail Detection During Normal Operation

Table 5. Power-Fail Detection States During Normal Operation

STATE	POWER-FAIL	INTERNAL REGULATOR	CRYSTAL OSCILLATOR	SRAM RETENTION	COMMENTS
A	On	Off	Off	—	$V_{DD} < V_{POR}$.
B	On	On	On	—	$V_{POR} < V_{DD} < V_{RST}$. Crystal warmup time, t_{XTAL_RDY}. CPU held in reset.
C	On	On	On	—	$V_{DD} > V_{RST}$. CPU normal operation.
D	On	On	On	—	Power drop too short. Power-fail not detected.
E	On	On	On	—	$V_{RST} < V_{DD} < V_{PFW}$. PFI is set when $V_{RST} < V_{DD} < V_{PFW}$ and maintains this state for at least t_{PFW}, at which time a power-fail interrupt is generated (if enabled). CPU continues normal operation.
F	On (Periodically)	Off	Off	Yes	$V_{POR} < V_{DD} < V_{RST}$. Power-fail detected. CPU goes into reset. Power-fail monitor turns on periodically.
G	On	On	On	—	$V_{DD} > V_{RST}$. Crystal warmup time, t_{XTAL_RDY}. CPU resumes normal operation from 8000h.
H	On (Periodically)	Off	Off	Yes	$V_{POR} < V_{DD} < V_{RST}$. Power-fail detected. CPU goes into reset. Power-fail monitor turns on periodically.
I	Off	Off	Off	—	$V_{DD} < V_{POR}$. Device held in reset. No operation allowed.

nanopower ring-oscillator cycles. If $V_{DD} > V_{RST}$ during detection, V_{DD} is monitored for an additional nanopower ring-oscillator period. If V_{DD} remains above V_{RST} for the third nanopower ring period, the CPU exits the reset state and resumes normal operation from utility ROM at 8000h after satisfying the crystal warmup period.

If a reset is generated by any other event, such as the $\overline{\text{RESET}}$ pin being driven low externally or the watchdog timer, the power-fail, internal regulator, and crystal remain on during the CPU reset. In these cases, the CPU exits the reset state in less than 20 crystal cycles after the reset source is removed.

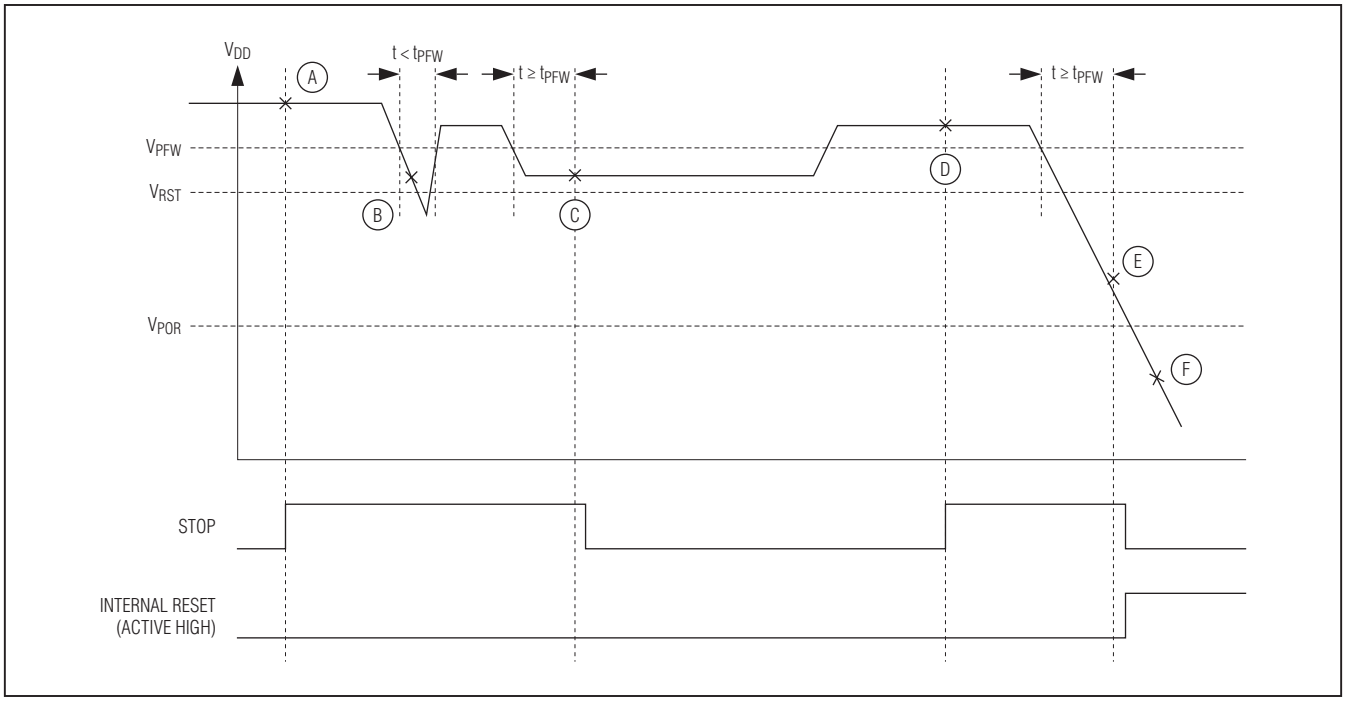


Figure 6. Stop Mode Power-Fail Detection States with Power-Fail Monitor Enabled

Table 6. Stop Mode Power-Fail Detection States with Power-Fail Monitor Enabled

STATE	POWER-FAIL	INTERNAL REGULATOR	CRYSTAL OSCILLATOR	SRAM RETENTION	COMMENTS
A	On	Off	Off	Yes	Application enters stop mode. $V_{DD} > V_{RST}$. CPU in stop mode.
B	On	Off	Off	Yes	Power drop too short. Power-fail not detected.
C	On	On	On	Yes	$V_{RST} < V_{DD} < V_{PFW}$. Power-fail warning detected. Turn on regulator and crystal. Crystal warmup time, t_{XTAL_RDY}. Exit stop mode.
D	On	Off	Off	Yes	Application enters stop mode. $V_{DD} > V_{RST}$. CPU in stop mode.
E	On (Periodically)	Off	Off	Yes	$V_{POR} < V_{DD} < V_{RST}$. Power-fail detected. CPU goes into reset. Power-fail monitor turns on periodically.
F	Off	Off	Off	—	$V_{DD} < V_{POR}$. Device held in reset. No operation allowed.

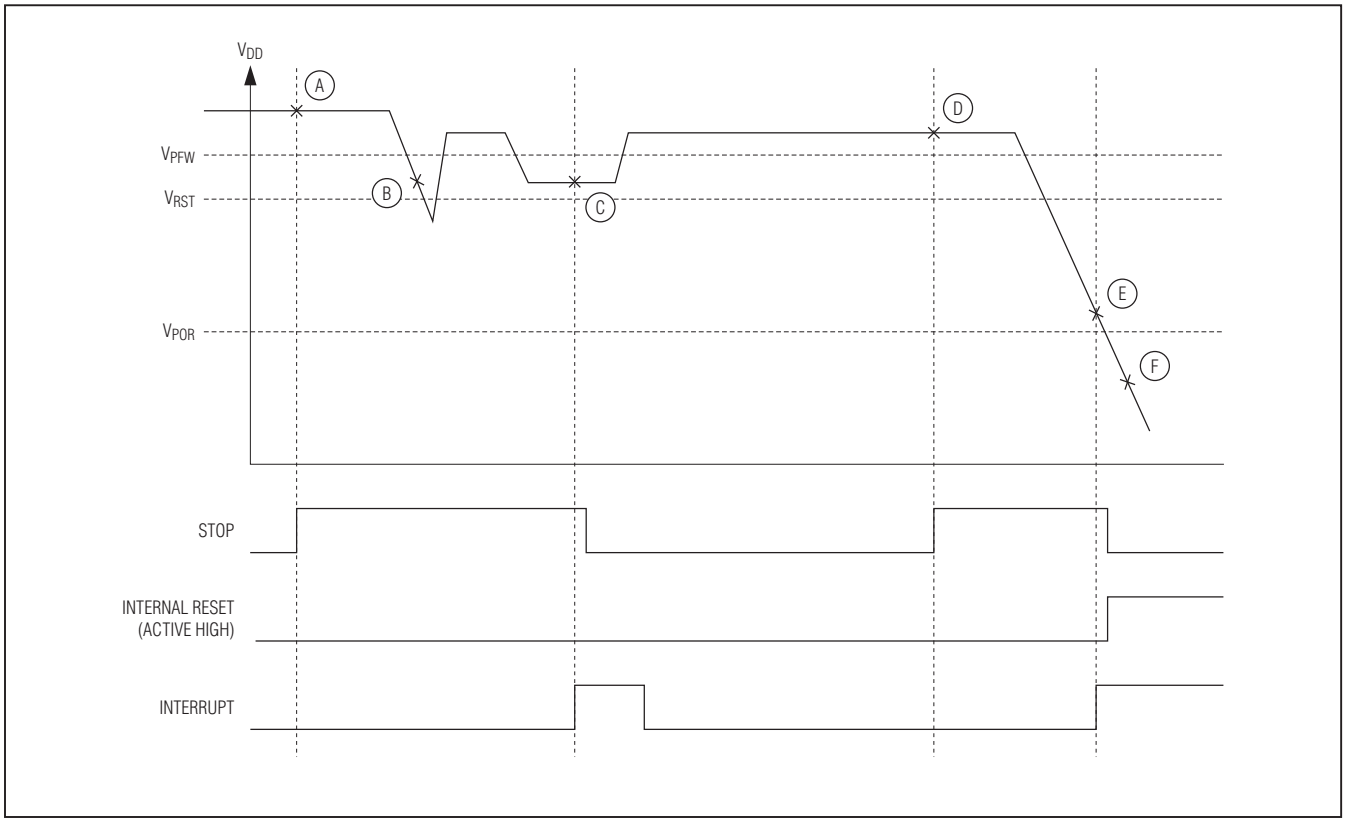


Figure 7. Stop Mode Power-Fail Detection with Power-Fail Monitor Disabled

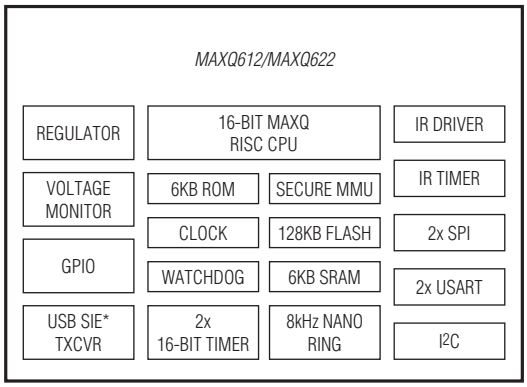
Table 7. Stop Mode Power-Fail Detection States with Power-Fail Monitor Disabled

STATE	POWER-FAIL	INTERNAL REGULATOR	CRYSTAL OSCILLATOR	SRAM RETENTION	COMMENTS
A	Off	Off	Off	Yes	Application enters stop mode. $V_{DD} > V_{RST}$. CPU in stop mode.
B	Off	Off	Off	Yes	$V_{DD} < V_{PFW}$. Power-fail not detected because power-fail monitor is disabled.
C	On	On	On	Yes	$V_{RST} < V_{DD} < V_{PFW}$. An interrupt occurs that causes the CPU to exit stop mode. Power-fail monitor is turned on, detects a power-fail warning, and sets the power-fail interrupt flag. Turn on regulator and crystal. Crystal warmup time, t_{XTAL_RDY}. On stop mode exit, CPU vectors to the higher priority of power-fail and the interrupt that causes stop mode exit.

MAXQ612/MAXQ622

16-Bit Microcontrollers with Infrared Module and Optional USB

Block Diagram



Development and Technical Support

Maxim and third-party suppliers provide a variety of highly versatile, affordably priced development tools for this microcontroller, including the following:

- Compilers
- In-circuit emulators
- Integrated Development Environments (IDEs)
- JTAG-to-serial converters for programming and debugging

A partial list of development tool vendors can be found at **www.maximintegrated.com/MAXQ_tools**.

For technical support, go to **https://support.maximintegrated.com/micro**.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
64 LQFP	C64+5	21-0083	90-0141
44 TQFN-EP	T4477+2	21-0144	90-0127

Ordering Information/Selector Guide

PART	TEMP RANGE	OPERATING VOLTAGE (V)	PROGRAM MEMORY (KB)	DATA MEMORY (KB)	USB FULL SPEED	PIN-PACKAGE
MAXQ612J-0000+	0°C to +70°C	1.7 to 3.6	128 Flash	6	No	44 TQFN-EP*
MAXQ612G-0000+	0°C to +70°C	1.7 to 3.6	128 Flash	6	No	64 LQFP
MAXQ622G-0000+	0°C to +70°C	1.7 to 3.6	128 Flash	6	Yes	64 LQFP

Note: *The 4-digit suffix "-0000" indicates a microcontroller in the default state with the flash memory unprogrammed. Any value other than 0000 indicates a device preprogrammed at Maxim with proprietary customer-supplied software. For more information on factory preprogramming of these devices, contact Maxim at https://support.maximintegrated.com/micro. Information on masked ROM devices and bare die versions for most of these devices are available. Contact the factory for availability.*

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*