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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I²C, IrDA, Microwire, SPI, SSI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT
Number of I/O	70
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1763fbd100-551

Table 5. Pin description *…continued*

Symbol	Pin/ball				Type	Description
	LQFP100	TFBGA100	WLCSP100			
P1[25]/MCOA1/ MAT1[1]	39	G5	F9	[1]	I/O	**P1[25] —** General purpose digital input/output pin.
					O	**MCOA1 —** Motor control PWM channel 1, output A.
					O	**MAT1[1] —** Match output for Timer 1, channel 1.
P1[26]/MCOB1/ PWM1[6]/CAP0[0]	40	K6	E10	[1]	I/O	**P1[26] —** General purpose digital input/output pin.
					O	**MCOB1 —** Motor control PWM channel 1, output B.
					O	**PWM1[6] —** Pulse Width Modulator 1, channel 6 output.
					I	**CAP0[0] —** Capture input for Timer 0, channel 0.
P1[27]/CLKOUT /USB_OVRCR/ CAP0[1]	43	K7	G9	[1]	I/O	**P1[27] —** General purpose digital input/output pin.
					O	**CLKOUT —** Clock output pin.
					I	**USB_OVRCR —** USB port Over-Current status. (LPC1769/68/66/65 only).
					I	**CAP0[1] —** Capture input for Timer 0, channel 1.
P1[28]/MCOA2/ PCAP1[0]/ MAT0[0]	44	J7	G10	[1]	I/O	**P1[28] —** General purpose digital input/output pin.
					O	**MCOA2 —** Motor control PWM channel 2, output A.
					I	**PCAP1[0] —** Capture input for PWM1, channel 0.
					O	**MAT0[0] —** Match output for Timer 0, channel 0.
P1[29]/MCOB2/ PCAP1[1]/ MAT0[1]	45	G6	G8	[1]	I/O	**P1[29] —** General purpose digital input/output pin.
					O	**MCOB2 —** Motor control PWM channel 2, output B.
					I	**PCAP1[1] —** Capture input for PWM1, channel 1.
					O	**MAT0[1] —** Match output for Timer 0, channel 1.
P1[30]/V_{BUS}/ AD0[4]	21	H1	B8	[2]	I/O	**P1[30] —** General purpose digital input/output pin.
					I	**V_{BUS} —** Monitors the presence of USB bus power. (LPC1769/68/66/65/64 only). **Note:** This signal must be HIGH for USB reset to occur.
					I	**AD0[4] —** A/D converter 0, input 4.
P1[31]/SCK1/ AD0[5]	20	F4	C7	[2]	I/O	**P1[31] —** General purpose digital input/output pin.
					I/O	**SCK1 —** Serial Clock for SSP1.
					I	**AD0[5] —** A/D converter 0, input 5.
P2[0] to P2[31]					I/O	**Port 2:** Port 2 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 2 pins depends upon the pin function selected via the pin connect block. Pins 14 through 31 of this port are not available.
P2[0]/PWM1[1]/ TXD1	75	B9	K1	[1]	I/O	**P2[0] —** General purpose digital input/output pin.
					O	**PWM1[1] —** Pulse Width Modulator 1, channel 1 output.
					O	**TXD1 —** Transmitter output for UART1.
P2[1]/PWM1[2]/ RXD1	74	B10	J2	[1]	I/O	**P2[1] —** General purpose digital input/output pin.
					O	**PWM1[2] —** Pulse Width Modulator 1, channel 2 output.
					I	**RXD1 —** Receiver input for UART1.

Table 5. Pin description *…continued*

Symbol	Pin/ball				Type	Description
	LQFP100	TFBGA100	WLCSP100			
P2[11]/$\overline{\text{EINT1}}$/ I2STX_CLK	52	H8	J8	[6]	I/O	**P2[11] —** General purpose digital input/output pin.
					I	**$\overline{\text{EINT1}}$ —** External interrupt 1 input.
					I/O	**I2STX_CLK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*. (LPC1769/68/67/66/65/63 only).
P2[12]/$\overline{\text{EINT2}}$/ I2STX_WS	51	K10	K10	[6]	I/O	**P2[12] —** General purpose digital input/output pin.
					I	**$\overline{\text{EINT2}}$ —** External interrupt 2 input.
					I/O	**I2STX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*. (LPC1769/68/67/66/65/63 only).
P2[13]/$\overline{\text{EINT3}}$/ I2STX_SDA	50	J9	J9	[6]	I/O	**P2[13] —** General purpose digital input/output pin.
					I	**$\overline{\text{EINT3}}$ —** External interrupt 3 input.
					I/O	**I2STX_SDA —** Transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*. (LPC1769/68/67/66/65/63 only).
P3[0] to P3[31]					I/O	**Port 3:** Port 3 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 3 pins depends upon the pin function selected via the pin connect block. Pins 0 through 24, and 27 through 31 of this port are not available.
P3[25]/MAT0[0]/ PWM1[2]	27	H3	D8	[1]	I/O	**P3[25] —** General purpose digital input/output pin.
					O	**MAT0[0] —** Match output for Timer 0, channel 0.
					O	**PWM1[2] —** Pulse Width Modulator 1, output 2.
P3[26]/STCLK/ MAT0[1]/PWM1[3]	26	K1	A10	[1]	I/O	**P3[26] —** General purpose digital input/output pin.
					I	**STCLK —** System tick timer clock input. The maximum STCLK frequency is 1/4 of the Arm processor clock frequency CCLK.
					O	**MAT0[1] —** Match output for Timer 0, channel 1.
					O	**PWM1[3] —** Pulse Width Modulator 1, output 3.
P4[0] to P4[31]					I/O	**Port 4:** Port 4 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 4 pins depends upon the pin function selected via the pin connect block. Pins 0 through 27, 30, and 31 of this port are not available.
P4[28]/RX_MCLK/ MAT2[0]/TXD3	82	C7	G1	[1]	I/O	**P4[28] —** General purpose digital input/output pin.
					O	**RX_MCLK —** I^2S receive master clock. (LPC1769/68/67/66/65 only).
					O	**MAT2[0] —** Match output for Timer 2, channel 0.
					O	**TXD3 —** Transmitter output for UART3.
P4[29]/TX_MCLK/ MAT2[1]/RXD3	85	E6	F1	[1]	I/O	**P4[29] —** General purpose digital input/output pin.
					O	**TX_MCLK —** I^2S transmit master clock. (LPC1769/68/67/66/65 only).
					O	**MAT2[1] —** Match output for Timer 2, channel 1.
					I	**RXD3 —** Receiver input for UART3.

Table 5. Pin description *…continued*

Symbol	Pin/ball				Type	Description
	LQFP100	TFBGA100	WLCSP100			
TDO/SWO	1	A1	A1	[7]	O	**TDO —** Test Data out for JTAG interface.
					O	**SWO —** Serial wire trace output.
TDI	2	C3	C4	[1][8]	I	**TDI —** Test Data in for JTAG interface.
TMS/SWDIO	3	B1	B3	[1][8]	I	**TMS —** Test Mode Select for JTAG interface.
					I/O	**SWDIO —** Serial wire debug data input/output.
$\overline{\text{TRST}}$	4	C2	A2	[1][8]	I	**$\overline{\text{TRST}}$ —** Test Reset for JTAG interface.
TCK/SWDCLK	5	C1	D4	[7]	I	**TCK —** Test Clock for JTAG interface.
					I	**SWDCLK —** Serial wire clock.
RTCK	100	B2	B2	[7]	O	**RTCK —** JTAG interface control signal.
$\overline{\text{RSTOUT}}$	14	-	-	-	O	**$\overline{\text{RSTOUT}}$ —** This is a 3.3 V pin. LOW on this pin indicates the microcontroller being in Reset state.
$\overline{\text{RESET}}$	17	F3	C6	[9]	I	**External reset input:** A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. TTL with hysteresis, 5 V tolerant.
XTAL1	22	H2	D7	[10][11]	I	Input to the oscillator circuit and internal clock generator circuits.
XTAL2	23	G3	A9	[10][11]	O	Output from the oscillator amplifier.
RTCX1	16	F2	A7	[10][11]	I	Input to the RTC oscillator circuit.
RTCX2	18	G1	B7	[10]	O	Output from the RTC oscillator circuit.
V_{SS}	31, 41, 55, 72, 83, 97	B3, B7, C9, G7, J6, K3	E5, F5, F6, G5, G6, G7	[10]	I	**ground:** 0 V reference.
V_{SSA}	11	E1	B5	[10]	I	**analog ground:** 0 V reference. This should nominally be the same voltage as V_{SS}, but should be isolated to minimize noise and error.
$V_{DD(3V3)}$	28, 54, 71, 96	K2, H9, C10, A3	E4, E6, F7, G4	[10]	I	**3.3 V supply voltage:** This is the power supply voltage for the I/O ports.
$V_{DD(REG)(3V3)}$	42, 84	H6, A7	F4, F10	[10]	I	**3.3 V voltage regulator supply voltage:** This is the supply voltage for the on-chip voltage regulator only.
V_{DDA}	10	E2	A4	[10]	I	**analog 3.3 V pad supply voltage:** This should be nominally the same voltage as $V_{DD(3V3)}$ but should be isolated to minimize noise and error. This voltage is used to power the ADC and DAC. This pin should be tied to 3.3 V if the ADC and DAC are not used.
VREFP	12	E3	A5	[10]	I	**ADC positive reference voltage:** This should be nominally the same voltage as V_{DDA} but should be isolated to minimize noise and error. Level on this pin is used as a reference for ADC and DAC. This pin should be tied to 3.3 V if the ADC and DAC are not used.

- Endpoint Maximum packet size selection (up to USB maximum specification) by software at run time.
- Supports SoftConnect and GoodLink features.
- While USB is in the Suspend mode, the part can enter one of the reduced power modes and wake up on USB activity.
- Supports DMA transfers with all on-chip SRAM blocks on all non-control endpoints.
- Allows dynamic switching between CPU-controlled slave and DMA modes.
- Double buffer implementation for Bulk and Isochronous endpoints.

8.12.2 USB host controller

The host controller enables full- and low-speed data exchange with USB devices attached to the bus. It consists of a register interface, a serial interface engine, and a DMA controller. The register interface complies with the OHCI specification.

8.12.2.1 Features

- OHCI compliant.
- One downstream port.
- Supports port power switching.

8.12.3 USB OTG controller

USB OTG is a supplement to the USB 2.0 specification that augments the capability of existing mobile devices and USB peripherals by adding host functionality for connection to USB peripherals.

The OTG Controller integrates the host controller, device controller, and a master-only I^2C-bus interface to implement OTG dual-role device functionality. The dedicated I^2C-bus interface controls an external OTG transceiver.

8.12.3.1 Features

- Fully compliant with *On-The-Go supplement to the USB 2.0 Specification, Revision 1.0a*.
- Hardware support for Host Negotiation Protocol (HNP).
- Includes a programmable timer required for HNP and Session Request Protocol (SRP).
- Supports any OTG transceiver compliant with the *OTG Transceiver Specification (CEA-2011), Rev. 1.0*.

8.13 CAN controller and acceptance filters

Remark: The CAN controllers are available on parts LPC1769/68/66/65/64. See Table 2.

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real-time control with a very high level of security. Its domain of application ranges from high-speed networks to low cost multiplex wiring.

The CAN block is intended to support multiple CAN buses simultaneously, allowing the device to be used as a gateway, switch, or router among a number of CAN buses in industrial or automotive applications.

8.13.1 Features

- Two CAN controllers and buses.
- Data rates to 1 Mbit/s on each bus.
- 32-bit register and RAM access.
- Compatible with *CAN specification 2.0B, ISO 11898-1*.
- Global Acceptance Filter recognizes standard (11-bit) and extended-frame (29-bit) receive identifiers for all CAN buses.
- Acceptance Filter can provide FullCAN-style automatic reception for selected Standard Identifiers.
- FullCAN messages can generate interrupts.

8.14 12-bit ADC

The LPC17xx contain a single 12-bit successive approximation ADC with eight channels and DMA support.

8.14.1 Features

- 12-bit successive approximation ADC.
- Input multiplexing among 8 pins.
- Power-down mode.
- Measurement range VREFN to VREFP.
- 12-bit conversion rate: 200 kHz.
- Individual channels can be selected for conversion.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition of input pin or Timer Match signal.
- Individual result registers for each ADC channel to reduce interrupt overhead.
- DMA support.

8.15 10-bit DAC

The DAC allows to generate a variable analog output. The maximum output value of the DAC is VREFP.

Remark: The DAC is available on parts LPC1769/68/67/66/65/63. See Table 2.

8.15.1 Features

- 10-bit DAC
- Resistor string architecture
- Buffered output
- Power-down mode
- Selectable output drive
- Dedicated conversion timer
- DMA support

8.20 I²S-bus serial I/O controllers

Remark: The I²S-bus interface is available on parts LPC1769/68/67/66/65/63. See Table 2.

The I²S-bus provides a standard communication interface for digital audio applications.

The *I²S-bus specification* defines a 3-wire serial bus using one data line, one clock line, and one word select signal. The basic I²S-bus connection has one master, which is always the master, and one slave. The I²S-bus interface provides a separate transmit and receive channel, each of which can operate as either a master or a slave.

8.20.1 Features

- The interface has separate input/output channels each of which can operate in master or slave mode.
- Capable of handling 8-bit, 16-bit, and 32-bit word sizes.
- Mono and stereo audio data supported.
- The sampling frequency can range from 16 kHz to 96 kHz (16, 22.05, 32, 44.1, 48, 96) kHz.
- Support for an audio master clock.
- Configurable word select period in master mode (separately for I²S-bus input and output).
- Two 8-word FIFO data buffers are provided, one for transmit and one for receive.
- Generates interrupt requests when buffer levels cross a programmable boundary.
- Two DMA requests, controlled by programmable buffer levels. These are connected to the GPDMA block.
- Controls include reset, stop and mute options separately for I²S-bus input and I²S-bus output.

8.21 General purpose 32-bit timers/external event counters

The LPC17xx include four 32-bit timer/counters. The timer/counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts, generate timed DMA requests, or perform other actions at specified timer values, based on four match registers. Each timer/counter also includes two capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

8.21.1 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler.
- Counter or timer operation.
- Two 32-bit capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.

- Supports single edge controlled and/or double edge controlled PWM outputs. Single edge controlled PWM outputs all go high at the beginning of each cycle unless the output is a constant low. Double edge controlled PWM outputs can have either edge occur at any position within a cycle. This allows for both positive going and negative going pulses.
- Pulse period and width can be any number of timer counts. This allows complete flexibility in the trade-off between resolution and repetition rate. All PWM outputs will occur at the same repetition rate.
- Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses.
- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must ‘release’ new match values before they can become effective.
- May be used as a standard 32-bit timer/counter with a programmable 32-bit prescaler if the PWM mode is not enabled.

8.23 Motor control PWM

The motor control PWM is a specialized PWM supporting 3-phase motors and other combinations. Feedback inputs are provided to automatically sense rotor position and use that information to ramp speed up or down. An abort input is also provided that causes the PWM to immediately release all motor drive outputs. At the same time, the motor control PWM is highly configurable for other generalized timing, counting, capture, and compare applications.

8.24 Quadrature Encoder Interface (QEI)

A quadrature encoder, also known as a 2-channel incremental encoder, converts angular displacement into two pulse signals. By monitoring both the number of pulses and the relative phase of the two signals, the user can track the position, direction of rotation, and velocity. In addition, a third channel, or index signal, can be used to reset the position counter. The quadrature encoder interface decodes the digital pulses from a quadrature encoder wheel to integrate position over time and determine direction of rotation. In addition, the QEI can capture the velocity of the encoder wheel.

8.24.1 Features

- Tracks encoder position.
- Increments/decrements depending on direction.
- Programmable for 2× or 4× position counting.
- Velocity capture using built-in timer.
- Velocity compare function with “less than” interrupt.
- Uses 32-bit registers for position and velocity.
- Three position compare registers with interrupts.
- Index counter for revolution counting.
- Index compare register with interrupts.
- Can combine index and position interrupts to produce an interrupt for whole and partial revolution displacement.

See Figure 6 for an overview of the LPC17xx clock generation.

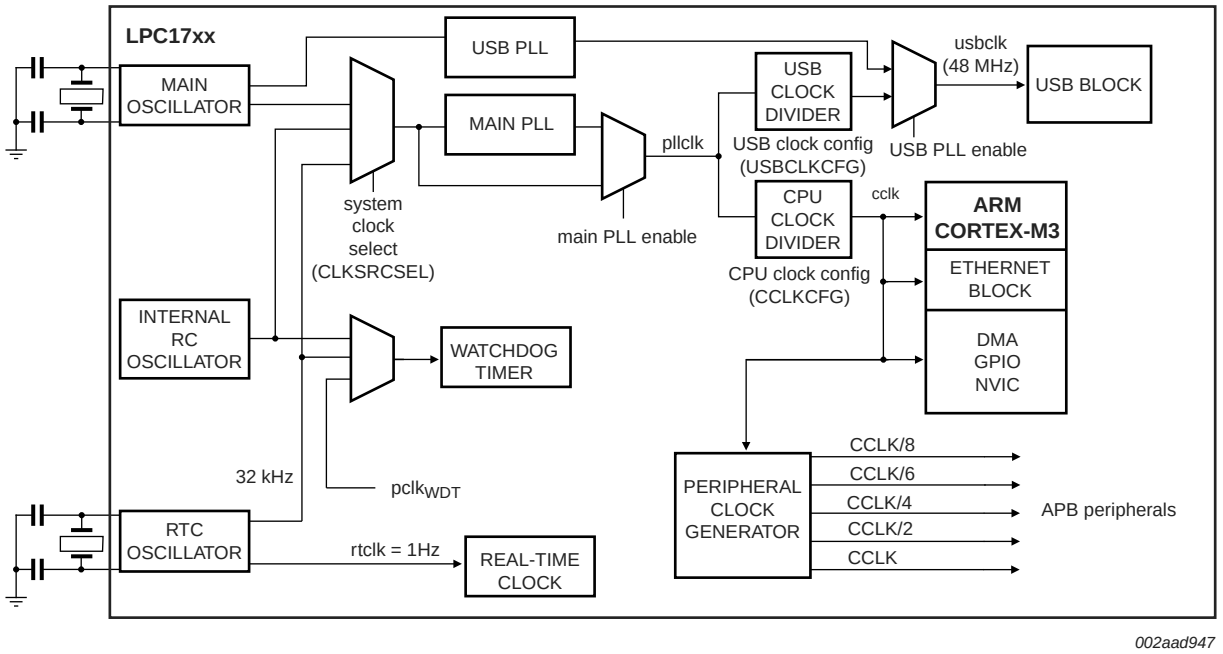


Fig 6. LPC17xx clocking generation block diagram

8.29.1.1 Internal RC oscillator

The IRC may be used as the clock source for the WDT, and/or as the clock that drives the PLL and subsequently the CPU. The nominal IRC frequency is 4 MHz. The IRC is trimmed to 1 % accuracy over the entire voltage and temperature range.

Upon power-up or any chip reset, the LPC17xx use the IRC as the clock source. Software may later switch to one of the other available clock sources.

8.29.1.2 Main oscillator

The main oscillator can be used as the clock source for the CPU, with or without using the PLL. The main oscillator also provides the clock source for the dedicated USB PLL.

The main oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the main PLL. The clock selected as the PLL input is PLLCLKIN. The Arm processor clock frequency is referred to as CCLK elsewhere in this document. The frequencies of PLLCLKIN and CCLK are the same value unless the PLL is active and connected. The clock frequency for each peripheral can be selected individually and is referred to as PCLK. Refer to Section 8.29.2 for additional information.

8.29.1.3 RTC oscillator

The RTC oscillator can be used as the clock source for the RTC block, the main PLL, and/or the CPU.

8.29.2 Main PLL (PLL0)

The PLL0 accepts an input clock frequency in the range of 32 kHz to 25 MHz. The input frequency is multiplied up to a high frequency, then divided down to provide the actual clock used by the CPU and/or the USB block.

The PLL0 input, in the range of 32 kHz to 25 MHz, may initially be divided down by a value ‘N’, which may be in the range of 1 to 256. This input division provides a wide range of output frequencies from the same input frequency.

Following the PLL0 input divider is the PLL0 multiplier. This can multiply the input divider output through the use of a Current Controlled Oscillator (CCO) by a value ‘M’, in the range of 1 through 32768. The resulting frequency must be in the range of 275 MHz to 550 MHz. The multiplier works by dividing the CCO output by the value of M, then using a phase-frequency detector to compare the divided CCO output to the multiplier input. The error value is used to adjust the CCO frequency.

The PLL0 is turned off and bypassed following a chip Reset and by entering Power-down mode. PLL0 is enabled by software only. The program must configure and activate the PLL0, wait for the PLL0 to lock, and then connect to the PLL0 as a clock source.

8.29.3 USB PLL (PLL1)

The LPC17xx contain a second, dedicated USB PLL1 to provide clocking for the USB interface.

The PLL1 receives its clock input from the main oscillator only and provides a fixed 48 MHz clock to the USB block only. The PLL1 is disabled and powered off on reset. If the PLL1 is left disabled, the USB clock will be supplied by the 48 MHz clock from the main PLL0.

The PLL1 accepts an input clock frequency in the range of 10 MHz to 25 MHz only. The input frequency is multiplied up the range of 48 MHz for the USB clock using a Current Controlled Oscillators (CCO). It is insured that the PLL1 output has a 50 % duty cycle.

8.29.4 RTC clock output

The LPC17xx feature a clock output function intended for synchronizing with external devices and for use during system development to allow checking the internal clocks CCLK, IRC clock, main crystal, RTC clock, and USB clock in the outside world. The RTC clock output allows tuning the RTC frequency without probing the pin, which would distort the results.

8.29.5 Wake-up timer

The LPC17xx begin operation at power-up and when awakened from Power-down mode by using the 4 MHz IRC oscillator as the clock source. This allows chip operation to resume quickly. If the main oscillator or the PLL is needed by the application, software will need to enable these features and wait for them to stabilize before they are used as a clock source.

When the main oscillator is initially activated, the wake-up timer allows software to ensure that the main oscillator is fully functional before the processor uses it as a clock source and starts to execute instructions. This is important at power on, all types of Reset, and

whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the wake-up timer.

The Wake-up Timer monitors the crystal oscillator to check whether it is safe to begin code execution. When power is applied to the chip, or when some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient amplitude to drive the clock logic. The amount of time depends on many factors, including the rate of $V_{DD(3V3)}$ ramp (in the case of power on), the type of crystal and its electrical characteristics (if a quartz crystal is used), as well as any other external circuitry (e.g., capacitors), and the characteristics of the oscillator itself under the existing ambient conditions.

8.29.6 Power control

The LPC17xx support a variety of power control features. There are four special modes of processor power reduction: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, Peripheral Power Control allows shutting down the clocks to individual on-chip peripherals, allowing fine tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Each of the peripherals has its own clock divider which provides even better power control.

Integrated PMU (Power Management Unit) automatically adjust internal regulators to minimize power consumption during Sleep, Deep sleep, Power-down, and Deep power-down modes.

The LPC17xx also implement a separate power domain to allow turning off power to the bulk of the device while maintaining operation of the RTC and a small set of registers for storing data during any of the power-down modes.

8.29.6.1 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the Arm core.

In Sleep mode, execution of instructions is suspended until either a Reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

8.29.6.2 Deep-sleep mode

In Deep-sleep mode, the oscillator is shut down and the chip receives no internal clocks. The processor state and registers, peripheral registers, and internal SRAM values are preserved throughout Deep-sleep mode and the logic levels of chip pins remain static. The output of the IRC is disabled but the IRC is not powered down for a fast wake-up later. The RTC oscillator is not stopped because the RTC interrupts may be used as the wake-up source. The PLL is automatically turned off and disconnected. The CCLK and USB clock dividers automatically get reset to zero.

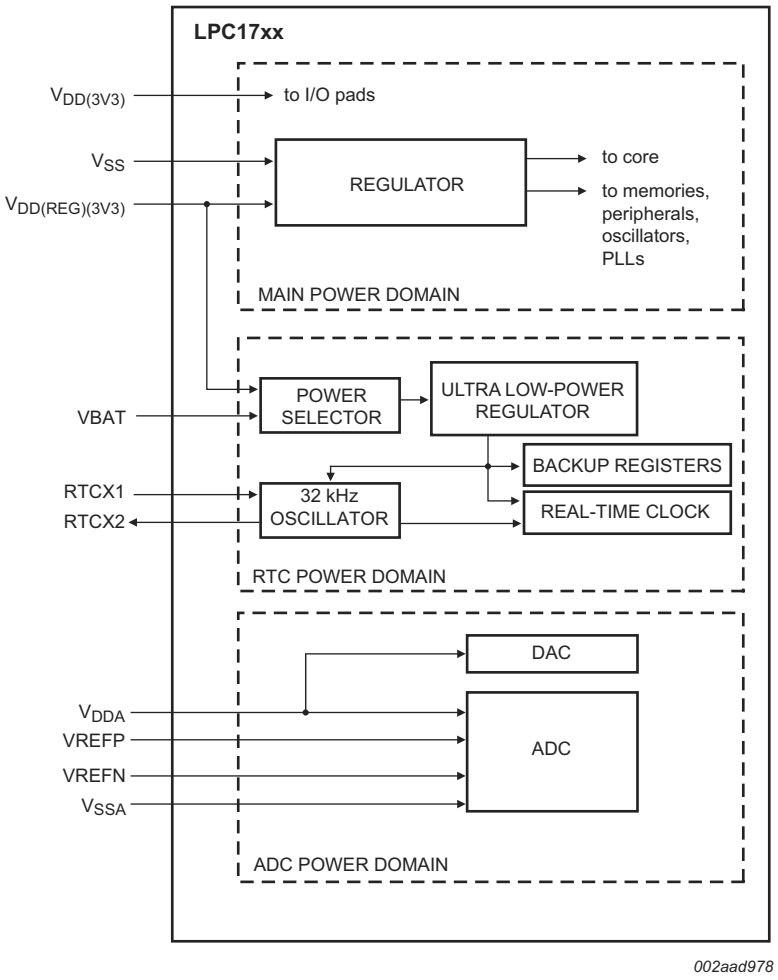


Fig 7. Power distribution

8.30 System control

8.30.1 Reset

Reset has four sources on the LPC17xx: the $\overline{\text{RESET}}$ pin, the Watchdog reset, power-on reset (POR), and the BrownOut Detection (BOD) circuit. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip Reset by any source, once the operating voltage attains a usable level, causes the $\overline{\text{RSTOUT}}$ pin to go LOW and starts the wake-up timer (see description in Section 8.29.5). The wake-up timer ensures that reset remains asserted until the external Reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the flash controller has completed its initialization. Once reset is de-asserted, or, in case of a BOD-triggered reset, once the voltage rises above the BOD threshold, the $\overline{\text{RSTOUT}}$ pin goes HIGH.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the Boot Block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

8.30.2 Brownout detection

The LPC17xx include 2-stage monitoring of the voltage on the $V_{DD(REG)(3V3)}$ pins. If this voltage falls below 2.2 V, the BOD asserts an interrupt signal to the Vectored Interrupt Controller. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC in order to cause a CPU interrupt; if not, software can monitor the signal by reading a dedicated status register.

The second stage of low-voltage detection asserts reset to inactivate the LPC17xx when the voltage on the $V_{DD(REG)(3V3)}$ pins falls below 1.85 V. This reset prevents alteration of the flash as operation of the various elements of the chip would otherwise become unreliable due to low voltage. The BOD circuit maintains this reset down below 1 V, at which point the power-on reset circuitry maintains the overall reset.

Both the 2.2 V and 1.85 V thresholds include some hysteresis. In normal operation, this hysteresis allows the 2.2 V detection to reliably interrupt, or a regularly executed event loop to sense the condition.

8.30.3 Code security (Code Read Protection - CRP)

This feature of the LPC17xx allows user to enable different levels of security in the system so that access to the on-chip flash and use of the JTAG and ISP can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

There are three levels of the Code Read Protection.

CRP1 disables access to chip via the JTAG and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors can not be erased.

CRP2 disables access to chip via the JTAG and only allows full flash erase and update using a reduced set of the ISP commands.

Running an application with level CRP3 selected fully disables any access to chip via the JTAG pins and the ISP. This mode effectively disables ISP override using P2[10] pin, too. It is up to the user's application to provide (if needed) flash update mechanism using IAP calls or call reinvoke ISP command to enable flash update via UART0.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

8.30.4 APB interface

The APB peripherals are split into two separate APB buses in order to distribute the bus bandwidth and thereby reducing stalls caused by contention between the CPU and the GPDMA controller.

12.3 Internal oscillators

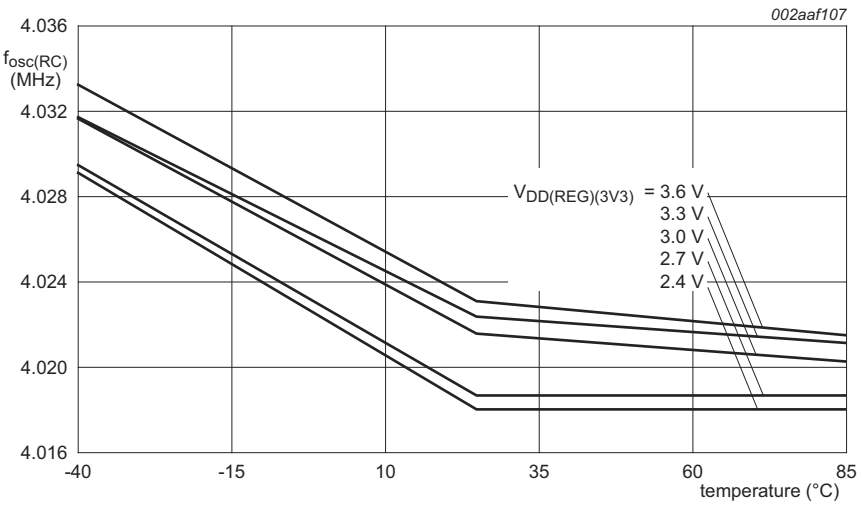
Table 12. Dynamic characteristic: internal oscillators

T_{amb} = −40 °C to +85 °C; 2.7 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V.[1]

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	-		3.96	4.02	4.04	MHz
$f_{i(RTC)}$	RTC input frequency	-		-	32.768	-	kHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.



Conditions: Frequency values are typical values. 4 MHz ± 1 % accuracy is guaranteed for 2.7 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V and T_{amb} = −40 °C to +85 °C. Variations between parts may cause the IRC to fall outside the 4 MHz ± 1 % accuracy specification for voltages below 2.7 V.

Fig 17. Internal RC oscillator frequency versus temperature

12.4 I/O pins

Table 13. Dynamic characteristic: I/O pins[1]

T_{amb} = −40 °C to +85 °C; $V_{DD(3V3)}$ over specified ranges.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	pin configured as output		3.0	-	5.0	ns
t_f	fall time	pin configured as output		2.5	-	5.0	ns

[1] Applies to standard I/O pins.

12.7 SSP interface

The maximum SSP speed is 33 Mbit/s in master mode or 8 Mbit/s in slave mode. In slave mode, the maximum SSP clock rate must be 1/12 of the SSP PCLK clock rate.

Table 16. Dynamic characteristics: SSP pins in SPI mode

C_L = 30 pF for all SSP pins; T_{amb} = −40 °C to 85 °C; $V_{DD(3V3)}$ = 3.3 V to 3.6 V; input slew = 1 ns; sampled at 10 % and 90 % of the signal level. Values guaranteed by design.

Symbol	Parameter	Conditions	Min	Max	Unit
SSP master					
t_{DS}	data set-up time	in SPI mode	16.1	-	ns
t_{DH}	data hold time	in SPI mode	0	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	-	2.5	ns
$t_{h(Q)}$	data output hold time	in SPI mode	0	-	ns
SSP slave					
t_{DS}	data set-up time	in SPI mode	16.1	-	ns
t_{DH}	data hold time	in SPI mode	0	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	-	$3*T_{cy(PCLK)} + 2.5$	ns
$t_{h(Q)}$	data output hold time	in SPI mode	0	-	ns

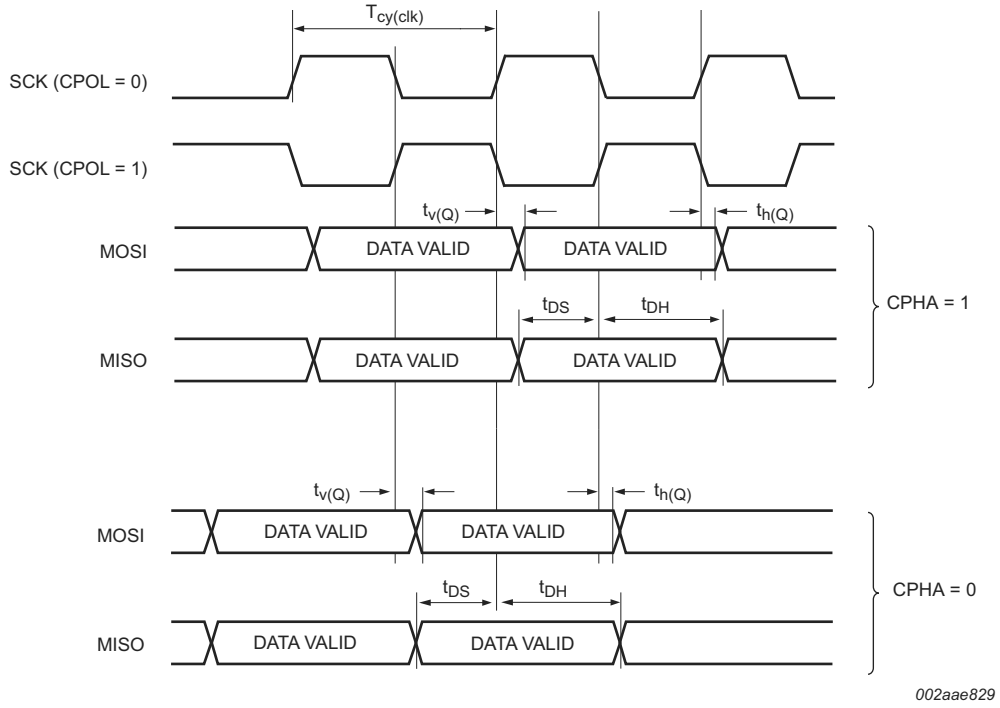


Fig 21. SSP master timing in SPI mode

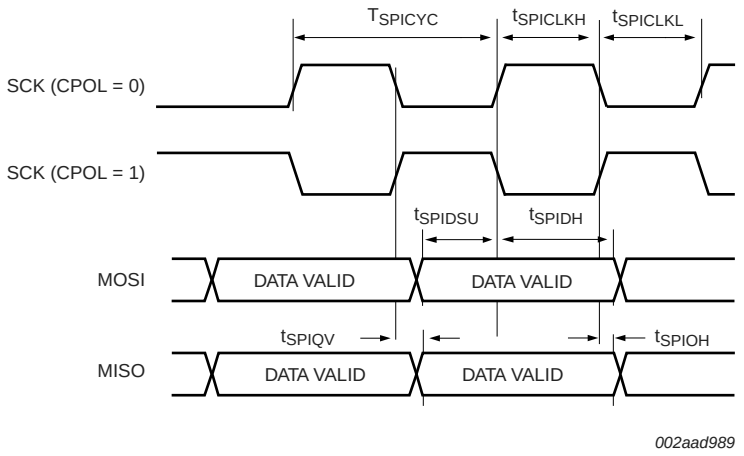


Fig 27. SPI slave timing (CPHA = 0)

13. ADC electrical characteristics

Table 19. ADC characteristics (full resolution)

V_{DDA} = 2.5 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified; ADC frequency 13 MHz; 12-bit resolution.[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IA}	analog input voltage			0	-	V_{DDA}	V
C_{ia}	analog input capacitance			-	-	15	pF
E_D	differential linearity error		[2][3]	-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity		[4]	-	-	±3	LSB
E_O	offset error		[5][6]	-	-	±2	LSB
E_G	gain error		[7]	-	-	0.5	%
E_T	absolute error		[8]	-	-	4	LSB
R_{vsi}	voltage source interface resistance		[9]	-	-	7.5	kΩ
$f_{clk(ADC)}$	ADC clock frequency			-	-	13	MHz
$f_{c(ADC)}$	ADC conversion frequency		[10]	-	-	200	kHz

[1] V_{DDA} and VREFP should be tied to $V_{DD(3V3)}$ if the ADC and DAC are not used.

[2] The ADC is monotonic, there are no missing codes.

[3] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 28.

[4] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 28.

[5] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 28.

[6] ADCOFFS value (bits 7:4) = 2 in the ADTRM register. See *LPC17xx user manual UM10360*.

[7] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 28.

[8] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 28.

[9] See Figure 29.

[10] The conversion frequency corresponds to the number of samples per second.

15.6 ElectroMagnetic Compatibility (EMC)

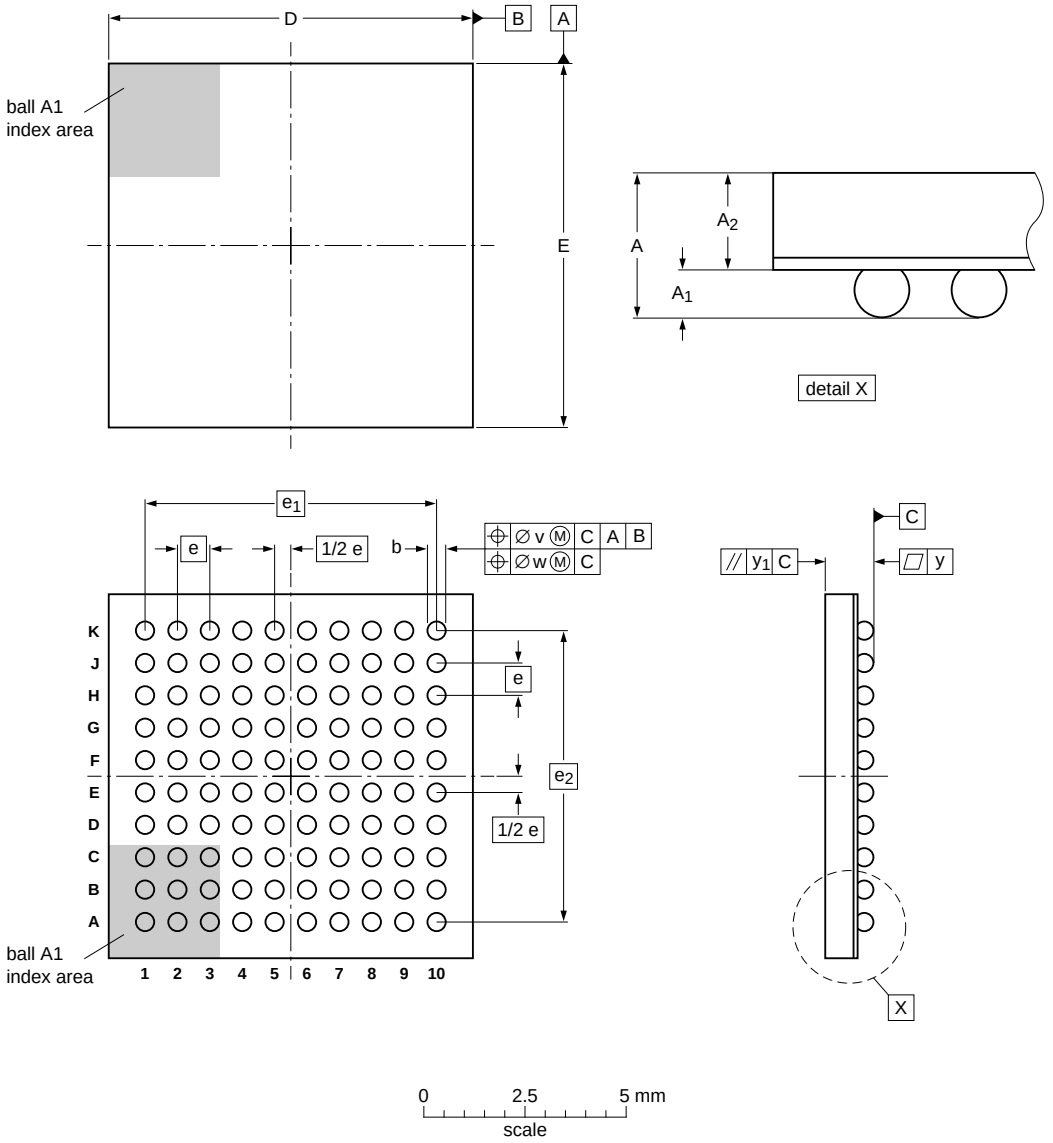
Radiated emission measurements according to the IEC61967-2 standard using the TEM-cell method are shown for part LPC1768.

Table 25. ElectroMagnetic Compatibility (EMC) for part LPC1768 (TEM-cell method)
V_{DD} = 3.3 V; T_{amb} = 25 °C.

Parameter	Frequency band	System clock =					Unit
		12 MHz	24 MHz	48 MHz	72 MHz	100 MHz	
Input clock: IRC (4 MHz)							
maximum peak level	150 kHz to 30 MHz	−7	−6	−4	−7	−7	dBμV
	30 MHz to 150 MHz	+1	+5	+11	+16	+9	dBμV
	150 MHz to 1 GHz	−2	+4	+11	+12	+19	dBμV
IEC level[1]	-	O	O	N	M	L	-
Input clock: crystal oscillator (12 MHz)							
maximum peak level	150 kHz to 30 MHz	−5	−4	−4	−7	−8	dBμV
	30 MHz to 150 MHz	−1	+5	+10	+15	+7	dBμV
	150 MHz to 1 GHz	−1	+6	+11	+10	+16	dBμV
IEC level[1]	-	O	O	N	M	M	-

[1] IEC levels refer to Appendix D in the IEC61967-2 Specification.

TFBGA100: plastic thin fine-pitch ball grid array package; 100 balls; body 9 x 9 x 0.7 mm **SOT926-1**



DIMENSIONS (mm are the original dimensions)

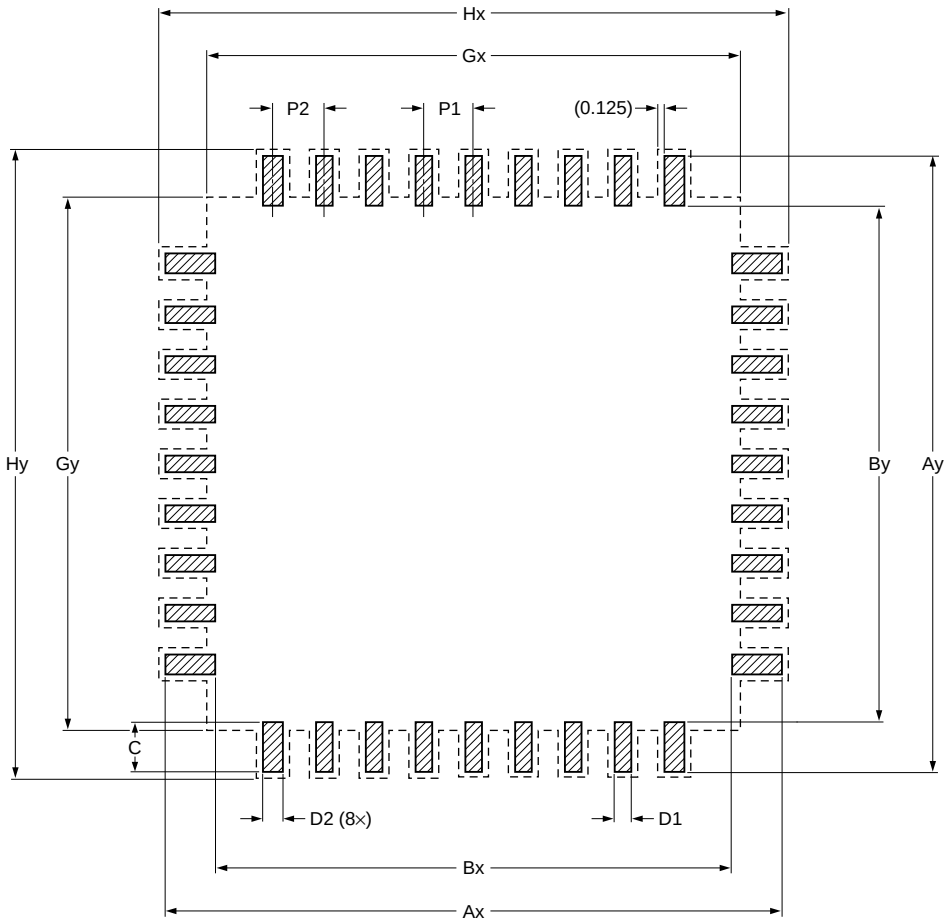
UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.2	0.4 0.3	0.8 0.65	0.5 0.4	9.1 8.9	9.1 8.9	0.8	7.2	7.2	0.15	0.05	0.08	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT926-1	- - -	- - -	- - -			~~05-12-09~~ 05-12-22

Fig 41. Package outline SOT926-1 (TFBGA100)

17. Soldering

Footprint information for reflow soldering of LQFP100 package **SOT407-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

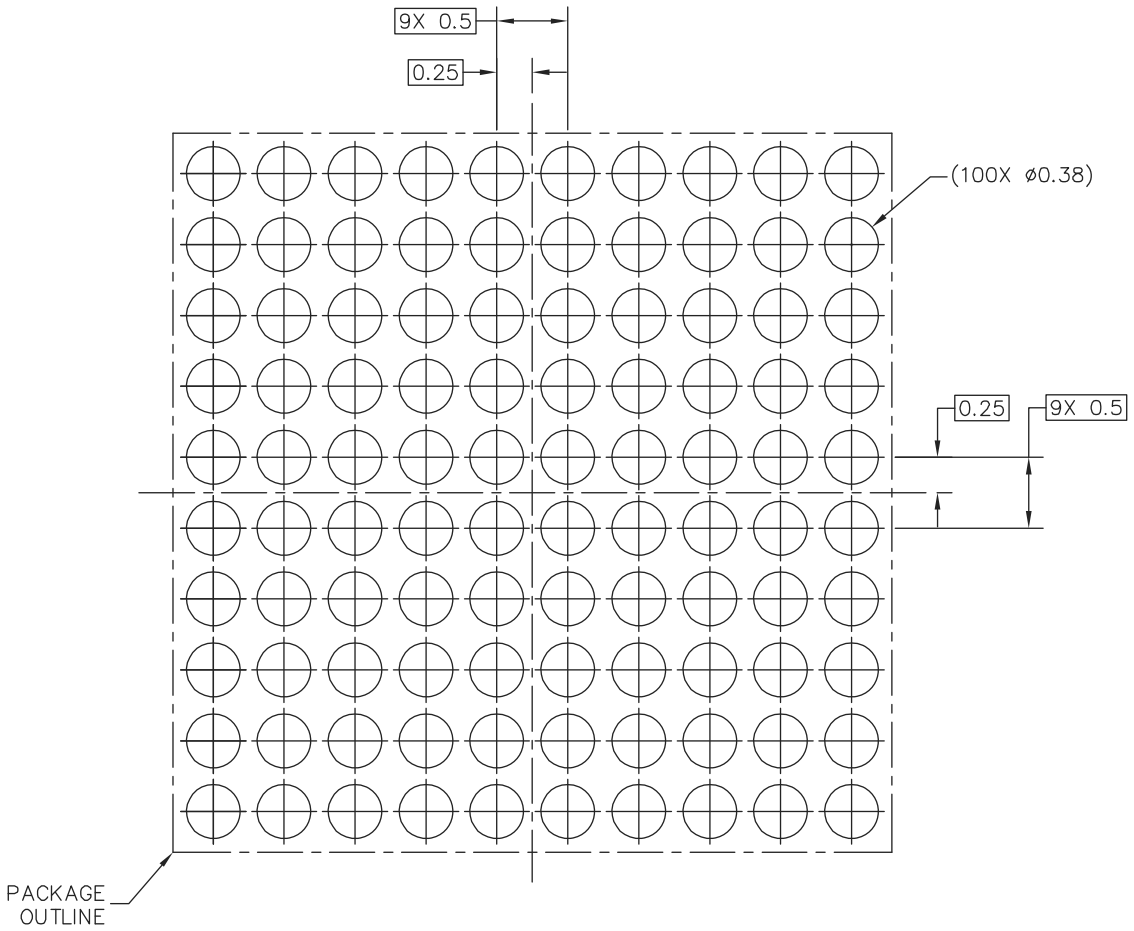
occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	17.300	17.300	14.300	14.300	1.500	0.280	0.400	14.500	14.500	17.550	17.550

sot407-1

Fig 43. Reflow soldering for the LQFP100 package



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

DATE: 06 MAR 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: SOT1450–2	REVISION: 0	

Fig 45. Reflow soldering of the WLCSP100 package (part 1)

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Date of release: 4 May 2018
Document identifier: LPC1769_68_67_66_65_64_63