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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I ² C, IrDA, Microwire, SPI, SSI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, Motor Control PWM, POR, PWM, WDT
Number of I/O	70
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1763fbd100k

- ◆ Two/one 16 kB SRAM blocks with separate access paths for higher throughput. These SRAM blocks may be used for Ethernet, USB, and DMA memory, as well as for general purpose CPU instruction and data storage.
- Eight channel General Purpose DMA controller (GPDMA) on the AHB multilayer matrix that can be used with SSP, I²S-bus, UART, Analog-to-Digital and Digital-to-Analog converter peripherals, timer match signals, and for memory-to-memory transfers.
- Multilayer AHB matrix interconnect provides a separate bus for each AHB master. AHB masters include the CPU, General Purpose DMA controller, Ethernet MAC, and the USB interface. This interconnect provides communication with no arbitration delays.
- Split APB bus allows high throughput with few stalls between the CPU and DMA.
- Serial interfaces:
 - ◆ Ethernet MAC with RMII interface and dedicated DMA controller. (Not available on all parts, see [Table 2](#).)
 - ◆ USB 2.0 full-speed device/Host/OTG controller with dedicated DMA controller and on-chip PHY for device, Host, and OTG functions. (Not available on all parts, see [Table 2](#).)
 - ◆ Four UARTs with fractional baud rate generation, internal FIFO, and DMA support. One UART has modem control I/O and RS-485/EIA-485 support, and one UART has IrDA support.
 - ◆ CAN 2.0B controller with two channels. (Not available on all parts, see [Table 2](#).)
 - ◆ SPI controller with synchronous, serial, full duplex communication and programmable data length.
 - ◆ Two SSP controllers with FIFO and multi-protocol capabilities. The SSP interfaces can be used with the GPDMA controller.
 - ◆ Three enhanced I²C bus interfaces, one with an open-drain output supporting full I²C specification and Fast mode plus with data rates of 1 Mbit/s, two with standard port pins. Enhancements include multiple address recognition and monitor mode.
 - ◆ I²S (Inter-IC Sound) interface for digital audio input or output, with fractional rate control. The I²S-bus interface can be used with the GPDMA. The I²S-bus interface supports 3-wire and 4-wire data transmit and receive as well as master clock input/output. (Not available on all parts, see [Table 2](#).)
- Other peripherals:
 - ◆ 70 (100 pin package) General Purpose I/O (GPIO) pins with configurable pull-up/down resistors. All GPIOs support a new, configurable open-drain operating mode. The GPIO block is accessed through the AHB multilayer bus for fast access and located in memory such that it supports Cortex-M3 bit banding and use by the General Purpose DMA Controller.
 - ◆ 12-bit Analog-to-Digital Converter (ADC) with input multiplexing among eight pins, conversion rates up to 200 kHz, and multiple result registers. The 12-bit ADC can be used with the GPDMA controller.
 - ◆ 10-bit Digital-to-Analog Converter (DAC) with dedicated conversion timer and DMA support. (Not available on all parts, see [Table 2](#))
 - ◆ Four general purpose timers/counters, with a total of eight capture inputs and ten compare outputs. Each timer block has an external count input. Specific timer events can be selected to generate DMA requests.
 - ◆ One motor control PWM with support for three-phase motor control.

- ◆ Quadrature encoder interface that can monitor one external quadrature encoder.
- ◆ One standard PWM/timer block with external count input.
- ◆ RTC with a separate power domain and dedicated RTC oscillator. The RTC block includes 20 bytes of battery-powered backup registers.
- ◆ WatchDog Timer (WDT). The WDT can be clocked from the internal RC oscillator, the RTC oscillator, or the APB clock.
- ◆ Arm Cortex-M3 system tick timer, including an external clock input option.
- ◆ Repetitive interrupt timer provides programmable and repeating timed interrupts.
- ◆ Each peripheral has its own clock divider for further power savings.
- Standard JTAG debug interface for compatibility with existing tools. Serial Wire Debug and Serial Wire Trace Port options. Boundary Scan Description Language (BSDL) is not available for this device.
- Emulation trace module enables non-intrusive, high-speed real-time tracing of instruction execution.
- Integrated PMU (Power Management Unit) automatically adjusts internal regulators to minimize power consumption during Sleep, Deep sleep, Power-down, and Deep power-down modes.
- Four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.
- Single 3.3 V power supply (2.4 V to 3.6 V).
- Four external interrupt inputs configurable as edge/level sensitive. All pins on Port 0 and Port 2 can be used as edge sensitive interrupt sources.
- Non-maskable Interrupt (NMI) input.
- Clock output function that can reflect the main oscillator clock, IRC clock, RTC clock, CPU clock, and the USB clock.
- The Wake-up Interrupt Controller (WIC) allows the CPU to automatically wake up from any priority interrupt that can occur while the clocks are stopped in deep sleep, Power-down, and Deep power-down modes.
- Processor wake-up from Power-down mode via any interrupt able to operate during Power-down mode (includes external interrupts, RTC interrupt, USB activity, Ethernet wake-up interrupt, CAN bus activity, Port 0/2 pin interrupt, and NMI).
- Brownout detect with separate threshold for interrupt and forced reset.
- Power-On Reset (POR).
- Crystal oscillator with an operating range of 1 MHz to 25 MHz.
- 4 MHz internal RC oscillator trimmed to 1 % accuracy that can optionally be used as a system clock.
- PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the main oscillator, the internal RC oscillator, or the RTC oscillator.
- USB PLL for added flexibility.
- Code Read Protection (CRP) with different security levels.
- Unique device serial number for identification purposes.
- Available as LQFP100 (14 mm × 14 mm × 1.4 mm), TFBGA100¹ (9 mm × 9 mm × 0.7 mm), and WLCSP100 (5.07 × 5.07 × 0.53 mm) package.

1. LPC1768/65 only.

3. Applications

- eMetering
- Lighting
- Industrial networking
- Alarm systems
- White goods
- Motor control

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC1769FBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1768FBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1768FET100	TFBGA100	plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC1768UK	WLCSP100	wafer level chip-scale package; 100 balls; 5.07 × 5.07 × 0.53 mm	-
LPC1767FBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1766FBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1765FBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1765FET100	TFBGA100	plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC1764FBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1763FBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1

4.1 Ordering options

Table 2. Ordering options

Type number	Device order part number	Flash (kB)	SRAM in kB				Ethernet	USB	CAN	I ² S	DAC	GPIO	Maximum CPU operating frequency (MHz)
			CPU	AHB SRAM0	AHB SRAM1	Total							
LPC1769FBD100	LPC1769FBD100,551	512	32	16	16	64	yes	Device/Host/OTG	2	yes	yes	70	120
LPC1768FBD100	LPC1768FBD100/CP32	512	32	16	16	64	yes	Device/Host/OTG	2	yes	yes	70	100
LPC1768FET100	LPC1768FET100Z	512	32	16	16	64	yes	Device/Host/OTG	2	yes	yes	70	100
LPC1768UK	LPC1768UKZ	512	32	16	16	64	yes	Device/Host/OTG	2	yes	yes	70	100
LPC1767FBD100	LPC1767FBD100,551	512	32	16	16	64	yes	no	no	yes	yes	70	100
LPC1766FBD100	LPC1766FBD100,551	256	32	16	16	64	yes	Device/Host/OTG	2	yes	yes	70	100
LPC1765FBD100	LPC1765FBD100/3271	256	32	16	16	64	no	Device/Host/OTG	2	yes	yes	70	100
LPC1765FET100	LPC1765FET100,551	256	32	16	16	64	no	Device/Host/OTG	2	yes	yes	70	100
LPC1764FBD100	LPC1764FBD100,551	128	16	16	-	32	yes	Device only	2	no	no	70	100
LPC1763FBD100	LPC1763FBD100K	256	32	16	16	64	no	no	no	yes	yes	70	100

8.9.1 Features

- Eight DMA channels. Each channel can support an unidirectional transfer.
- 16 DMA request lines.
- Single DMA and burst DMA request signals. Each peripheral connected to the DMA Controller can assert either a burst DMA request or a single DMA request. The DMA burst size is set by programming the DMA Controller.
- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral transfers are supported.
- Scatter or gather DMA is supported through the use of linked lists. This means that the source and destination areas do not have to occupy contiguous areas of memory.
- Hardware DMA channel priority.
- AHB slave DMA programming interface. The DMA Controller is programmed by writing to the DMA control registers over the AHB slave interface.
- One AHB bus master for transferring data. The interface transfers data when a DMA request goes active.
- 32-bit AHB master bus width.
- Incrementing or non-incrementing addressing for source and destination.
- Programmable DMA burst size. The DMA burst size can be programmed to more efficiently transfer data.
- Internal four-word FIFO per channel.
- Supports 8, 16, and 32-bit wide transactions.
- Big-endian and little-endian support. The DMA Controller defaults to little-endian mode on reset.
- An interrupt to the processor can be generated on a DMA completion or when a DMA error has occurred.
- Raw interrupt status. The DMA error and DMA count raw interrupt status can be read prior to masking.

8.10 Fast general purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back as well as the current state of the port pins.

LPC17xx use accelerated GPIO functions:

- GPIO registers are accessed through the AHB multilayer bus so that the fastest possible I/O timing can be achieved.
- Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
- All GPIO registers are byte and half-word addressable.
- Entire port value can be written in one instruction.
- Support for Cortex-M3 bit banding.
- Support for use with the GPDMA controller.

- Endpoint Maximum packet size selection (up to USB maximum specification) by software at run time.
- Supports SoftConnect and GoodLink features.
- While USB is in the Suspend mode, the part can enter one of the reduced power modes and wake up on USB activity.
- Supports DMA transfers with all on-chip SRAM blocks on all non-control endpoints.
- Allows dynamic switching between CPU-controlled slave and DMA modes.
- Double buffer implementation for Bulk and Isochronous endpoints.

8.12.2 USB host controller

The host controller enables full- and low-speed data exchange with USB devices attached to the bus. It consists of a register interface, a serial interface engine, and a DMA controller. The register interface complies with the OHCI specification.

8.12.2.1 Features

- OHCI compliant.
- One downstream port.
- Supports port power switching.

8.12.3 USB OTG controller

USB OTG is a supplement to the USB 2.0 specification that augments the capability of existing mobile devices and USB peripherals by adding host functionality for connection to USB peripherals.

The OTG Controller integrates the host controller, device controller, and a master-only I²C-bus interface to implement OTG dual-role device functionality. The dedicated I²C-bus interface controls an external OTG transceiver.

8.12.3.1 Features

- Fully compliant with *On-The-Go supplement to the USB 2.0 Specification, Revision 1.0a*.
- Hardware support for Host Negotiation Protocol (HNP).
- Includes a programmable timer required for HNP and Session Request Protocol (SRP).
- Supports any OTG transceiver compliant with the *OTG Transceiver Specification (CEA-2011), Rev. 1.0*.

8.13 CAN controller and acceptance filters

Remark: The CAN controllers are available on parts LPC1769/68/66/65/64. See [Table 2](#).

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real-time control with a very high level of security. Its domain of application ranges from high-speed networks to low cost multiplex wiring.

The CAN block is intended to support multiple CAN buses simultaneously, allowing the device to be used as a gateway, switch, or router among a number of CAN buses in industrial or automotive applications.

8.29.2 Main PLL (PLL0)

The PLL0 accepts an input clock frequency in the range of 32 kHz to 25 MHz. The input frequency is multiplied up to a high frequency, then divided down to provide the actual clock used by the CPU and/or the USB block.

The PLL0 input, in the range of 32 kHz to 25 MHz, may initially be divided down by a value 'N', which may be in the range of 1 to 256. This input division provides a wide range of output frequencies from the same input frequency.

Following the PLL0 input divider is the PLL0 multiplier. This can multiply the input divider output through the use of a Current Controlled Oscillator (CCO) by a value 'M', in the range of 1 through 32768. The resulting frequency must be in the range of 275 MHz to 550 MHz. The multiplier works by dividing the CCO output by the value of M, then using a phase-frequency detector to compare the divided CCO output to the multiplier input. The error value is used to adjust the CCO frequency.

The PLL0 is turned off and bypassed following a chip Reset and by entering Power-down mode. PLL0 is enabled by software only. The program must configure and activate the PLL0, wait for the PLL0 to lock, and then connect to the PLL0 as a clock source.

8.29.3 USB PLL (PLL1)

The LPC17xx contain a second, dedicated USB PLL1 to provide clocking for the USB interface.

The PLL1 receives its clock input from the main oscillator only and provides a fixed 48 MHz clock to the USB block only. The PLL1 is disabled and powered off on reset. If the PLL1 is left disabled, the USB clock will be supplied by the 48 MHz clock from the main PLL0.

The PLL1 accepts an input clock frequency in the range of 10 MHz to 25 MHz only. The input frequency is multiplied up the range of 48 MHz for the USB clock using a Current Controlled Oscillators (CCO). It is insured that the PLL1 output has a 50 % duty cycle.

8.29.4 RTC clock output

The LPC17xx feature a clock output function intended for synchronizing with external devices and for use during system development to allow checking the internal clocks CCLK, IRC clock, main crystal, RTC clock, and USB clock in the outside world. The RTC clock output allows tuning the RTC frequency without probing the pin, which would distort the results.

8.29.5 Wake-up timer

The LPC17xx begin operation at power-up and when awakened from Power-down mode by using the 4 MHz IRC oscillator as the clock source. This allows chip operation to resume quickly. If the main oscillator or the PLL is needed by the application, software will need to enable these features and wait for them to stabilize before they are used as a clock source.

When the main oscillator is initially activated, the wake-up timer allows software to ensure that the main oscillator is fully functional before the processor uses it as a clock source and starts to execute instructions. This is important at power on, all types of Reset, and

whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the wake-up timer.

The Wake-up Timer monitors the crystal oscillator to check whether it is safe to begin code execution. When power is applied to the chip, or when some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient amplitude to drive the clock logic. The amount of time depends on many factors, including the rate of $V_{DD(3V3)}$ ramp (in the case of power on), the type of crystal and its electrical characteristics (if a quartz crystal is used), as well as any other external circuitry (e.g., capacitors), and the characteristics of the oscillator itself under the existing ambient conditions.

8.29.6 Power control

The LPC17xx support a variety of power control features. There are four special modes of processor power reduction: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, Peripheral Power Control allows shutting down the clocks to individual on-chip peripherals, allowing fine tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Each of the peripherals has its own clock divider which provides even better power control.

Integrated PMU (Power Management Unit) automatically adjust internal regulators to minimize power consumption during Sleep, Deep sleep, Power-down, and Deep power-down modes.

The LPC17xx also implement a separate power domain to allow turning off power to the bulk of the device while maintaining operation of the RTC and a small set of registers for storing data during any of the power-down modes.

8.29.6.1 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the Arm core.

In Sleep mode, execution of instructions is suspended until either a Reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

8.29.6.2 Deep-sleep mode

In Deep-sleep mode, the oscillator is shut down and the chip receives no internal clocks. The processor state and registers, peripheral registers, and internal SRAM values are preserved throughout Deep-sleep mode and the logic levels of chip pins remain static. The output of the IRC is disabled but the IRC is not powered down for a fast wake-up later. The RTC oscillator is not stopped because the RTC interrupts may be used as the wake-up source. The PLL is automatically turned off and disconnected. The CCLK and USB clock dividers automatically get reset to zero.

8.29.8 Power domains

The LPC17xx provide two independent power domains that allow the bulk of the device to have power removed while maintaining operation of the RTC and the backup Registers.

On the LPC17xx, I/O pads are powered by the 3.3 V ($V_{DD(3V3)}$) pins, while the $V_{DD(REG)(3V3)}$ pin powers the on-chip voltage regulator which in turn provides power to the CPU and most of the peripherals.

Depending on the LPC17xx application, a design can use two power options to manage power consumption.

The first option assumes that power consumption is not a concern and the design ties the $V_{DD(3V3)}$ and $V_{DD(REG)(3V3)}$ pins together. This approach requires only one 3.3 V power supply for both pads, the CPU, and peripherals. While this solution is simple, it does not support powering down the I/O pad ring “on the fly” while keeping the CPU and peripherals alive.

The second option uses two power supplies; a 3.3 V supply for the I/O pads ($V_{DD(3V3)}$) and a dedicated 3.3 V supply for the CPU ($V_{DD(REG)(3V3)}$). Having the on-chip voltage regulator powered independently from the I/O pad ring enables shutting down of the I/O pad power supply “on the fly”, while the CPU and peripherals stay active.

The VBAT pin supplies power only to the RTC domain. The RTC requires a minimum of power to operate, which can be supplied by an external battery. The device core power ($V_{DD(REG)(3V3)}$) is used to operate the RTC whenever $V_{DD(REG)(3V3)}$ is present. Therefore, there is no power drain from the RTC battery when $V_{DD(REG)(3V3)}$ is available.

8.30.5 AHB multilayer matrix

The LPC17xx use an AHB multilayer matrix. This matrix connects the instruction (I-code) and data (D-code) CPU buses of the Arm Cortex-M3 to the flash memory, the main (32 kB) static RAM, and the Boot ROM. The GPDMA can also access all of these memories. The peripheral DMA controllers, Ethernet, and USB can access all SRAM blocks. Additionally, the matrix connects the CPU system bus and all of the DMA controllers to the various peripheral functions.

8.30.6 External interrupt inputs

The LPC17xx include up to 46 edge sensitive interrupt inputs combined with up to four level sensitive external interrupt inputs as selectable pin functions. The external interrupt inputs can optionally be used to wake up the processor from Power-down mode.

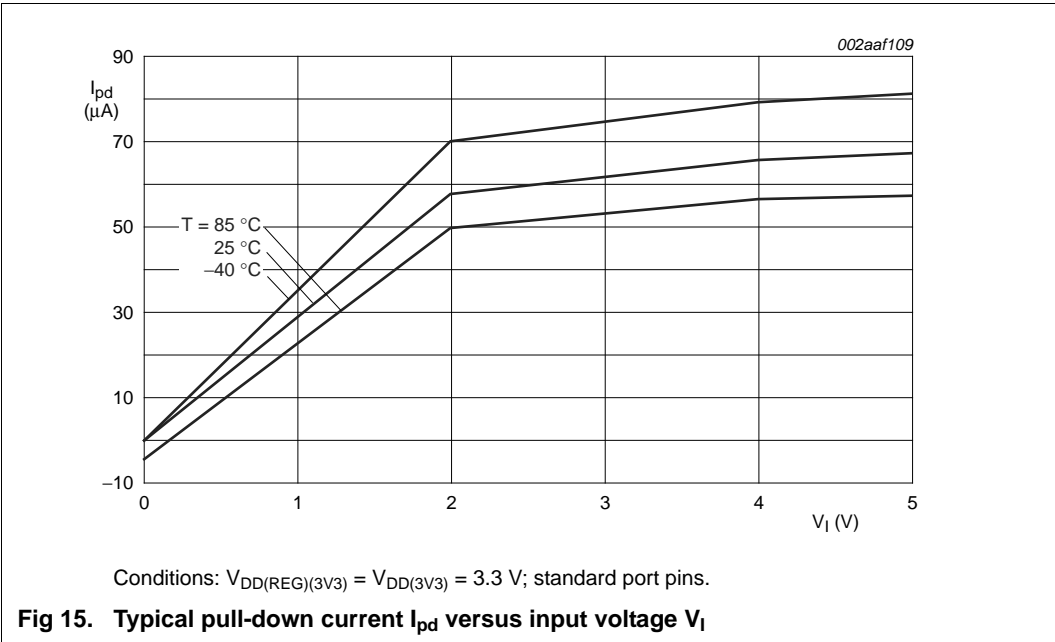
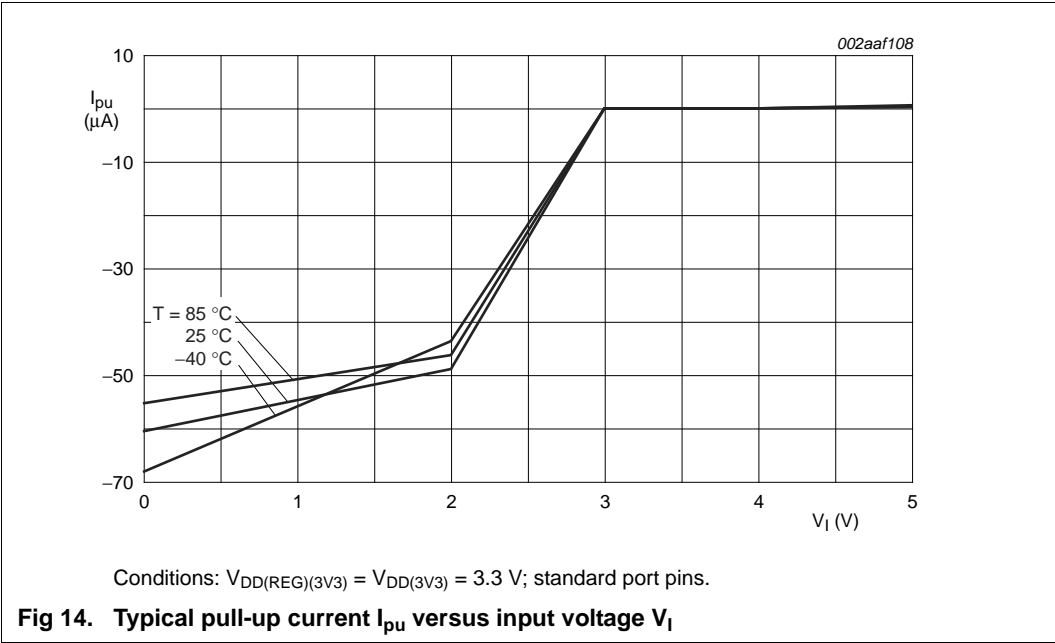
8.30.7 Memory mapping control

The Cortex-M3 incorporates a mechanism that allows remapping the interrupt vector table to alternate locations in the memory map. This is controlled via the Vector Table Offset Register contained in the NVIC.

The vector table may be located anywhere within the bottom 1 GB of Cortex-M3 address space. The vector table must be located on a 128 word (512 byte) boundary because the NVIC on the LPC17xx is configured for 128 total interrupts.

8.31 Emulation and debugging

Debug and trace functions are integrated into the Arm Cortex-M3. Serial wire debug and trace functions are supported in addition to a standard JTAG debug and parallel trace functions. The Arm Cortex-M3 is configured to support up to eight breakpoints and four watch points.



12. Dynamic characteristics

12.1 Flash memory

Table 10. Flash characteristics

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance		[1]	10000	100000	-	cycles
t_{ret}	retention time	powered		10	-	-	years
		unpowered		20	-	-	years
t_{er}	erase time	sector or multiple consecutive sectors		95	100	105	ms
t_{prog}	programming time		[2]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 256 bytes from RAM to the flash. Data must be written to the flash in blocks of 256 bytes.

12.2 External clock

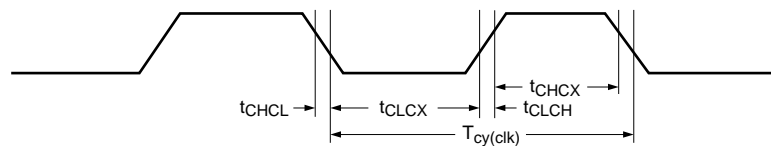
Table 11. Dynamic characteristic: external clock

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$; $V_{DD(3V3)}$ over specified ranges.[1]

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
f_{osc}	oscillator frequency			1	-	25	MHz
$T_{cy(clk)}$	clock cycle time			40	-	1000	ns
t_{CHCX}	clock HIGH time			$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time			$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time			-	-	5	ns
t_{CHCL}	clock fall time			-	-	5	ns

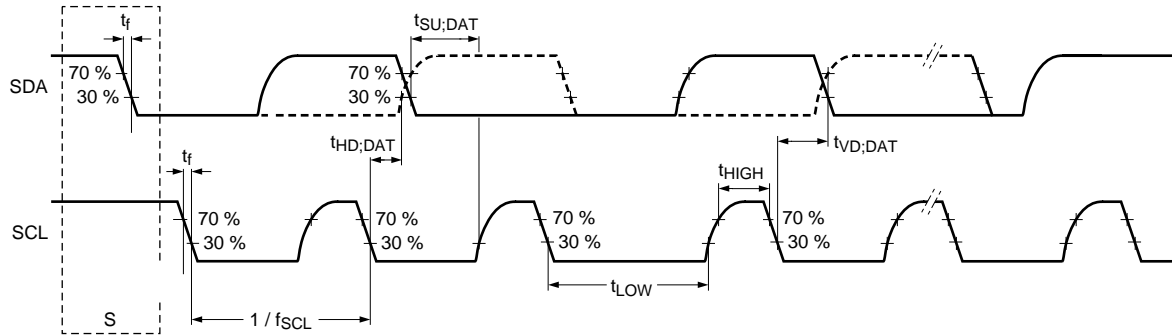
[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.



002aaa907

Fig 16. External clock timing (with an amplitude of at least $V_{i(RMS)} = 200\text{ mV}$)



002aaf425

Fig 18. I²C-bus pins clock timing

12.6 I²S-bus interface

Remark: The I²S-bus interface is available on parts LPC1769/68/67/66/65/63. See [Table 2](#).

Table 15. Dynamic characteristics: I²S-bus interface pins

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
common to input and output							
t _r	rise time		[1]	-	-	35	ns
t _f	fall time		[1]	-	-	35	ns
t _{WH}	pulse width HIGH	on pins I2STX_CLK and I2SRX_CLK	[1]	0.495 × T _{cy(clk)}	-	-	-
t _{WL}	pulse width LOW	on pins I2STX_CLK and I2SRX_CLK	[1]	-	-	0.505 × T _{cy(clk)}	ns
output							
t _{v(Q)}	data output valid time	on pin I2STX_SDA	[1]	-	-	30	ns
		on pin I2STX_WS	[1]	-	-	30	ns
input							
t _{su(D)}	data input set-up time	on pin I2SRX_SDA	[1]	3.5	-	-	ns
t _{h(D)}	data input hold time	on pin I2SRX_SDA	[1]	4.0	-	-	ns

[1] CCLK = 20 MHz; peripheral clock to the I²S-bus interface PCLK = $\frac{CCLK}{4}$; I²S clock cycle time $T_{cy(clk)} = 1600\text{ ns}$, corresponds to the SCK signal in the I²S-bus specification.

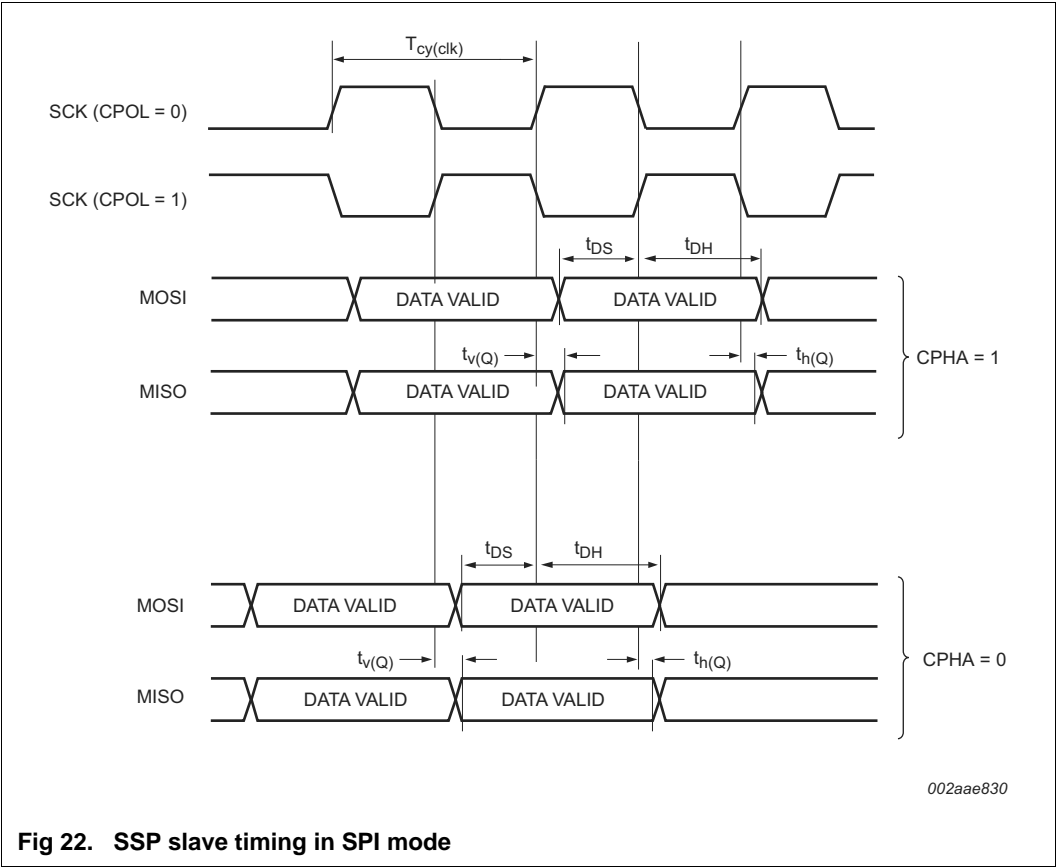


Fig 22. SSP slave timing in SPI mode

12.8 USB interface

Remark: The USB controller is available as a device/Host/OTG controller on parts LPC1769/68/66/65 and as device-only controller on part LPC1764.

Table 17. Dynamic characteristics: USB pins (full-speed)

$C_L = 50 \text{ pF}$; $R_{pu} = 1.5 \text{ k}\Omega$ on D+ to $V_{DD(3V3)}$; $3.0 \text{ V} \leq V_{DD(3V3)} \leq 3.6 \text{ V}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	10 % to 90 %	8.5	-	13.8	ns
t_f	fall time	10 % to 90 %	7.7	-	13.7	ns
t_{FRFM}	differential rise and fall time matching	t_r / t_f	-	-	109	%
V_{CRS}	output signal crossover voltage		1.3	-	2.0	V
t_{FEOPT}	source SE0 interval of EOP	see Figure 23	160	-	175	ns
t_{FDEOP}	source jitter for differential transition to SE0 transition	see Figure 23	-2	-	+5	ns
t_{JR1}	receiver jitter to next transition		-18.5	-	+18.5	ns
t_{JR2}	receiver jitter for paired transitions	10 % to 90 %	-9	-	+9	ns
t_{EOPR1}	EOP width at receiver	must reject as EOP; see Figure 23	[1] 40	-	-	ns
t_{EOPR2}	EOP width at receiver	must accept as EOP; see Figure 23	[1] 82	-	-	ns

[1] Characterized but not implemented as production test. Guaranteed by design.

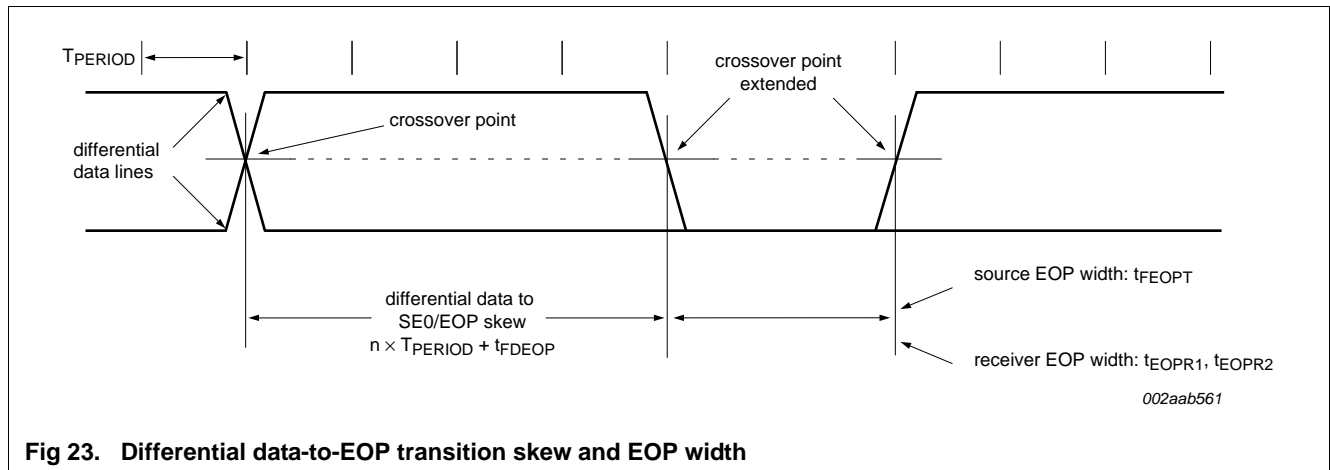
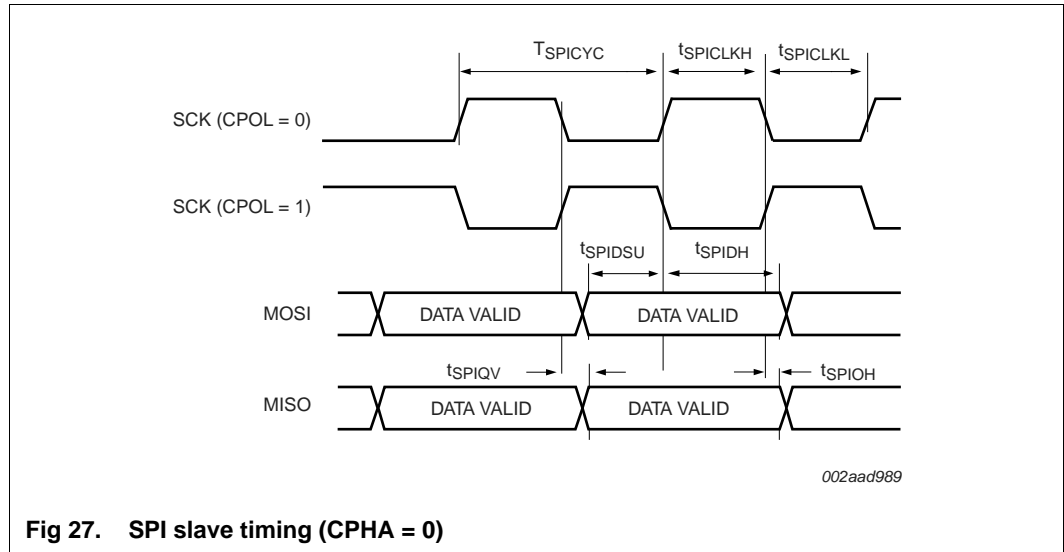


Fig 23. Differential data-to-EOP transition skew and EOP width



13. ADC electrical characteristics

Table 19. ADC characteristics (full resolution)

$V_{DDA} = 2.5\text{ V to }3.6\text{ V}$; $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ unless otherwise specified; ADC frequency 13 MHz; 12-bit resolution.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IA}	analog input voltage		0	-	V_{DDA}	V
C_{ia}	analog input capacitance		-	-	15	pF
E_D	differential linearity error	[2][3]	-	-	± 1	LSB
$E_{L(adj)}$	integral non-linearity	[4]	-	-	± 3	LSB
E_O	offset error	[5][6]	-	-	± 2	LSB
E_G	gain error	[7]	-	-	0.5	%
E_T	absolute error	[8]	-	-	4	LSB
R_{vsi}	voltage source interface resistance	[9]	-	-	7.5	k Ω
$f_{clk(ADC)}$	ADC clock frequency		-	-	13	MHz
$f_c(ADC)$	ADC conversion frequency	[10]	-	-	200	kHz

- [1] V_{DDA} and VREFP should be tied to $V_{DD(3V3)}$ if the ADC and DAC are not used.
- [2] The ADC is monotonic, there are no missing codes.
- [3] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 28.
- [4] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 28.
- [5] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 28.
- [6] ADCOFFS value (bits 7:4) = 2 in the ADTRM register. See LPC17xx user manual UM10360.
- [7] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 28.
- [8] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 28.
- [9] See Figure 29.
- [10] The conversion frequency corresponds to the number of samples per second.

15. Application information

15.1 Suggested USB interface solutions

Remark: The USB controller is available as a device/Host/OTG controller on parts LPC1769/68/66/65 and as device-only controller on part LPC1764.

If the LPC1769/68/67/66/65/64/63 V_{DD} is always greater than 0 V while $V_{BUS} = 5$ V, the V_{BUS} pin can be connected directly to the V_{BUS} pin on the USB connector.

This applies to bus powered devices where the USB cable supplies the system power. For systems where V_{DD} can be 0 V and V_{BUS} is directly applied to the V_{BUS} pin, precautions must be taken to reduce the voltage to below 3.6 V.

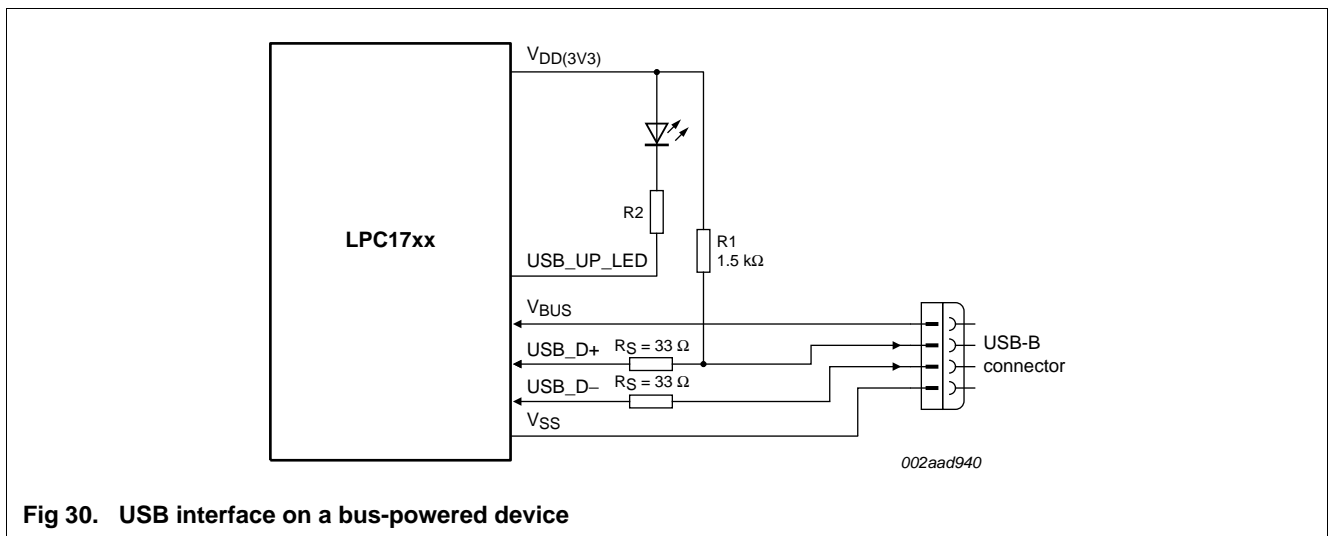


Fig 30. USB interface on a bus-powered device

The maximum allowable voltage on the V_{BUS} pin is 3.6 V. One method is to use a voltage divider to connect the V_{BUS} pin to the V_{BUS} on the USB connector.

The voltage divider ratio should be such that the V_{BUS} pin will be greater than $0.7V_{DD}$ to indicate a logic HIGH while below the 3.6 V allowable maximum voltage.

Use the following operating conditions:

$$V_{BUS_{max}} = 5.25 \text{ V}$$

$$V_{DD} = 3.6 \text{ V}$$

The voltage divider would need to provide a reduction of $3.6 \text{ V}/5.25 \text{ V}$ or $\sim 0.686 \text{ V}$.

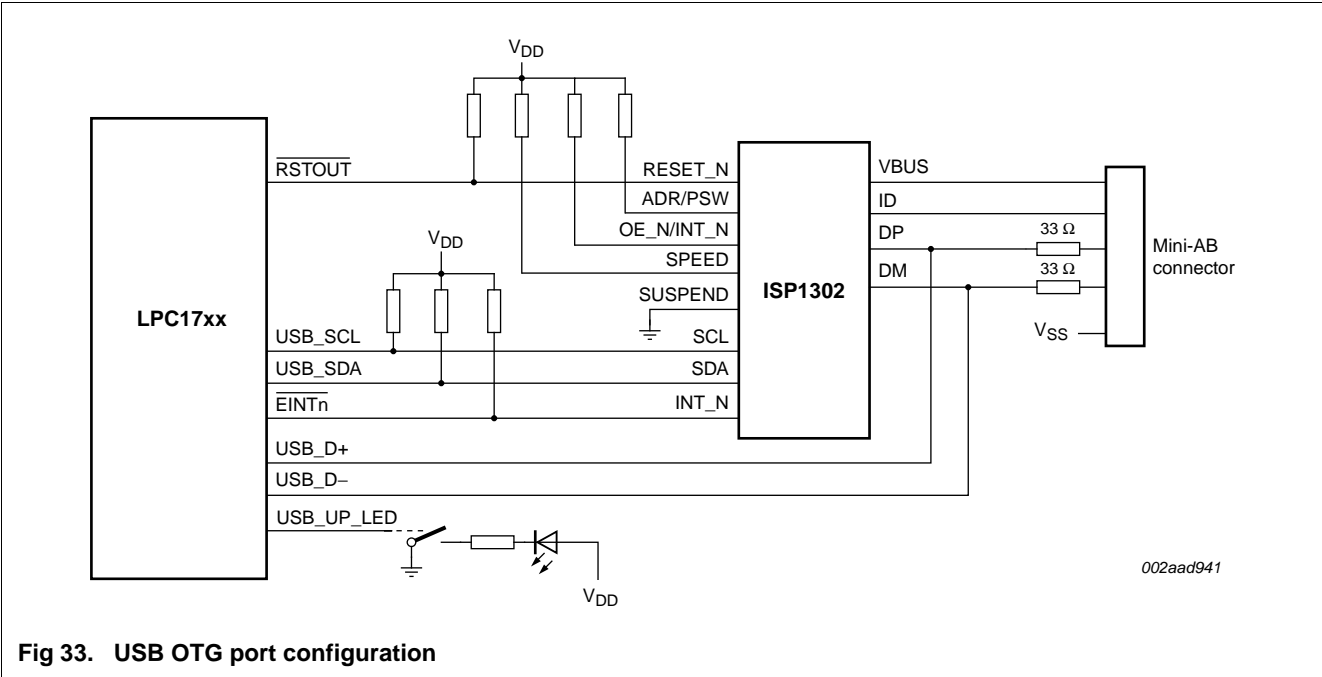


Fig 33. USB OTG port configuration

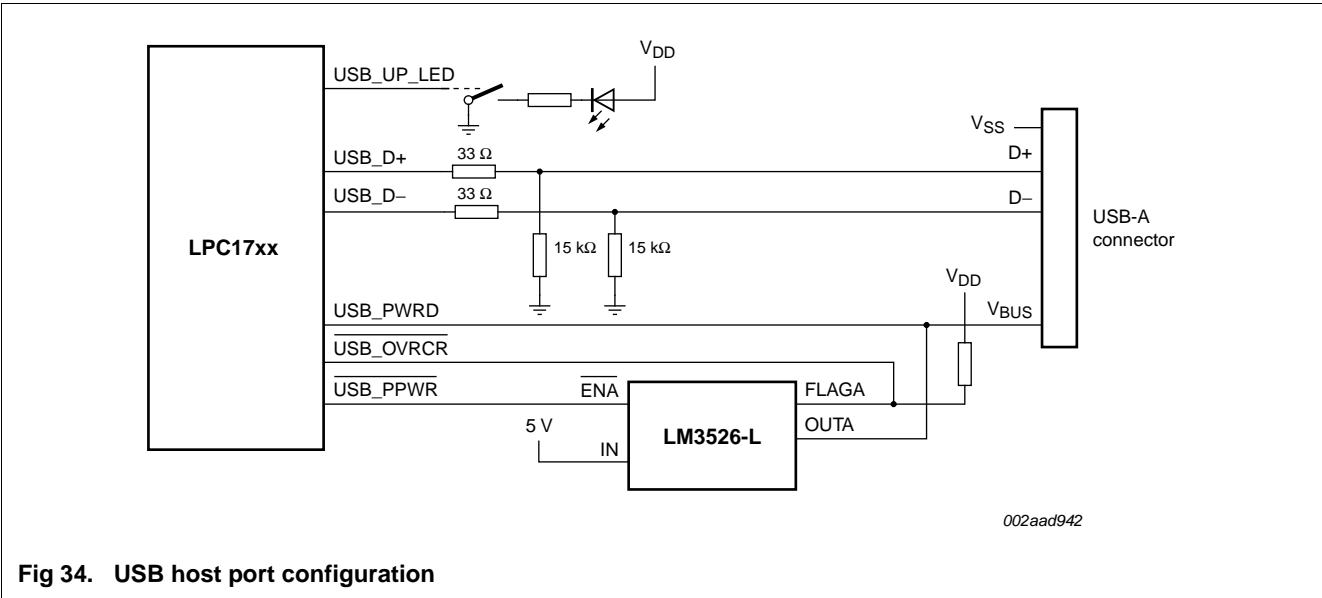


Fig 34. USB host port configuration

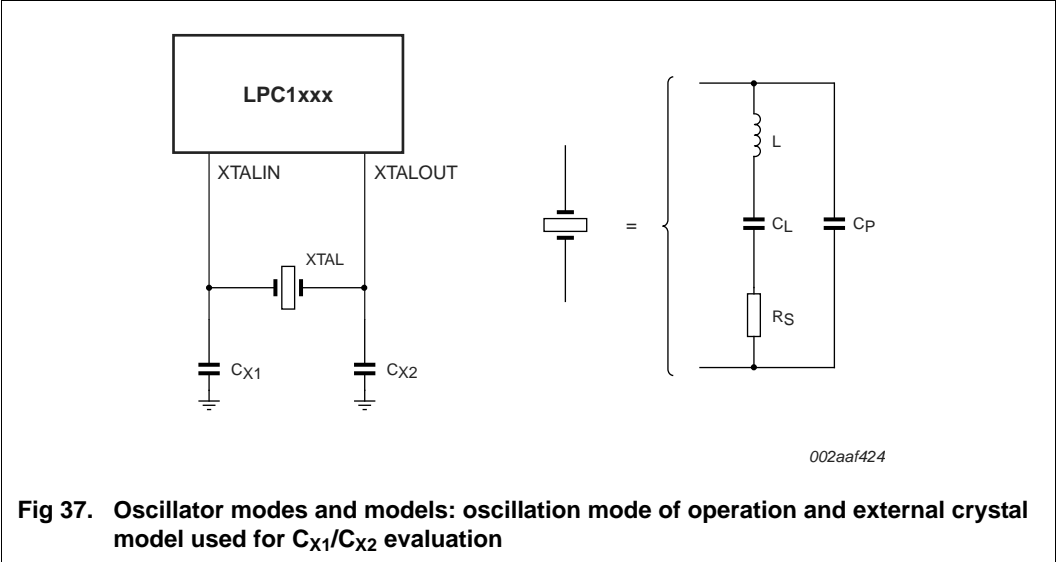


Table 23. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters): low frequency mode

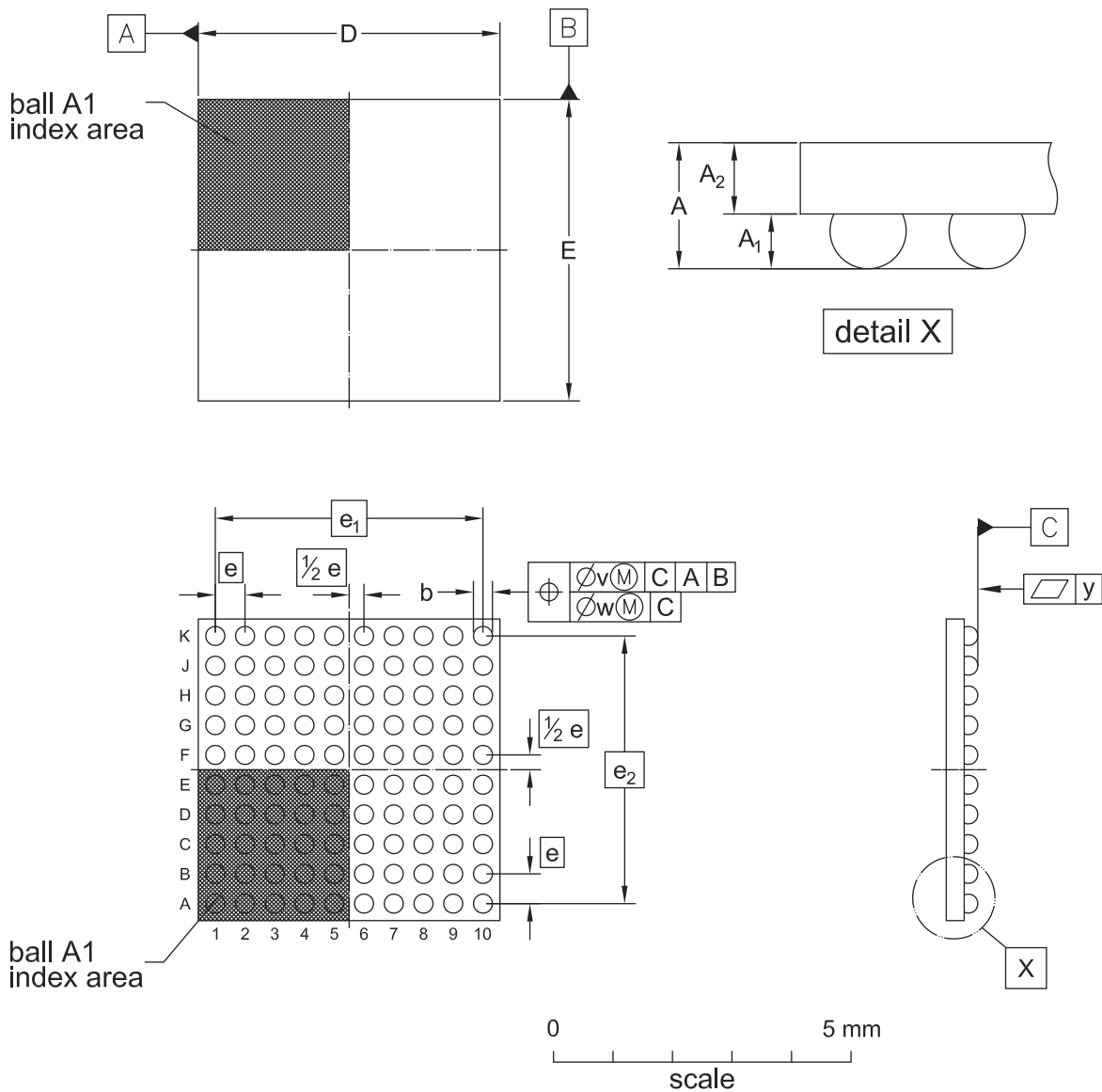
Fundamental oscillation frequency F_{Osc}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}/C_{X2}
1 MHz to 5 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 300 Ω	39 pF, 39 pF
	30 pF	< 300 Ω	57 pF, 57 pF
5 MHz to 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz to 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz to 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

Table 24. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters): high frequency mode

Fundamental oscillation frequency F_{Osc}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz to 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz to 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

15.3 XTAL and RTCX Printed Circuit Board (PCB) layout guidelines

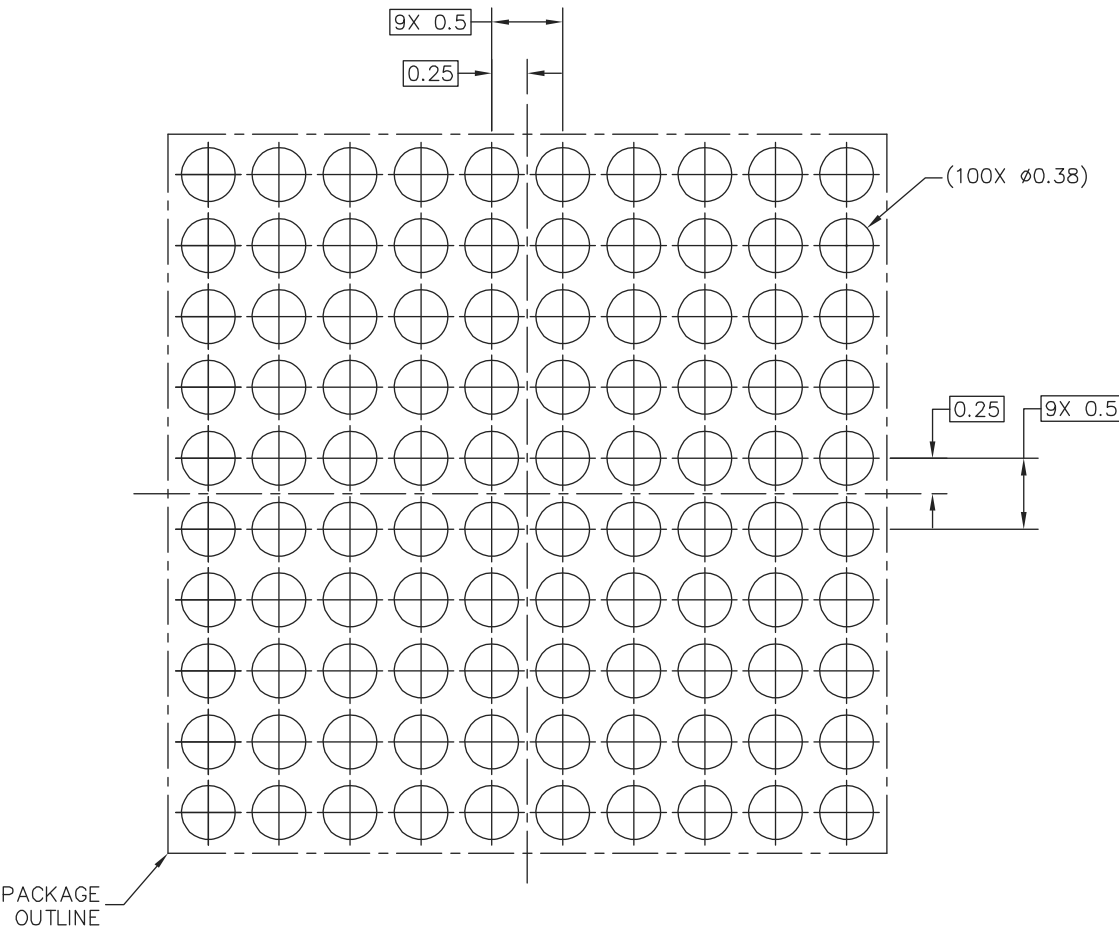
The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{X1} , C_{X2} , and C_{X3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plain. Loops must be made as small as possible in



DIMENSIONS (mm are the original dimensions)

UNIT		A	A ₁	A ₂	b	D	E	e	e ₁	e ₂	v	w	y
mm	MAX	0.57	0.26	0.325	0.35	5.10	5.10						
	NOM	0.53	0.23	0.300	0.32	5.07	5.07	0.5	4.5	4.5	0.15	0.05	0.03
	MIN	0.49	0.20	0.275	0.29	5.04	5.04						

Fig 42. Package outline SOT1450-2 LPC1768UK (WLCSP100)



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

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MECHANICAL OUTLINE	STANDARD:	DRAWING NUMBER:	REVISION:		
PRINT VERSION NOT TO SCALE	NON JEDEC	SOT1450-2	0		

Fig 45. Reflow soldering of the WLCSP100 package (part 1)