Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, I²C, IrDA, Microwire, SPI, SSI, SSP, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT
Number of I/O	70
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1765fbd100-551

5. Marking

The LPC176x devices typically have the following top-side marking:

LPC176xxxx

xxxxxxx

xxYYWWR[x]

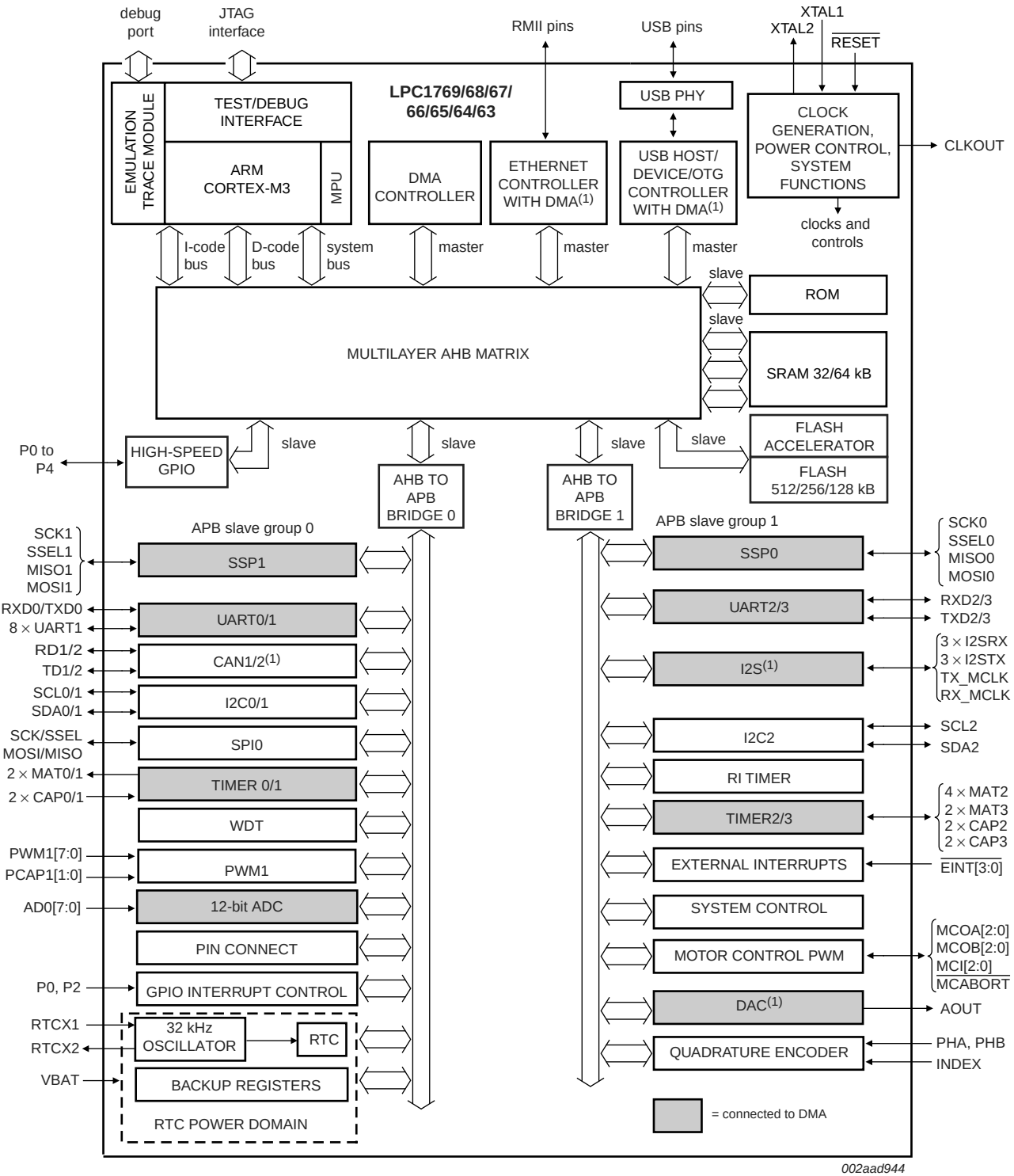
The last/second to last letter in the third line (field ‘R’) will identify the device revision. This data sheet covers the following revisions of the LPC176x:

Table 3. Device revision table

Revision identifier (R)	Revision description
‘-’	Initial device revision
‘A’	Second device revision
‘B’	Third device revision

Field ‘YY’ states the year the device was manufactured. Field ‘WW’ states the week the device was manufactured during that year.

6. Block diagram



(1) Not available on all parts. See Table 2.

Fig 1. Block diagram

Table 5. Pin description *…continued*

Symbol	Pin/ball				Type	Description
	LQFP100	TFBGA100	WLCSP100			
P0[23]/AD0[0]/ I2SRX_CLK/ CAP3[0]	9	E5	D5	[2]	I/O	**P0[23] —** General purpose digital input/output pin.
					I	**AD0[0] —** A/D converter 0, input 0.
					I/O	**I2SRX_CLK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*. (LPC1769/68/67/66/65/63 only).
					I	**CAP3[0] —** Capture input for Timer 3, channel 0.
P0[24]/AD0[1]/ I2SRX_WS/ CAP3[1]	8	D1	B4	[2]	I/O	**P0[24] —** General purpose digital input/output pin.
					I	**AD0[1] —** A/D converter 0, input 1.
					I/O	**I2SRX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*. (LPC1769/68/67/66/65/63 only).
					I	**CAP3[1] —** Capture input for Timer 3, channel 1.
P0[25]/AD0[2]/ I2SRX_SDA/ TXD3	7	D2	A3	[2]	I/O	**P0[25] —** General purpose digital input/output pin.
					I	**AD0[2] —** A/D converter 0, input 2.
					I/O	**I2SRX_SDA —** Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*. (LPC1769/68/67/66/65/63 only).
					O	**TXD3 —** Transmitter output for UART3.
P0[26]/AD0[3]/ AOUT/RXD3	6	D3	C5	[3]	I/O	**P0[26] —** General purpose digital input/output pin.
					I	**AD0[3] —** A/D converter 0, input 3.
					O	**AOUT —** DAC output (LPC1769/68/67/66/65/63 only).
					I	**RXD3 —** Receiver input for UART3.
P0[27]/SDA0/ USB_SDA	25	J2	C8	[4]	I/O	**P0[27] —** General purpose digital input/output pin. Output is open-drain.
					I/O	**SDA0 —** I^2C0 data input/output. Open-drain output (for I^2C-bus compliance).
					I/O	**USB_SDA —** USB port I^2C serial data (OTG transceiver, LPC1769/68/66/65 only).
P0[28]/SCL0/ USB_SCL	24	J1	B9	[4]	I/O	**P0[28] —** General purpose digital input/output pin. Output is open-drain.
					I/O	**SCL0 —** I^2C0 clock input/output. Open-drain output (for I^2C-bus compliance).
					I/O	**USB_SCL —** USB port I^2C serial clock (OTG transceiver, LPC1769/68/66/65 only).
P0[29]/USB_D+	29	J3	B10	[5]	I/O	**P0[29] —** General purpose digital input/output pin.
					I/O	**USB_D+ —** USB bidirectional D+ line. (LPC1769/68/66/65/64 only).
P0[30]/USB_D−	30	G4	C9	[5]	I/O	**P0[30] —** General purpose digital input/output pin.
					I/O	**USB_D− —** USB bidirectional D− line. (LPC1769/68/66/65/64 only).

Table 5. Pin description *…continued*

Symbol	Pin/ball				Type	Description
	LQFP100	TFBGA100	WLCSP100			
P1[18]/ USB_UP_LED/ PWM1[1]/ CAP1[0]	32	H4	D9	[1]	I/O	**P1[18] —** General purpose digital input/output pin.
					O	**USB_UP_LED —** USB GoodLink LED indicator. It is LOW when the device is configured (non-control endpoints enabled), or when the host is enabled and has detected a device on the bus. It is HIGH when the device is not configured, or when host is enabled and has not detected a device on the bus, or during global suspend. It transitions between LOW and HIGH (flashes) when the host is enabled and detects activity on the bus. (LPC1769/68/66/65/64 only).
					O	**PWM1[1] —** Pulse Width Modulator 1, channel 1 output.
					I	**CAP1[0] —** Capture input for Timer 1, channel 0.
P1[19]/MCOA0/ USB_PPWR/ CAP1[1]	33	J4	C10	[1]	I/O	**P1[19] —** General purpose digital input/output pin.
					O	**MCOA0 —** Motor control PWM channel 0, output A.
					O	**USB_PPWR —** Port Power enable signal for USB port. (LPC1769/68/66/65 only).
					I	**CAP1[1] —** Capture input for Timer 1, channel 1.
P1[20]/MCI0/ PWM1[2]/SCK0	34	K4	E8	[1]	I/O	**P1[20] —** General purpose digital input/output pin.
					I	**MCI0 —** Motor control PWM channel 0, input. Also Quadrature Encoder Interface PHA input.
					O	**PWM1[2] —** Pulse Width Modulator 1, channel 2 output.
					I/O	**SCK0 —** Serial clock for SSP0.
P1[21]/MCABORT/ PWM1[3]/ SSEL0	35	F5	E9	[1]	I/O	**P1[21] —** General purpose digital input/output pin.
					O	**MCABORT —** Motor control PWM, LOW-active fast abort.
					O	**PWM1[3] —** Pulse Width Modulator 1, channel 3 output.
					I/O	**SSEL0 —** Slave Select for SSP0.
P1[22]/MCOB0/ USB_PWRD/ MAT1[0]	36	J5	D10	[1]	I/O	**P1[22] —** General purpose digital input/output pin.
					O	**MCOB0 —** Motor control PWM channel 0, output B.
					I	**USB_PWRD —** Power Status for USB port (host power switch, LPC1769/68/66/65 only).
					O	**MAT1[0] —** Match output for Timer 1, channel 0.
P1[23]/MCI1/ PWM1[4]/MISO0	37	K5	E7	[1]	I/O	**P1[23] —** General purpose digital input/output pin.
					I	**MCI1 —** Motor control PWM channel 1, input. Also Quadrature Encoder Interface PHB input.
					O	**PWM1[4] —** Pulse Width Modulator 1, channel 4 output.
					I/O	**MISO0 —** Master In Slave Out for SSP0.
P1[24]/MCI2/ PWM1[5]/MOSI0	38	H5	F8	[1]	I/O	**P1[24] —** General purpose digital input/output pin.
					I	**MCI2 —** Motor control PWM channel 2, input. Also Quadrature Encoder Interface INDEX input.
					O	**PWM1[5] —** Pulse Width Modulator 1, channel 5 output.
					I/O	**MOSI0 —** Master Out Slave in for SSP0.

- Endpoint Maximum packet size selection (up to USB maximum specification) by software at run time.
- Supports SoftConnect and GoodLink features.
- While USB is in the Suspend mode, the part can enter one of the reduced power modes and wake up on USB activity.
- Supports DMA transfers with all on-chip SRAM blocks on all non-control endpoints.
- Allows dynamic switching between CPU-controlled slave and DMA modes.
- Double buffer implementation for Bulk and Isochronous endpoints.

8.12.2 USB host controller

The host controller enables full- and low-speed data exchange with USB devices attached to the bus. It consists of a register interface, a serial interface engine, and a DMA controller. The register interface complies with the OHCI specification.

8.12.2.1 Features

- OHCI compliant.
- One downstream port.
- Supports port power switching.

8.12.3 USB OTG controller

USB OTG is a supplement to the USB 2.0 specification that augments the capability of existing mobile devices and USB peripherals by adding host functionality for connection to USB peripherals.

The OTG Controller integrates the host controller, device controller, and a master-only I^2C-bus interface to implement OTG dual-role device functionality. The dedicated I^2C-bus interface controls an external OTG transceiver.

8.12.3.1 Features

- Fully compliant with *On-The-Go supplement to the USB 2.0 Specification, Revision 1.0a*.
- Hardware support for Host Negotiation Protocol (HNP).
- Includes a programmable timer required for HNP and Session Request Protocol (SRP).
- Supports any OTG transceiver compliant with the *OTG Transceiver Specification (CEA-2011), Rev. 1.0*.

8.13 CAN controller and acceptance filters

Remark: The CAN controllers are available on parts LPC1769/68/66/65/64. See Table 2.

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real-time control with a very high level of security. Its domain of application ranges from high-speed networks to low cost multiplex wiring.

The CAN block is intended to support multiple CAN buses simultaneously, allowing the device to be used as a gateway, switch, or router among a number of CAN buses in industrial or automotive applications.

8.29.2 Main PLL (PLL0)

The PLL0 accepts an input clock frequency in the range of 32 kHz to 25 MHz. The input frequency is multiplied up to a high frequency, then divided down to provide the actual clock used by the CPU and/or the USB block.

The PLL0 input, in the range of 32 kHz to 25 MHz, may initially be divided down by a value ‘N’, which may be in the range of 1 to 256. This input division provides a wide range of output frequencies from the same input frequency.

Following the PLL0 input divider is the PLL0 multiplier. This can multiply the input divider output through the use of a Current Controlled Oscillator (CCO) by a value ‘M’, in the range of 1 through 32768. The resulting frequency must be in the range of 275 MHz to 550 MHz. The multiplier works by dividing the CCO output by the value of M, then using a phase-frequency detector to compare the divided CCO output to the multiplier input. The error value is used to adjust the CCO frequency.

The PLL0 is turned off and bypassed following a chip Reset and by entering Power-down mode. PLL0 is enabled by software only. The program must configure and activate the PLL0, wait for the PLL0 to lock, and then connect to the PLL0 as a clock source.

8.29.3 USB PLL (PLL1)

The LPC17xx contain a second, dedicated USB PLL1 to provide clocking for the USB interface.

The PLL1 receives its clock input from the main oscillator only and provides a fixed 48 MHz clock to the USB block only. The PLL1 is disabled and powered off on reset. If the PLL1 is left disabled, the USB clock will be supplied by the 48 MHz clock from the main PLL0.

The PLL1 accepts an input clock frequency in the range of 10 MHz to 25 MHz only. The input frequency is multiplied up the range of 48 MHz for the USB clock using a Current Controlled Oscillators (CCO). It is insured that the PLL1 output has a 50 % duty cycle.

8.29.4 RTC clock output

The LPC17xx feature a clock output function intended for synchronizing with external devices and for use during system development to allow checking the internal clocks CCLK, IRC clock, main crystal, RTC clock, and USB clock in the outside world. The RTC clock output allows tuning the RTC frequency without probing the pin, which would distort the results.

8.29.5 Wake-up timer

The LPC17xx begin operation at power-up and when awakened from Power-down mode by using the 4 MHz IRC oscillator as the clock source. This allows chip operation to resume quickly. If the main oscillator or the PLL is needed by the application, software will need to enable these features and wait for them to stabilize before they are used as a clock source.

When the main oscillator is initially activated, the wake-up timer allows software to ensure that the main oscillator is fully functional before the processor uses it as a clock source and starts to execute instructions. This is important at power on, all types of Reset, and

The Deep-sleep mode can be terminated and normal operation resumed by either a Reset or certain specific interrupts that are able to function without clocks. Since all dynamic operation of the chip is suspended, Deep-sleep mode reduces chip power consumption to a very low value. Power to the flash memory is left on in Deep-sleep mode, allowing a very quick wake-up.

On wake-up from Deep-sleep mode, the code execution and peripherals activities will resume after 4 cycles expire if the IRC was used before entering Deep-sleep mode. If the main external oscillator was used, the code execution will resume when 4096 cycles expire. PLL and clock dividers need to be reconfigured accordingly.

8.29.6.3 Power-down mode

Power-down mode does everything that Deep-sleep mode does, but also turns off the power to the IRC oscillator and the flash memory. This saves more power but requires waiting for resumption of flash operation before execution of code or data access in the flash memory can be accomplished.

On the wake-up of Power-down mode, if the IRC was used before entering Power-down mode, it will take IRC 60 μs to start-up. After this 4 IRC cycles will expire before the code execution can then be resumed if the code was running from SRAM. In the meantime, the flash wake-up timer then counts 4 MHz IRC clock cycles to make the 100 μs flash start-up time. When it times out, access to the flash will be allowed. Users need to reconfigure the PLL and clock dividers accordingly.

8.29.6.4 Deep power-down mode

The Deep power-down mode can only be entered from the RTC block. In Deep power-down mode, power is shut off to the entire chip with the exception of the RTC module and the $\overline{\text{RESET}}$ pin.

The LPC17xx can wake up from Deep power-down mode via the $\overline{\text{RESET}}$ pin or an alarm match event of the RTC.

8.29.6.5 Wake-up interrupt controller

The Wake-up Interrupt Controller (WIC) allows the CPU to automatically wake up from any enabled priority interrupt that can occur while the clocks are stopped in Deep sleep, Power-down, and Deep power-down modes.

The WIC works in connection with the Nested Vectored Interrupt Controller (NVIC). When the CPU enters Deep sleep, Power-down, or Deep power-down mode, the NVIC sends a mask of the current interrupt situation to the WIC.This mask includes all of the interrupts that are both enabled and of sufficient priority to be serviced immediately. With this information, the WIC simply notices when one of the interrupts has occurred and then it wakes up the CPU.

The WIC eliminates the need to periodically wake up the CPU and poll the interrupts resulting in additional power savings.

8.29.7 Peripheral power control

A Power Control for Peripherals feature allows individual peripherals to be turned off if they are not needed in the application, resulting in additional power savings.

9. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(3V3)}$	supply voltage (3.3 V)	external rail	[2]	−0.5	+4.6	V
$V_{DD(REG)(3V3)}$	regulator supply voltage (3.3 V)		[2]	−0.5	+4.6	V
V_{DDA}	analog 3.3 V pad supply voltage		[2]	−0.5	+4.6	V
$V_{i(VBAT)}$	input voltage on pin VBAT	for the RTC	[2]	−0.5	+4.6	V
$V_{i(VREFP)}$	input voltage on pin VREFP		[2]	−0.5	+4.6	V
V_{IA}	analog input voltage	on ADC related pins	[2][3]	−0.5	+5.1	V
V_I	input voltage	5 V tolerant digital I/O pins; $V_{DD} \geq 2.4$ V	[2][4]	−0.5	+5.5	V_I
		$V_{DD} = 0$ V		−0.5	+3.6	
		5 V tolerant open-drain pins PIO0_27 and PIO0_28	[2][5]	−0.5	+5.5	
I_{DD}	supply current	per supply pin		-	100	mA
I_{SS}	ground current	per ground pin		-	100	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD(3V3)}) < V_I < (1.5V_{DD(3V3)})$; $T_j < 125$ °C		-	100	mA
T_{stg}	storage temperature		[6]	−65	+150	°C
$T_{j(max)}$	maximum junction temperature				150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins	[7]	−4000	+4000	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

c) The limiting values are stress ratings only. Operating the part at these values is not recommended, and proper operation is not guaranteed. The conditions for functional operation are specified in Table 8.

[2] Maximum/minimum voltage above the maximum operating voltage (see Table 8) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

[3] See Table 19 for maximum operating voltage.

[4] Including voltage on outputs in 3-state mode.

[5] V_{DD} present or not present. Compliant with the I^2C-bus standard. 5.5 V can be applied to this pin when V_{DD} is powered down.

[6] The maximum non-operating storage temperature is different than the temperature for required shelf life which should be determined based on required shelf lifetime. Please refer to the JEDEC spec (J-STD-033B.1) for further details.

[7] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

Table 8. Static characteristics *…continued*

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$I_{DD(ADC)}$	ADC supply current	active mode; ADC powered	[16][17]	-	1.95	-	mA
		ADC in Power-down mode	[16][18]	-	<0.2	-	μA
		deep sleep mode	[16]	-	38	-	nA
		power-down mode	[16]	-	38	-	nA
		deep power-down mode	[16]	-	24	-	nA
$I_{I(ADC)}$	ADC input current	on pin VREFP					
		deep sleep mode	[19]	-	100	-	nA
		power-down mode	[19]	-	100	-	nA
		deep power-down mode	[19]	-	100	-	nA
Standard port pins, $\overline{\text{RESET}}$, RTCK							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD(3V3)}$; on-chip pull-down resistor disabled		-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD(3V3)}$; on-chip pull-up/down resistors disabled		-	0.5	10	nA
V_I	input voltage	pin configured to provide a digital function	[20][21][22]	0	-	5.0	V
V_O	output voltage	output active		0	-	$V_{DD(3V3)}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD(3V3)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(3V3)}$	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA		$V_{DD(3V3)} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(3V3)} - 0.4$ V		−4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[23]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD(3V3)}$	[23]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V		10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V		−15	−50	−85	μA
		$V_{DD(3V3)} < V_I < 5$ V		0	0	0	μA

[5] The RTC typically fails when $V_{i(VBAT)}$ drops below 1.6 V.

[6] $V_{DD(REG)(3V3)}$ = 3.3 V; T_{amb} = 25 °C for all power consumption measurements.

[7] Applies to LPC1768/67/66/65/64/63.

[8] Applies to LPC1769 only.

[9] IRC running at 4 MHz; main oscillator and PLL disabled; PCLK = $^{CCLK}/_{8}$.

[10] BOD disabled.

[11] On pin $V_{DD(REG)(3V3)}$. I_{BAT} = 530 nA. $V_{DD(REG)(3V3)}$ = 3.0 V; V_{BAT} = 3.0 V; T_{amb} = 25 °C.

[12] On pin VBAT; $I_{DD(REG)(3V3)}$ = 630 nA; $V_{DD(REG)(3V3)}$ = 3.0 V; V_{BAT} = 3.0 V; T_{amb} = 25 °C.

[13] On pin VBAT; V_{BAT} = 3.0 V; T_{amb} = 25 °C.

[14] All internal pull-ups disabled. All pins configured as output and driven LOW. $V_{DD(3V3)}$ = 3.3 V; T_{amb} = 25 °C.

[15] TCK/SWDCLK pin needs to be externally pulled LOW.

[16] On pin V_{DDA}; V_{DDA} = 3.3 V; T_{amb} = 25 °C. The ADC is powered if the PDN bit in the AD0CR register is set to 1 and in Power-down mode of the PDN bit is set to 0.

[17] The ADC is powered if the PDN bit in the AD0CR register is set to 1. See *LPC17xx user manual UM10360_1*.

[18] The ADC is in Power-down mode if the PDN bit in the AD0CR register is set to 0. See *LPC17xx user manual UM10360_1*.

[19] $V_{i(VREFP)}$ = 3.3 V; T_{amb} = 25 °C.

[20] Including voltage on outputs in 3-state mode.

[21] $V_{DD(3V3)}$ supply voltages must be present.

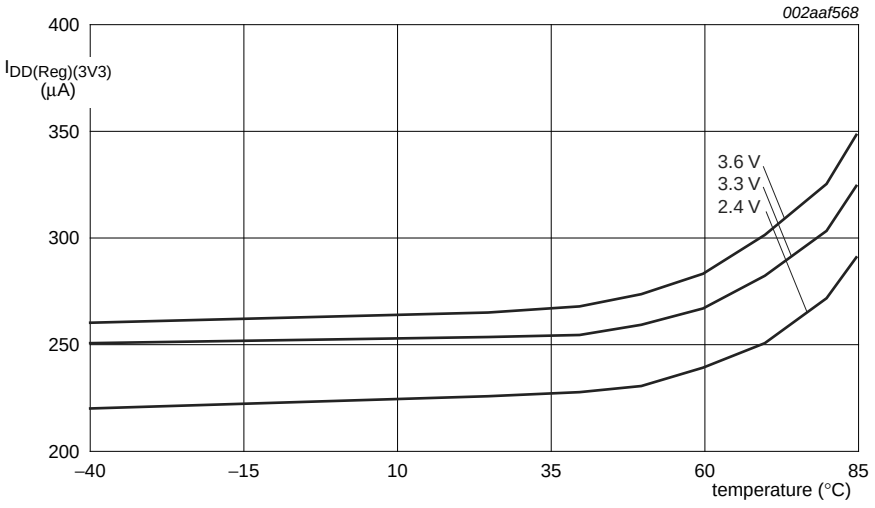
[22] 3-state outputs go into 3-state mode in Deep power-down mode.

[23] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[24] To V_{SS}.

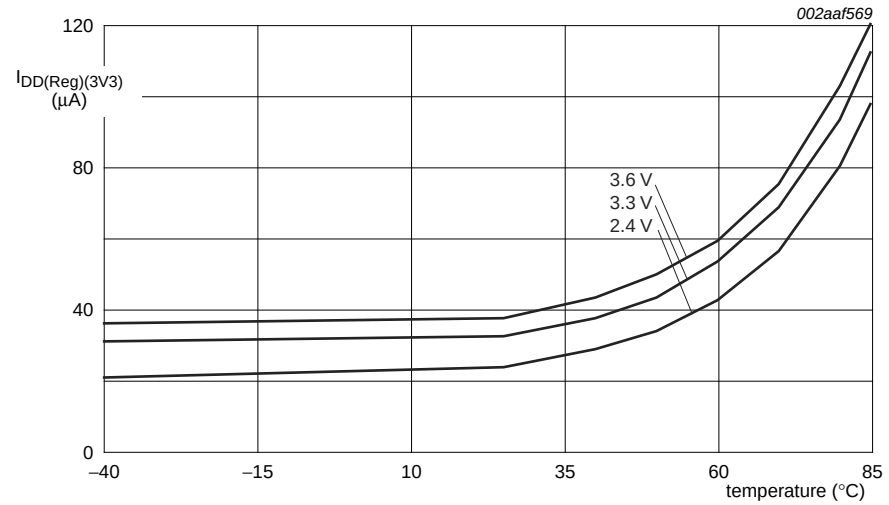
[25] Includes external resistors of 33 Ω ± 1 % on D+ and D−.

11.1 Power consumption



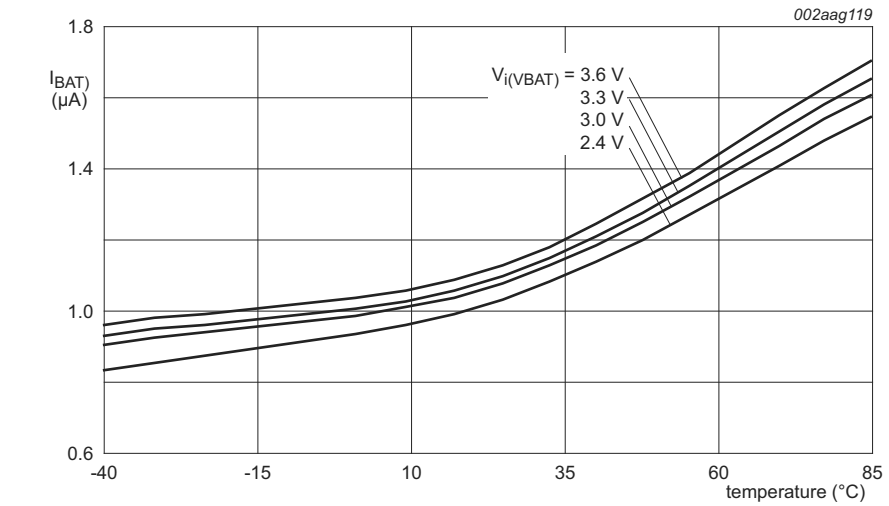
Conditions: BOD disabled.

Fig 8. Deep-sleep mode: typical regulator supply current $I_{DD(Reg)(3V3)}$ versus temperature



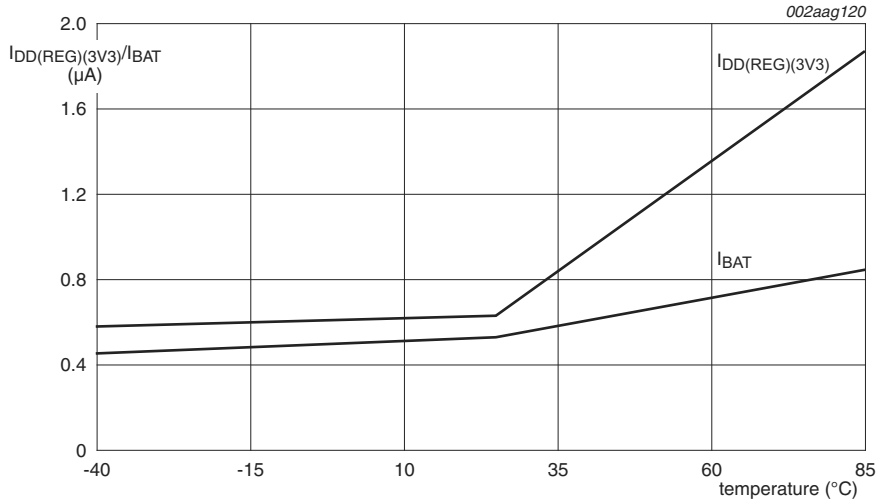
Conditions: BOD disabled.

Fig 9. Power-down mode: Typical regulator supply current $I_{DD(Reg)(3V3)}$ versus temperature



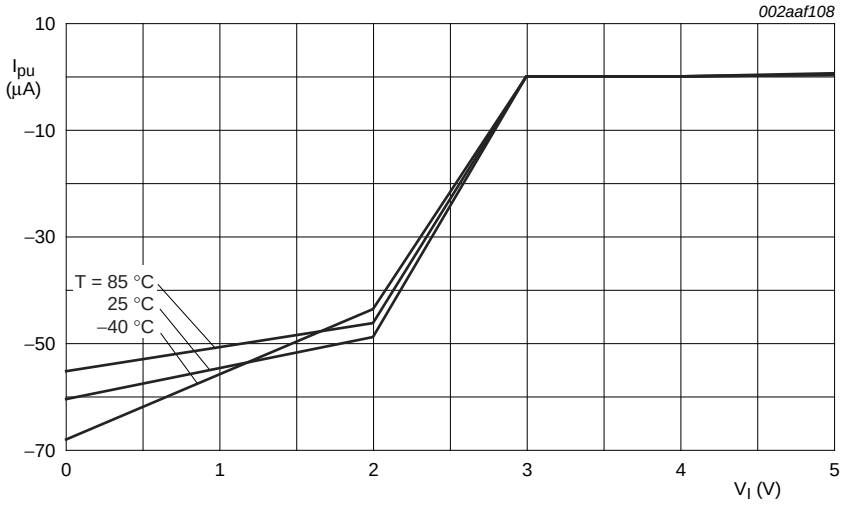
Conditions: $V_{DD(REG)(3V3)}$ floating; RTC running.

Fig 10. Deep power-down mode: Typical battery supply current I_{BAT} versus temperature



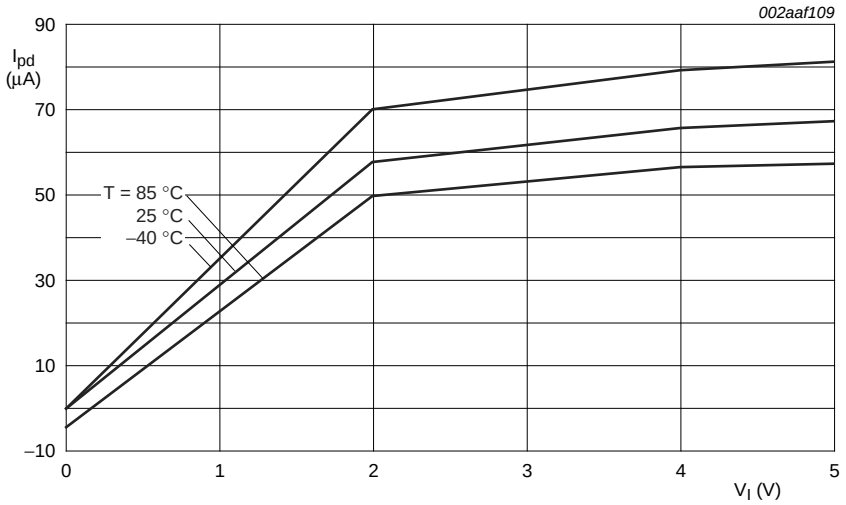
Conditions: V_{BAT} = 3.0 V; $V_{DD(REG)(3V3)}$ = 3.0 V; RTC running.

Fig 11. Deep power-down mode: Typical regulator supply current $I_{DD(REG)(3V3)}$ and battery supply current I_{BAT} versus temperature



Conditions: $V_{DD(REG)(3V3)} = V_{DD(3V3)} = 3.3$ V; standard port pins.

Fig 14. Typical pull-up current I_{pu} versus input voltage V_I



Conditions: $V_{DD(REG)(3V3)} = V_{DD(3V3)} = 3.3$ V; standard port pins.

Fig 15. Typical pull-down current I_{pd} versus input voltage V_I

12.3 Internal oscillators

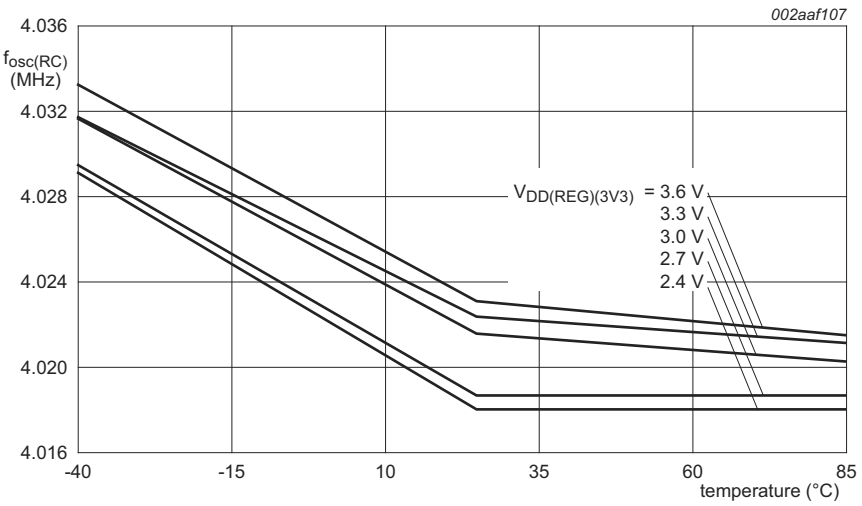
Table 12. Dynamic characteristic: internal oscillators

T_{amb} = −40 °C to +85 °C; 2.7 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V.[1]

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	-		3.96	4.02	4.04	MHz
$f_{i(RTC)}$	RTC input frequency	-		-	32.768	-	kHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.



Conditions: Frequency values are typical values. 4 MHz ± 1 % accuracy is guaranteed for 2.7 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V and T_{amb} = −40 °C to +85 °C. Variations between parts may cause the IRC to fall outside the 4 MHz ± 1 % accuracy specification for voltages below 2.7 V.

Fig 17. Internal RC oscillator frequency versus temperature

12.4 I/O pins

Table 13. Dynamic characteristic: I/O pins[1]

T_{amb} = −40 °C to +85 °C; $V_{DD(3V3)}$ over specified ranges.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	pin configured as output		3.0	-	5.0	ns
t_f	fall time	pin configured as output		2.5	-	5.0	ns

[1] Applies to standard I/O pins.

12.9 SPI

Table 18. Dynamic characteristics of SPI pins

T_{amb} = −40 °C to +85 °C.

Symbol	Parameter		Min	Typ	Max	Unit
$T_{cy(PCLK)}$	PCLK cycle time		10	-	-	ns
T_{SPICYC}	SPI cycle time	[1]	79.6	-	-	ns
$t_{SPICLKH}$	SPICLK HIGH time		0.485 × T_{SPICYC}	-	-	ns
$t_{SPICLKL}$	SPICLK LOW time			-	0.515 × T_{SPICYC}	ns
SPI master						
t_{SPIDSU}	SPI data set-up time	[2]	0	-	-	ns
t_{SPIDH}	SPI data hold time	[2]	2 × $T_{cy(PCLK)}$ − 5	-	-	ns
t_{SPIQV}	SPI data output valid time	[2]	2 × $T_{cy(PCLK)}$ + 30	-	-	ns
t_{SPIOH}	SPI output data hold time	[2]	2 × $T_{cy(PCLK)}$ + 5	-	-	ns
SPI slave						
t_{SPIDSU}	SPI data set-up time	[2]	0	-	-	ns
t_{SPIDH}	SPI data hold time	[2]	2 × $T_{cy(PCLK)}$ + 5	-	-	ns
t_{SPIQV}	SPI data output valid time	[2]	2 × $T_{cy(PCLK)}$ + 35	-	-	ns
t_{SPIOH}	SPI output data hold time	[2]	2 × $T_{cy(PCLK)}$ + 15	-	-	ns

[1] $T_{SPICYC} = (T_{cy(PCLK)} \times n) \pm 0.5$ %, n is the SPI clock divider value ($n \geq 8$); PCLK is derived from the processor clock CCLK.

[2] Timing parameters are measured with respect to the 50 % edge of the clock SCK and the 10 % (90 %) edge of the data signal (MOSI or MISO).

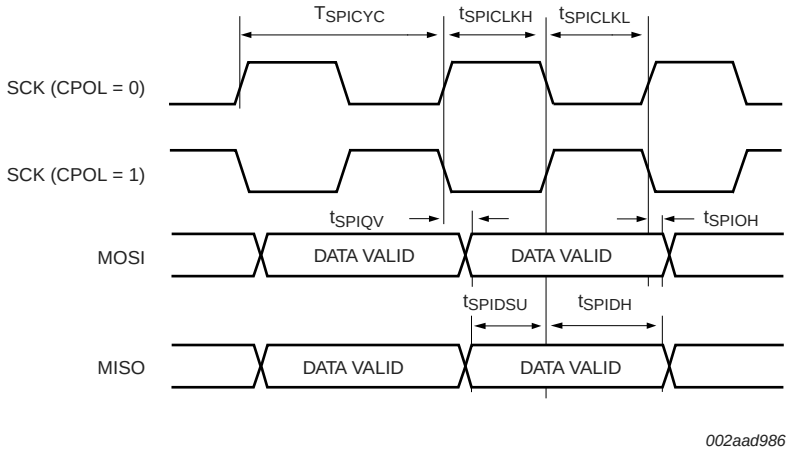


Fig 24. SPI master timing (CPHA = 1)

Table 20. ADC characteristics (lower resolution)

T_{amb} = −40 °C to +85 °C unless otherwise specified; 12-bit ADC used as 10-bit resolution ADC.[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
E_D	differential linearity error		[2][3]	-	±1	-	LSB
$E_{L(adj)}$	integral non-linearity		[4]	-	±1.5	-	LSB
E_O	offset error		[5]	-	±2	-	LSB
E_G	gain error		[6]	-	±2	-	LSB
$f_{clk(ADC)}$	ADC clock frequency	$3.0\ V \leq V_{DDA} \leq 3.6\ V$		-	-	33	MHz
		$2.7\ V \leq V_{DDA} < 3.0\ V$		-	-	25	MHz
$f_{c(ADC)}$	ADC conversion frequency	$3\ V \leq V_{DDA} \leq 3.6\ V$	[7]	-	-	500	kHz
		$2.7\ V \leq V_{DDA} < 3.0\ V$	[7]	-	-	400	kHz

[1] V_{DDA} and VREFP should be tied to $V_{DD(3V3)}$ if the ADC and DAC are not used.

[2] The ADC is monotonic, there are no missing codes.

[3] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 28.

[4] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 28.

[5] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 28.

[6] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 28.

[7] The conversion frequency corresponds to the number of samples per second.

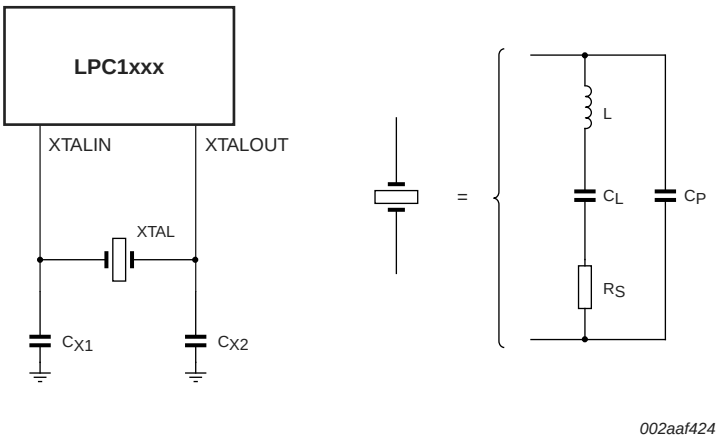


Fig 37. Oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

Table 23. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters): low frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}/C_{X2}
1 MHz to 5 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 300 Ω	39 pF, 39 pF
	30 pF	< 300 Ω	57 pF, 57 pF
5 MHz to 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz to 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz to 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

Table 24. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters): high frequency mode

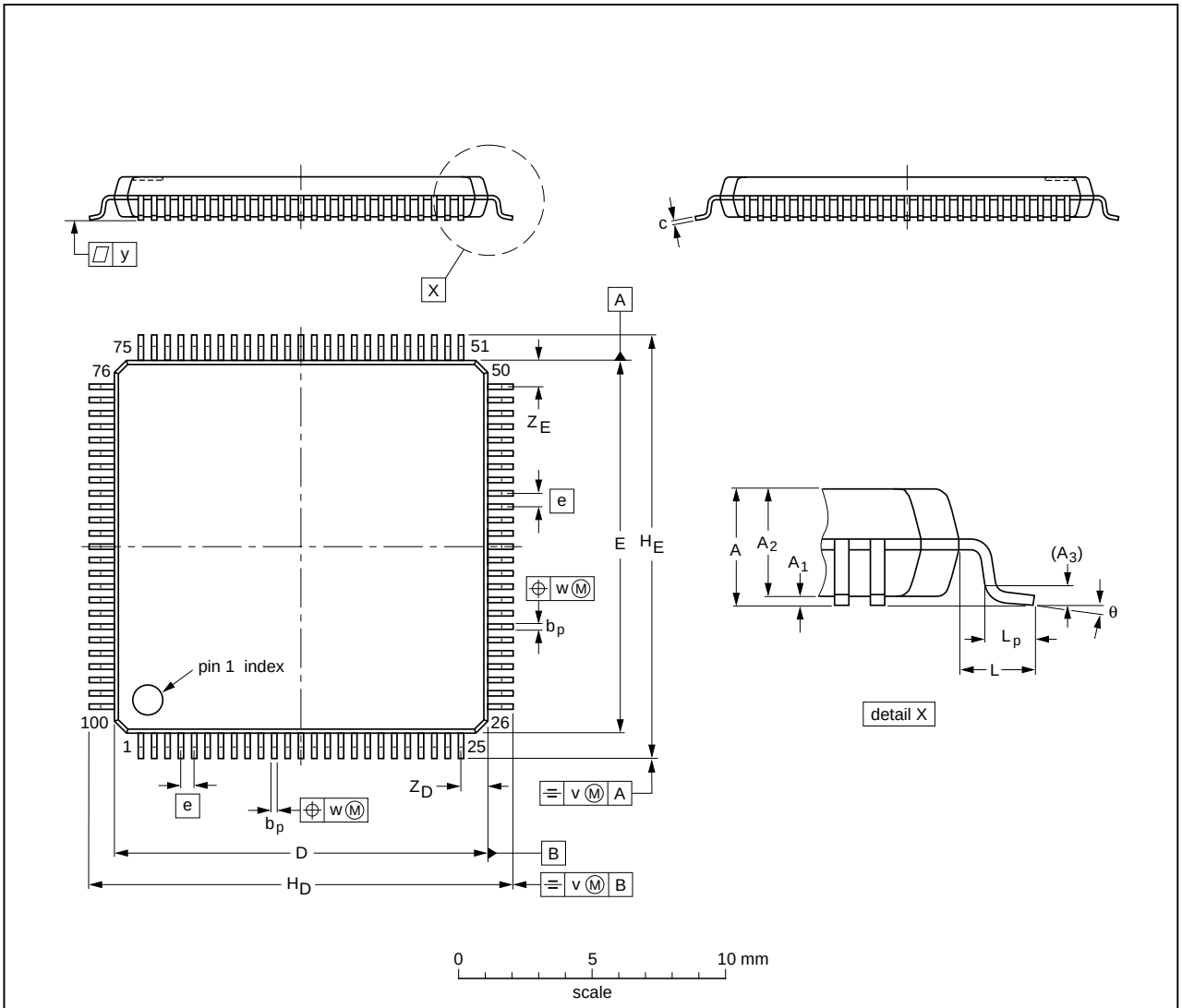
Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz to 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz to 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

15.3 XTAL and RTCX Printed Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{x1}, C_{x2}, and C_{x3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plain. Loops must be made as small as possible in

16. Package outline

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm **SOT407-1**



DIMENSIONS (mm are the original dimensions)

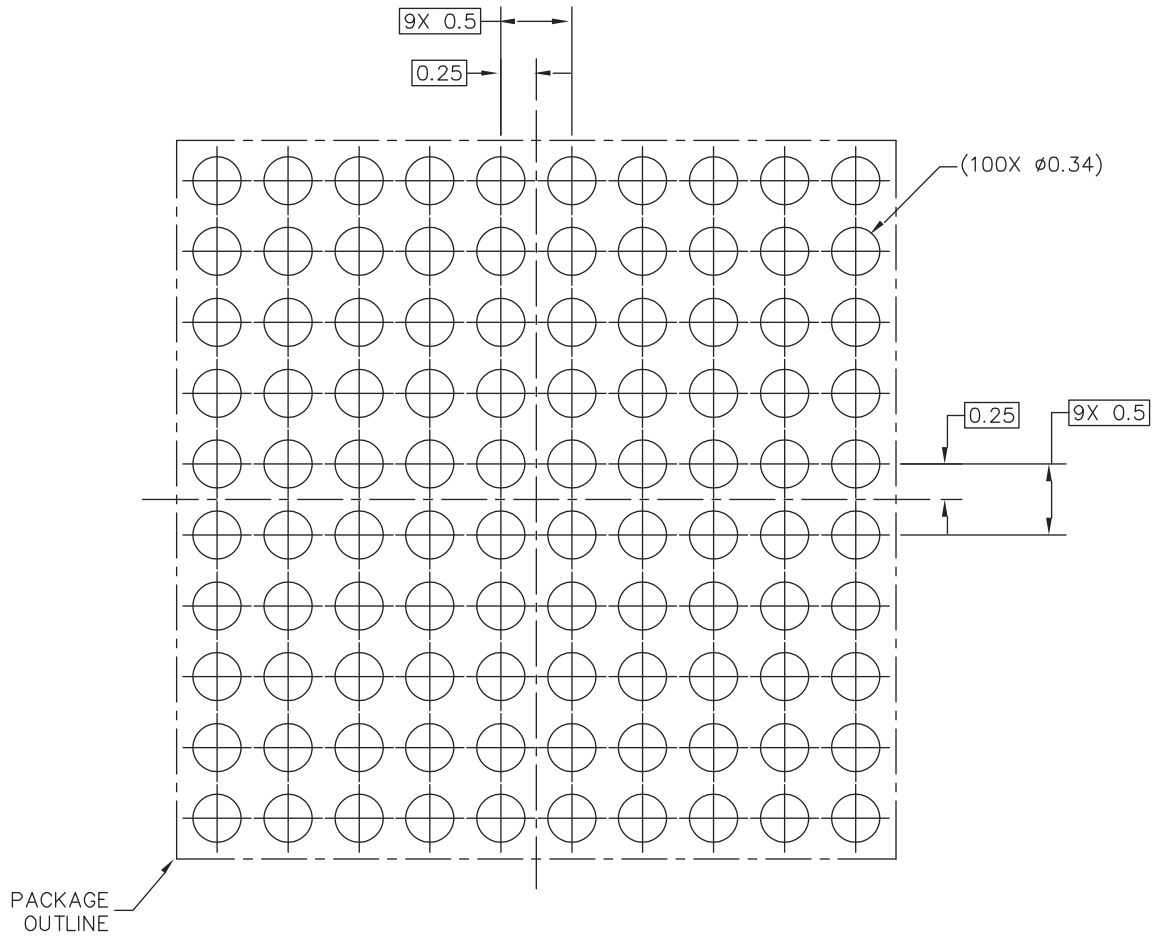
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1	0.75 0.45	0.2	0.08	0.08	1.15 0.85	1.15 0.85	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT407-1	136E20	MS-026				~~00-02-01~~ 03-02-20

Fig 40. Package outline SOT407-1 (LQFP100)



RECOMMENDED STENCIL THICKNESS 0.125

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

 DATE: 06 MAR 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: SOT1450–2	REVISION: 0	

Fig 47. Reflow soldering of the WLCSP100 package (part 3)

Table 27. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC1769_68_67_66_65_64_63 v.9.2	20131021	Product data sheet	-	LPC1769_68_67_66_65_64 v.9.1
Modifications:	• Table 8 “Static characteristics”: – Added Table note 3 “VDDA and VREFP should be tied to VDD(3V3) if the ADC and DAC are not used.” – Added Table note 4 “VDDA for DAC specs are from 2.7 V to 3.6 V.” – V_{DDA}/VREFP spec changed from 2.7 V to 2.5 V. • Table 19 “ADC characteristics (full resolution)”: – Added Table note 1 “VDDA and VREFP should be tied to VDD(3V3) if the ADC and DAC are not used.” – V_{DDA} changed from 2.7 V to 2.5 V. • Table 20 “ADC characteristics (lower resolution)”: Added Table note 1 “VDDA and VREFP should be tied to VDD(3V3) if the ADC and DAC are not used.”			
LPC1769_68_67_66_65_64_63 v.9.1	20130916	Product data sheet	-	LPC1769_68_67_66_65_64 v.9
Modifications:	• Added Table 7 “Thermal resistance”. • Table 6 “Limiting values”: – Updated min/max values for $V_{DD(3V3)}$ and $V_{DD(REG)(3V3)}$. – Updated conditions for V_I. – Updated table notes. • Table 8 “Static characteristics”: Added Table note 15 “TCK/SWDCLK pin needs to be externally pulled LOW.” • Updated Section 15.1 “Suggested USB interface solutions”. • Added Section 5 “Marking”. • Changed title of Figure 31 from “USB interface on a self-powered device” to “USB interface with soft-connect”.			
LPC1769_68_67_66_65_64_63 v.9	20120810	Product data sheet	-	LPC1769_68_67_66_65_64 v.8
Modifications:	• Remove table note “The peak current is limited to 25 times the corresponding maximum current.” from Table 5 “Limiting values”. • Change $V_{DD(3V3)}$ to $V_{DD(REG)(3V3)}$ in Section 11.3 “Internal oscillators”. • Glitch filter constant changed to 10 ns in Table note 6 in Table 4. • Description of $\overline{\text{RESET}}$ function updated in Table 4. • Pull-up value added for GPIO pins in Table 4. • Pin configuration diagram for LQFP100 package corrected (Figure 2).			
LPC1769_68_67_66_65_64_63 v.8	20111114	Product data sheet	-	LPC1769_68_67_66_65_64 v.7
Modifications:	• Pin description of USB_UP_LED pin updated in Table 4. • R_{i1} and R_{i2} labels in Figure 27 updated. • Part LPC1765FET100 added. • Table note 10 updated in Table 4. • Table note 1 updated in Table 12. • Pin description of STCLK pin updated in Table 4. • Electromagnetic compatibility data added in Section 14.6. • Section 16 added.			