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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, Ethernet, I²C, IrDA, Microwire, SPI, SSI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT
Number of I/O	70
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1768fbd100-551

Table 5. Pin description *…continued*

Symbol	Pin/ball				Type	Description
	LQFP100	TFBGA100	WLCSP100			
P0[4]/ I2SRX_CLK/ RD2/CAP2[0]	81	A8	G2	[1]	I/O	**P0[4] —** General purpose digital input/output pin.
					I/O	**I2SRX_CLK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I²S-bus specification*. (LPC1769/68/67/66/65/63 only).
					I	**RD2 —** CAN2 receiver input. (LPC1769/68/66/65/64 only).
					I	**CAP2[0] —** Capture input for Timer 2, channel 0.
P0[5]/ I2SRX_WS/ TD2/CAP2[1]	80	D7	H1	[1]	I/O	**P0[5] —** General purpose digital input/output pin.
					I/O	**I2SRX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*. (LPC1769/68/67/66/65/63 only).
					O	**TD2 —** CAN2 transmitter output. (LPC1769/68/66/65/64 only).
					I	**CAP2[1] —** Capture input for Timer 2, channel 1.
P0[6]/ I2SRX_SDA/ SSEL1/MAT2[0]	79	B8	G3	[1]	I/O	**P0[6] —** General purpose digital input/output pin.
					I/O	**I2SRX_SDA —** Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*. (LPC1769/68/67/66/65/63 only).
					I/O	**SSEL1 —** Slave Select for SSP1.
					O	**MAT2[0] —** Match output for Timer 2, channel 0.
P0[7]/ I2STX_CLK/ SCK1/MAT2[1]	78	A9	J1	[1]	I/O	**P0[7] —** General purpose digital input/output pin.
					I/O	**I2STX_CLK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I²S-bus specification*. (LPC1769/68/67/66/65/63 only).
					I/O	**SCK1 —** Serial Clock for SSP1.
					O	**MAT2[1] —** Match output for Timer 2, channel 1.
P0[8]/ I2STX_WS/ MISO1/MAT2[2]	77	C8	H2	[1]	I/O	**P0[8] —** General purpose digital input/output pin.
					I/O	**I2STX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*. (LPC1769/68/67/66/65/63 only).
					I/O	**MISO1 —** Master In Slave Out for SSP1.
					O	**MAT2[2] —** Match output for Timer 2, channel 2.
P0[9]/ I2STX_SDA/ MOSI1/MAT2[3]	76	A10	H3	[1]	I/O	**P0[9] —** General purpose digital input/output pin.
					I/O	**I2STX_SDA —** Transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*. (LPC1769/68/67/66/65/63 only).
					I/O	**MOSI1 —** Master Out Slave In for SSP1.
					O	**MAT2[3] —** Match output for Timer 2, channel 3.
P0[10]/TXD2/ SDA2/MAT3[0]	48	H7	H8	[1]	I/O	**P0[10] —** General purpose digital input/output pin.
					O	**TXD2 —** Transmitter output for UART2.
					I/O	**SDA2 —** I²C2 data input/output (this is not an open-drain pin).
					O	**MAT3[0] —** Match output for Timer 3, channel 0.

Table 5. Pin description *…continued*

Symbol	Pin/ball				Type	Description
	LQFP100	TFBGA100	WLCSP100			
P2[2]/PWM1[3]/ CTS1/ TRACEDATA[3]	73	D8	K2	[1]	I/O	**P2[2] —** General purpose digital input/output pin.
					O	**PWM1[3] —** Pulse Width Modulator 1, channel 3 output.
					I	**CTS1 —** Clear to Send input for UART1.
					O	**TRACEDATA[3] —** Trace data, bit 3.
P2[3]/PWM1[4]/ DCD1/ TRACEDATA[2]	70	E7	K3	[1]	I/O	**P2[3] —** General purpose digital input/output pin.
					O	**PWM1[4] —** Pulse Width Modulator 1, channel 4 output.
					I	**DCD1 —** Data Carrier Detect input for UART1.
					O	**TRACEDATA[2] —** Trace data, bit 2.
P2[4]/PWM1[5]/ DSR1/ TRACEDATA[1]	69	D9	J3	[1]	I/O	**P2[4] —** General purpose digital input/output pin.
					O	**PWM1[5] —** Pulse Width Modulator 1, channel 5 output.
					I	**DSR1 —** Data Set Ready input for UART1.
					O	**TRACEDATA[1] —** Trace data, bit 1.
P2[5]/PWM1[6]/ DTR1/ TRACEDATA[0]	68	D10	H4	[1]	I/O	**P2[5] —** General purpose digital input/output pin.
					O	**PWM1[6] —** Pulse Width Modulator 1, channel 6 output.
					O	**DTR1 —** Data Terminal Ready output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal.
					O	**TRACEDATA[0] —** Trace data, bit 0.
P2[6]/PCAP1[0]/ RI1/TRACECLK	67	E8	K4	[1]	I/O	**P2[6] —** General purpose digital input/output pin.
					I	**PCAP1[0] —** Capture input for PWM1, channel 0.
					I	**RI1 —** Ring Indicator input for UART1.
					O	**TRACECLK —** Trace Clock.
P2[7]/RD2/ RTS1	66	E9	J4	[1]	I/O	**P2[7] —** General purpose digital input/output pin.
					I	**RD2 —** CAN2 receiver input. (LPC1769/68/66/65/64 only).
					O	**RTS1 —** Request to Send output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal.
P2[8]/TD2/ TXD2	65	E10	H5	[1]	I/O	**P2[8] —** General purpose digital input/output pin.
					O	**TD2 —** CAN2 transmitter output. (LPC1769/68/66/65/64 only).
					O	**TXD2 —** Transmitter output for UART2.
P2[9]/ USB_CONNECT/ RXD2	64	F7	K5	[1]	I/O	**P2[9] —** General purpose digital input/output pin.
					O	**USB_CONNECT —** Signal used to switch an external 1.5 kΩ resistor under software control. Used with the SoftConnect USB feature. (LPC1769/68/66/65/64 only).
					I	**RXD2 —** Receiver input for UART2.
P2[10]/$\overline{\text{EINT0}}$/NMI	53	J10	K9	[6]	I/O	**P2[10] —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
					I	**$\overline{\text{EINT0}}$ —** External interrupt 0 input.
					I	**NMI —** Non-maskable interrupt input.

8.7 Nested Vectored Interrupt Controller (NVIC)

The NVIC is an integral part of the Cortex-M3. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

8.7.1 Features

- Controls system exceptions and peripheral interrupts
- In the LPC17xx, the NVIC supports 33 vectored interrupts
- 32 programmable interrupt priority levels, with hardware priority level masking
- Relocatable vector table
- Non-Maskable Interrupt (NMI)
- Software interrupt generation

8.7.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Any pin on Port 0 and Port 2 (total of 42 pins) regardless of the selected function, can be programmed to generate an interrupt on a rising edge, a falling edge, or both.

8.8 Pin connect block

The pin connect block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Peripherals should be connected to the appropriate pins prior to being activated and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

Most pins can also be configured as open-drain outputs or to have a pull-up, pull-down, or no resistor enabled.

8.9 General purpose DMA controller

The GPDMA is an AMBA AHB compliant peripheral allowing selected peripherals to have DMA support.

The GPDMA enables peripheral-to-memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions. The source and destination areas can each be either a memory region or a peripheral, and can be accessed through the AHB master. The GPDMA controller allows data transfers between the USB and Ethernet controllers and the various on-chip SRAM areas. The supported APB peripherals are SSP0/1, all UARTs, the I^2S-bus interface, the ADC, and the DAC. Two match signals for each timer can be used to trigger DMA transfers.

Remark: The Ethernet controller is available on parts LPC1769/68/67/66/64. The USB controller is available on parts LPC1769/68/66/65/64. The I^2S-bus interface is available on parts LPC1769/68/67/66/65. The DAC is available on parts LPC1769/68/67/66/65/63.

8.9.1 Features

- Eight DMA channels. Each channel can support an unidirectional transfer.
- 16 DMA request lines.
- Single DMA and burst DMA request signals. Each peripheral connected to the DMA Controller can assert either a burst DMA request or a single DMA request. The DMA burst size is set by programming the DMA Controller.
- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral transfers are supported.
- Scatter or gather DMA is supported through the use of linked lists. This means that the source and destination areas do not have to occupy contiguous areas of memory.
- Hardware DMA channel priority.
- AHB slave DMA programming interface. The DMA Controller is programmed by writing to the DMA control registers over the AHB slave interface.
- One AHB bus master for transferring data. The interface transfers data when a DMA request goes active.
- 32-bit AHB master bus width.
- Incrementing or non-incrementing addressing for source and destination.
- Programmable DMA burst size. The DMA burst size can be programmed to more efficiently transfer data.
- Internal four-word FIFO per channel.
- Supports 8, 16, and 32-bit wide transactions.
- Big-endian and little-endian support. The DMA Controller defaults to little-endian mode on reset.
- An interrupt to the processor can be generated on a DMA completion or when a DMA error has occurred.
- Raw interrupt status. The DMA error and DMA count raw interrupt status can be read prior to masking.

8.10 Fast general purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back as well as the current state of the port pins.

LPC17xx use accelerated GPIO functions:

- GPIO registers are accessed through the AHB multilayer bus so that the fastest possible I/O timing can be achieved.
- Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
- All GPIO registers are byte and half-word addressable.
- Entire port value can be written in one instruction.
- Support for Cortex-M3 bit banding.
- Support for use with the GPDMA controller.

- Supports single edge controlled and/or double edge controlled PWM outputs. Single edge controlled PWM outputs all go high at the beginning of each cycle unless the output is a constant low. Double edge controlled PWM outputs can have either edge occur at any position within a cycle. This allows for both positive going and negative going pulses.
- Pulse period and width can be any number of timer counts. This allows complete flexibility in the trade-off between resolution and repetition rate. All PWM outputs will occur at the same repetition rate.
- Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses.
- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must ‘release’ new match values before they can become effective.
- May be used as a standard 32-bit timer/counter with a programmable 32-bit prescaler if the PWM mode is not enabled.

8.23 Motor control PWM

The motor control PWM is a specialized PWM supporting 3-phase motors and other combinations. Feedback inputs are provided to automatically sense rotor position and use that information to ramp speed up or down. An abort input is also provided that causes the PWM to immediately release all motor drive outputs. At the same time, the motor control PWM is highly configurable for other generalized timing, counting, capture, and compare applications.

8.24 Quadrature Encoder Interface (QEI)

A quadrature encoder, also known as a 2-channel incremental encoder, converts angular displacement into two pulse signals. By monitoring both the number of pulses and the relative phase of the two signals, the user can track the position, direction of rotation, and velocity. In addition, a third channel, or index signal, can be used to reset the position counter. The quadrature encoder interface decodes the digital pulses from a quadrature encoder wheel to integrate position over time and determine direction of rotation. In addition, the QEI can capture the velocity of the encoder wheel.

8.24.1 Features

- Tracks encoder position.
- Increments/decrements depending on direction.
- Programmable for 2× or 4× position counting.
- Velocity capture using built-in timer.
- Velocity compare function with “less than” interrupt.
- Uses 32-bit registers for position and velocity.
- Three position compare registers with interrupts.
- Index counter for revolution counting.
- Index compare register with interrupts.
- Can combine index and position interrupts to produce an interrupt for whole and partial revolution displacement.

The Deep-sleep mode can be terminated and normal operation resumed by either a Reset or certain specific interrupts that are able to function without clocks. Since all dynamic operation of the chip is suspended, Deep-sleep mode reduces chip power consumption to a very low value. Power to the flash memory is left on in Deep-sleep mode, allowing a very quick wake-up.

On wake-up from Deep-sleep mode, the code execution and peripherals activities will resume after 4 cycles expire if the IRC was used before entering Deep-sleep mode. If the main external oscillator was used, the code execution will resume when 4096 cycles expire. PLL and clock dividers need to be reconfigured accordingly.

8.29.6.3 Power-down mode

Power-down mode does everything that Deep-sleep mode does, but also turns off the power to the IRC oscillator and the flash memory. This saves more power but requires waiting for resumption of flash operation before execution of code or data access in the flash memory can be accomplished.

On the wake-up of Power-down mode, if the IRC was used before entering Power-down mode, it will take IRC 60 μs to start-up. After this 4 IRC cycles will expire before the code execution can then be resumed if the code was running from SRAM. In the meantime, the flash wake-up timer then counts 4 MHz IRC clock cycles to make the 100 μs flash start-up time. When it times out, access to the flash will be allowed. Users need to reconfigure the PLL and clock dividers accordingly.

8.29.6.4 Deep power-down mode

The Deep power-down mode can only be entered from the RTC block. In Deep power-down mode, power is shut off to the entire chip with the exception of the RTC module and the $\overline{\text{RESET}}$ pin.

The LPC17xx can wake up from Deep power-down mode via the $\overline{\text{RESET}}$ pin or an alarm match event of the RTC.

8.29.6.5 Wake-up interrupt controller

The Wake-up Interrupt Controller (WIC) allows the CPU to automatically wake up from any enabled priority interrupt that can occur while the clocks are stopped in Deep sleep, Power-down, and Deep power-down modes.

The WIC works in connection with the Nested Vectored Interrupt Controller (NVIC). When the CPU enters Deep sleep, Power-down, or Deep power-down mode, the NVIC sends a mask of the current interrupt situation to the WIC.This mask includes all of the interrupts that are both enabled and of sufficient priority to be serviced immediately. With this information, the WIC simply notices when one of the interrupts has occurred and then it wakes up the CPU.

The WIC eliminates the need to periodically wake up the CPU and poll the interrupts resulting in additional power savings.

8.29.7 Peripheral power control

A Power Control for Peripherals feature allows individual peripherals to be turned off if they are not needed in the application, resulting in additional power savings.

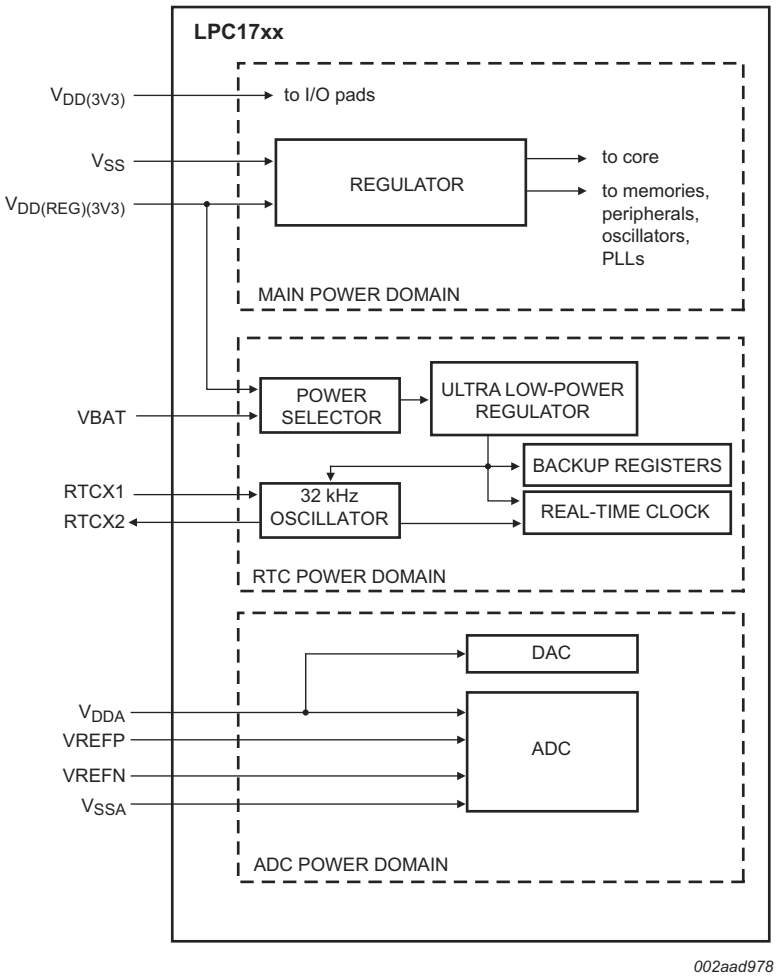


Fig 7. Power distribution

8.30 System control

8.30.1 Reset

Reset has four sources on the LPC17xx: the $\overline{\text{RESET}}$ pin, the Watchdog reset, power-on reset (POR), and the BrownOut Detection (BOD) circuit. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip Reset by any source, once the operating voltage attains a usable level, causes the $\overline{\text{RSTOUT}}$ pin to go LOW and starts the wake-up timer (see description in Section 8.29.5). The wake-up timer ensures that reset remains asserted until the external Reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the flash controller has completed its initialization. Once reset is de-asserted, or, in case of a BOD-triggered reset, once the voltage rises above the BOD threshold, the $\overline{\text{RSTOUT}}$ pin goes HIGH.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the Boot Block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

Table 8. Static characteristics *…continued*

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I²C-bus pins (P0[27] and P0[28])							
V_{IH}	HIGH-level input voltage			$0.7V_{DD(3V3)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(3V3)}$	V
V_{hys}	hysteresis voltage			-	$0.05 \times V_{DD(3V3)}$	-	V
V_{OL}	LOW-level output voltage	I_{OLS} = 3 mA		-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{DD(3V3)}$	[24]	-	2	4	μA
		V_I = 5 V		-	10	22	μA
Oscillator pins							
$V_{i(XTAL1)}$	input voltage on pin XTAL1			−0.5	1.8	1.95	V
$V_{o(XTAL2)}$	output voltage on pin XTAL2			−0.5	1.8	1.95	V
$V_{i(RTCX1)}$	input voltage on pin RTCX1			−0.5	-	3.6	V
$V_{o(RTCX2)}$	output voltage on pin RTCX2			−0.5	-	3.6	V
USB pins (LPC1769/68/66/65/64 only)							
I_{OZ}	OFF-state output current	0 V < V_I < 3.3 V	[2]	-	-	±10	μA
V_{BUS}	bus supply voltage		[2]	-	-	5.25	V
V_{DI}	differential input sensitivity voltage	|(D+) − (D−)|	[2]	0.2	-	-	V
V_{CM}	differential common mode voltage range	includes V_{DI} range	[2]	0.8	-	2.5	V
$V_{th(rs)se}$	single-ended receiver switching threshold voltage		[2]	0.8	-	2.0	V
V_{OL}	LOW-level output voltage for low-/full-speed	R_L of 1.5 kΩ to 3.6 V	[2]	-	-	0.18	V
V_{OH}	HIGH-level output voltage (driven) for low-/full-speed	R_L of 15 kΩ to GND	[2]	2.8	-	3.5	V
C_{trans}	transceiver capacitance	pin to GND	[2]	-	-	20	pF
Z_{DRV}	driver output impedance for driver which is not high-speed capable	with 33 Ω series resistor; steady state drive	[2][25]	36	-	44.1	Ω

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] For USB operation 3.0 V ≤ $V_{DD((3V3)}$ ≤ 3.6 V. Guaranteed by design.

[3] V_{DDA} and VREFP should be tied to $V_{DD(3V3)}$ if the ADC and DAC are not used.

[4] V_{DDA} for DAC specs are from 2.7 V to 3.6 V.

[5] The RTC typically fails when $V_{i(VBAT)}$ drops below 1.6 V.

[6] $V_{DD(REG)(3V3)}$ = 3.3 V; T_{amb} = 25 °C for all power consumption measurements.

[7] Applies to LPC1768/67/66/65/64/63.

[8] Applies to LPC1769 only.

[9] IRC running at 4 MHz; main oscillator and PLL disabled; PCLK = $^{CCLK}/_{8}$.

[10] BOD disabled.

[11] On pin $V_{DD(REG)(3V3)}$. I_{BAT} = 530 nA. $V_{DD(REG)(3V3)}$ = 3.0 V; V_{BAT} = 3.0 V; T_{amb} = 25 °C.

[12] On pin VBAT; $I_{DD(REG)(3V3)}$ = 630 nA; $V_{DD(REG)(3V3)}$ = 3.0 V; V_{BAT} = 3.0 V; T_{amb} = 25 °C.

[13] On pin VBAT; V_{BAT} = 3.0 V; T_{amb} = 25 °C.

[14] All internal pull-ups disabled. All pins configured as output and driven LOW. $V_{DD(3V3)}$ = 3.3 V; T_{amb} = 25 °C.

[15] TCK/SWDCLK pin needs to be externally pulled LOW.

[16] On pin V_{DDA}; V_{DDA} = 3.3 V; T_{amb} = 25 °C. The ADC is powered if the PDN bit in the AD0CR register is set to 1 and in Power-down mode of the PDN bit is set to 0.

[17] The ADC is powered if the PDN bit in the AD0CR register is set to 1. See *LPC17xx user manual UM10360_1*.

[18] The ADC is in Power-down mode if the PDN bit in the AD0CR register is set to 0. See *LPC17xx user manual UM10360_1*.

[19] $V_{i(VREFP)}$ = 3.3 V; T_{amb} = 25 °C.

[20] Including voltage on outputs in 3-state mode.

[21] $V_{DD(3V3)}$ supply voltages must be present.

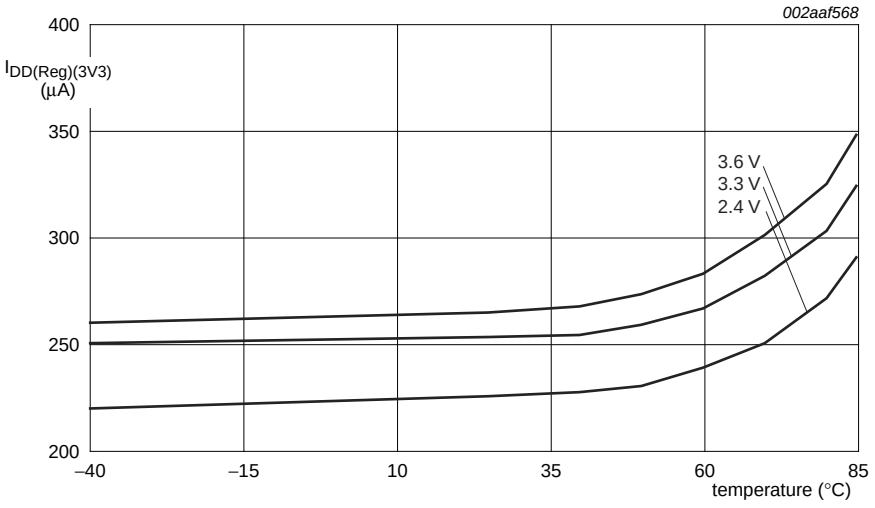
[22] 3-state outputs go into 3-state mode in Deep power-down mode.

[23] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[24] To V_{SS}.

[25] Includes external resistors of 33 Ω ± 1 % on D+ and D−.

11.1 Power consumption



Conditions: BOD disabled.

Fig 8. Deep-sleep mode: typical regulator supply current $I_{DD(Reg)(3V3)}$ versus temperature

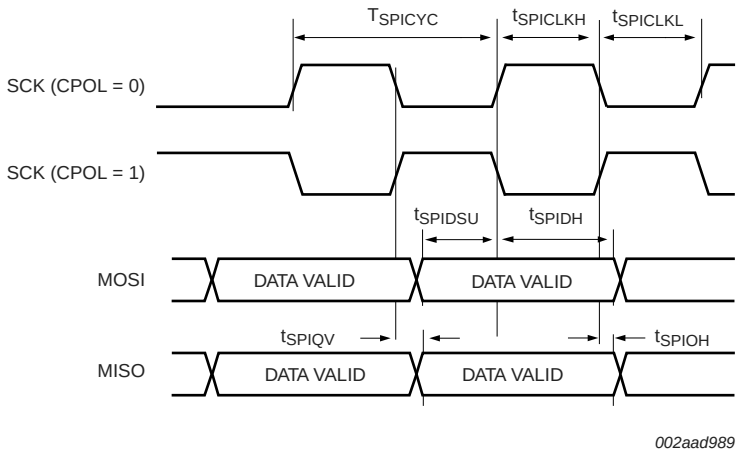


Fig 27. SPI slave timing (CPHA = 0)

13. ADC electrical characteristics

Table 19. ADC characteristics (full resolution)

V_{DDA} = 2.5 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified; ADC frequency 13 MHz; 12-bit resolution.[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IA}	analog input voltage			0	-	V_{DDA}	V
C_{ia}	analog input capacitance			-	-	15	pF
E_D	differential linearity error		[2][3]	-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity		[4]	-	-	±3	LSB
E_O	offset error		[5][6]	-	-	±2	LSB
E_G	gain error		[7]	-	-	0.5	%
E_T	absolute error		[8]	-	-	4	LSB
R_{vsi}	voltage source interface resistance		[9]	-	-	7.5	kΩ
$f_{clk(ADC)}$	ADC clock frequency			-	-	13	MHz
$f_{c(ADC)}$	ADC conversion frequency		[10]	-	-	200	kHz

[1] V_{DDA} and VREFP should be tied to $V_{DD(3V3)}$ if the ADC and DAC are not used.

[2] The ADC is monotonic, there are no missing codes.

[3] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 28.

[4] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 28.

[5] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 28.

[6] ADCOFFS value (bits 7:4) = 2 in the ADTRM register. See *LPC17xx user manual UM10360*.

[7] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 28.

[8] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 28.

[9] See Figure 29.

[10] The conversion frequency corresponds to the number of samples per second.

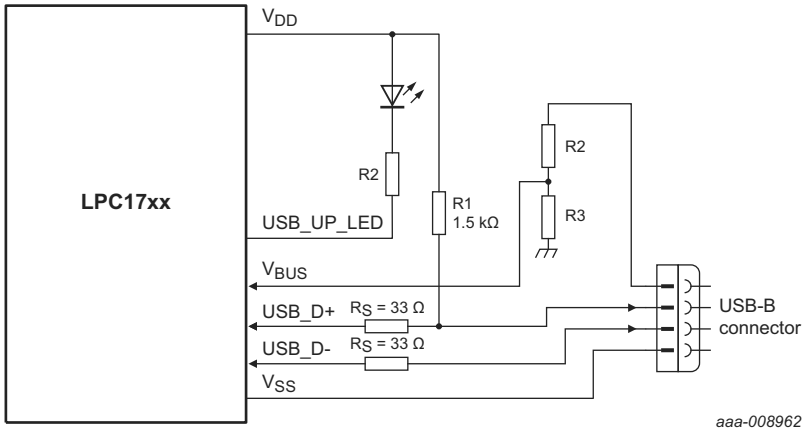


Fig 31. USB interface on a bus-powered device where V_{BUS} = 5 V, V_{DD} not present

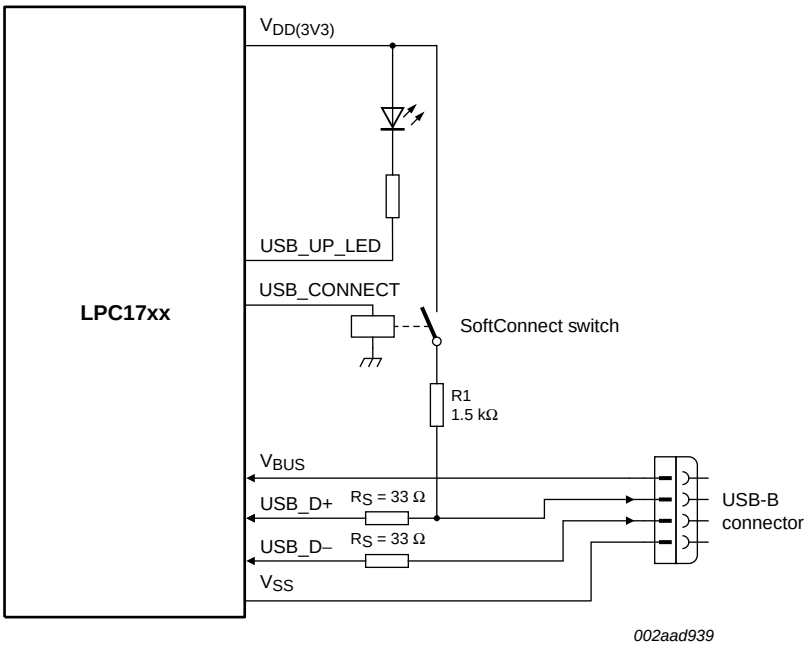


Fig 32. USB interface with soft-connect

order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Values of C_{x1} and C_{x2} should be chosen smaller accordingly to the increase in parasitics of the PCB layout.

15.4 Standard I/O pin configuration

Figure 38 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver: Open-drain mode enabled/disabled
- Digital input: Pull-up enabled/disabled
- Digital input: Pull-down enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Analog input

The default configuration for standard I/O pins is input with pull-up enabled. The weak MOS devices provide a drive capability equivalent to pull-up and pull-down resistors.

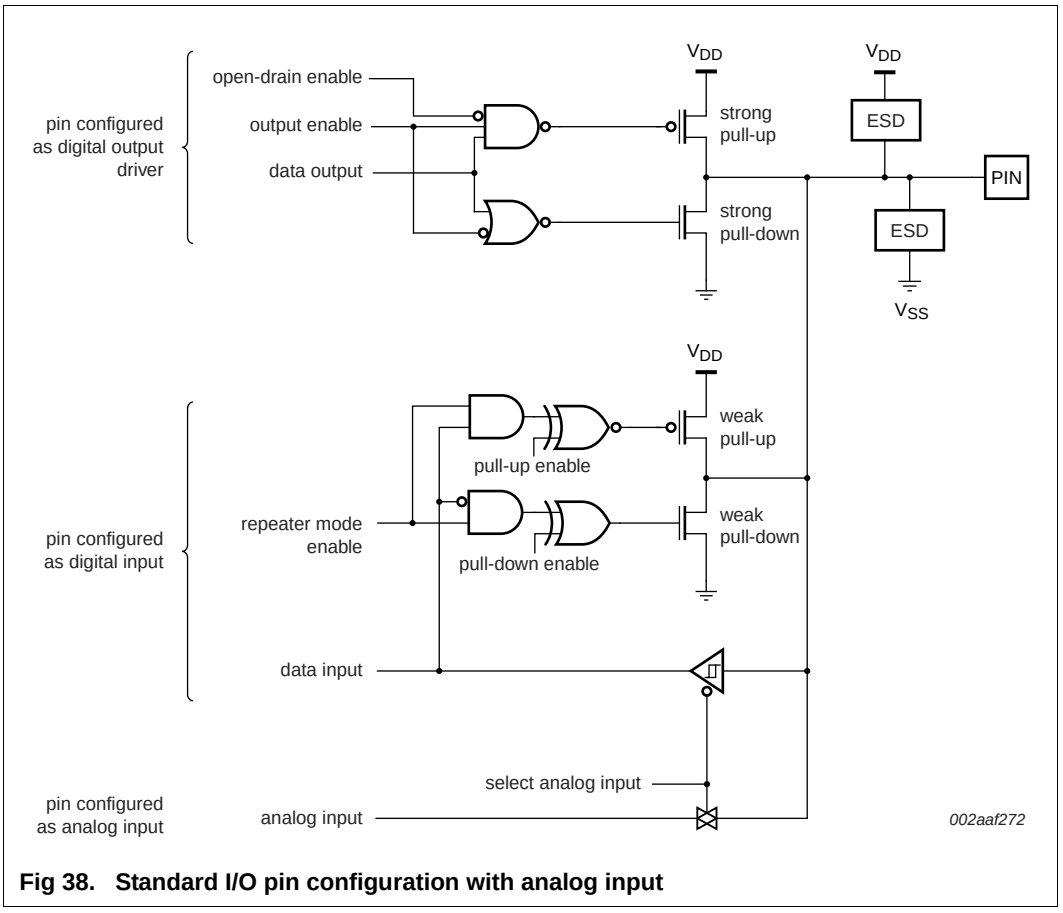
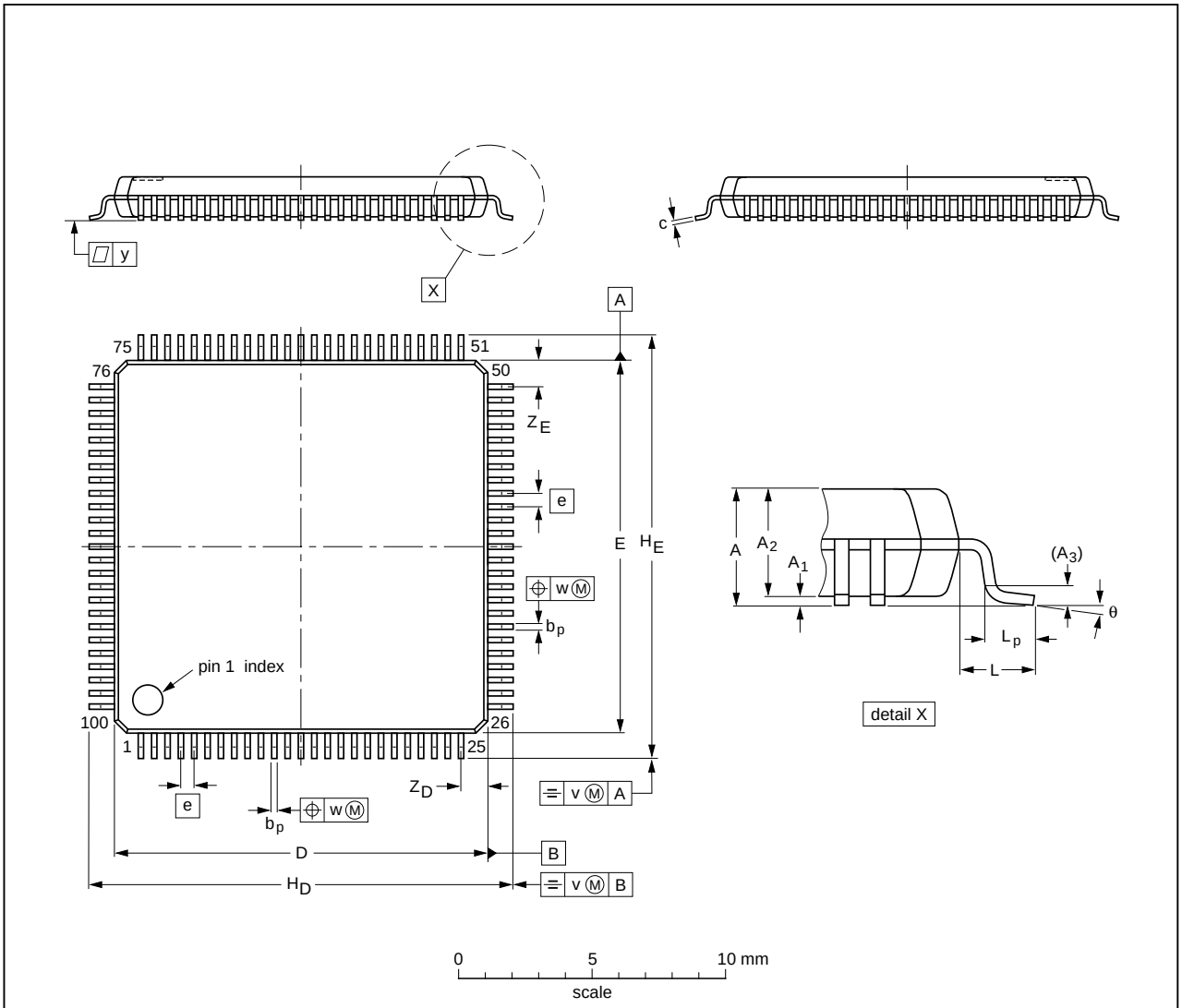


Fig 38. Standard I/O pin configuration with analog input

16. Package outline

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm **SOT407-1**



DIMENSIONS (mm are the original dimensions)

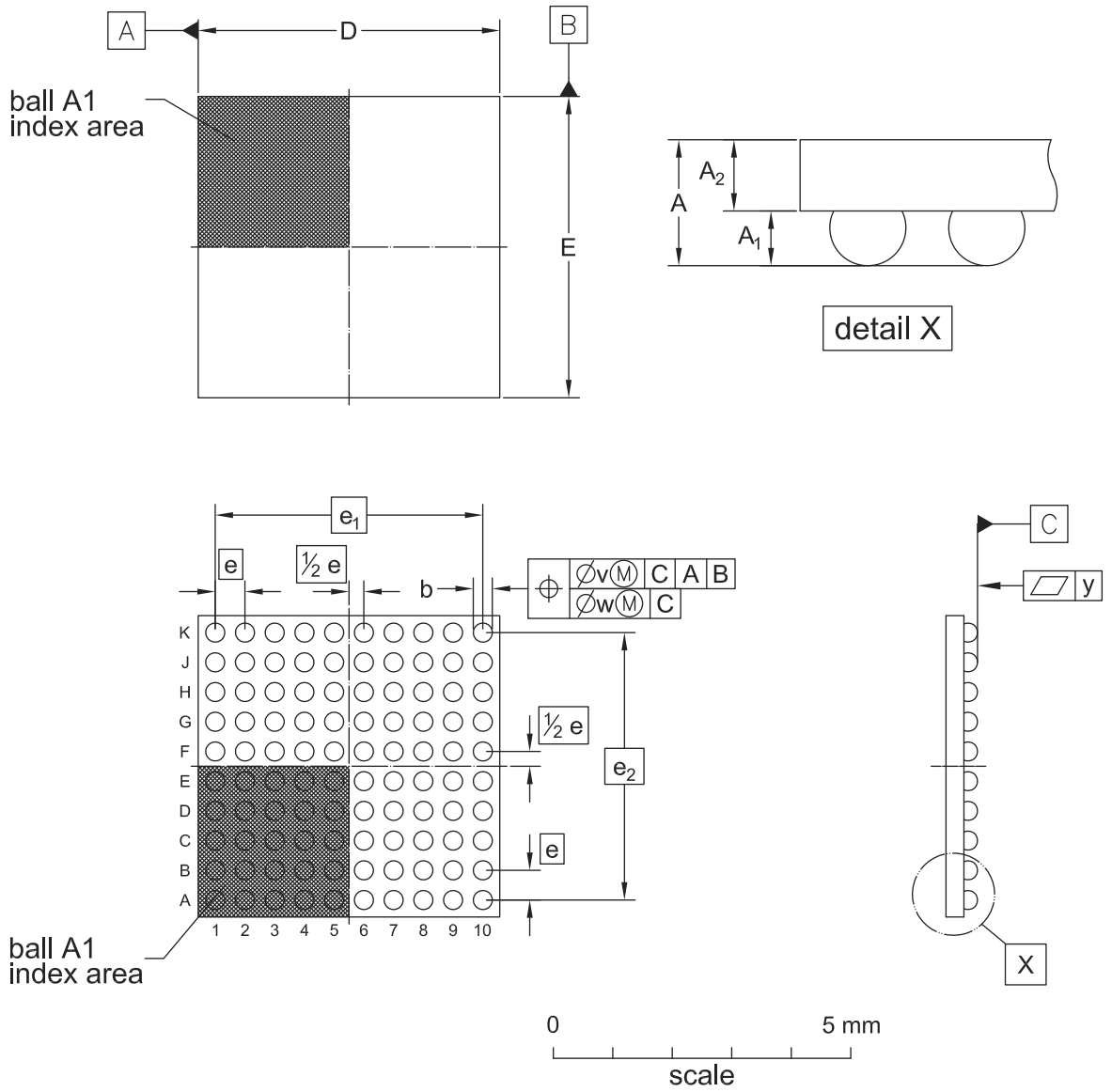
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1	0.75 0.45	0.2	0.08	0.08	1.15 0.85	1.15 0.85	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT407-1	136E20	MS-026				~~00-02-01~~ 03-02-20

Fig 40. Package outline SOT407-1 (LQFP100)

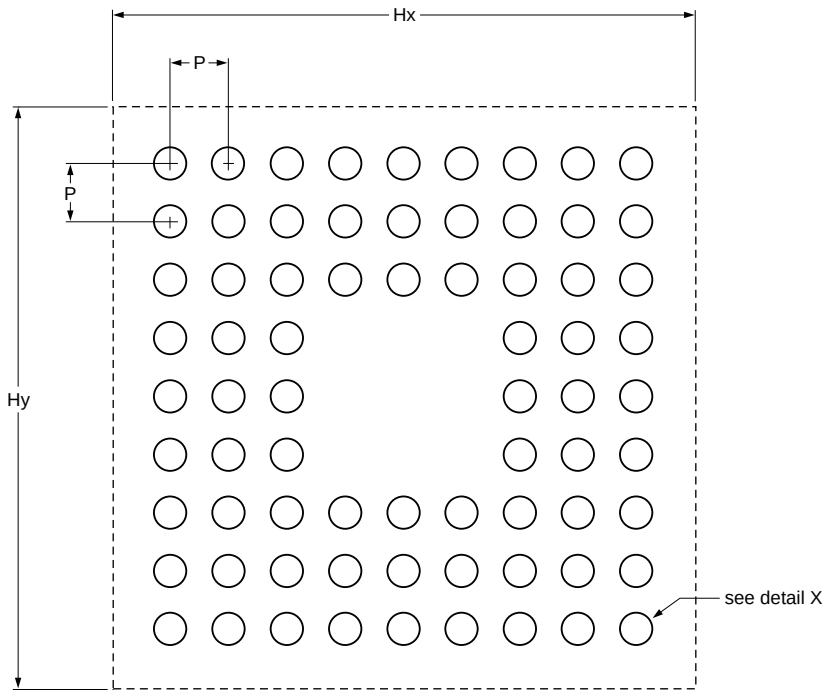


DIMENSIONS (mm are the original dimensions)

UNIT		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
mm	MAX	0.57	0.26	0.325	0.35	5.10	5.10	0.5	4.5	4.5	0.15	0.05	0.03
	NOM	0.53	0.23	0.300	0.32	5.07	5.07						
	MIN	0.49	0.20	0.275	0.29	5.04	5.04						

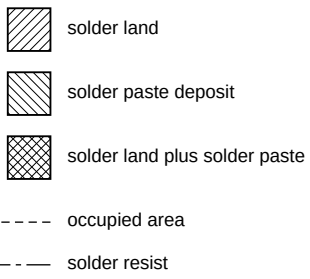
Fig 42. Package outline SOT1450-2 LPC1768UK (WLCSP100)

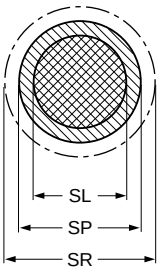
Footprint information for reflow soldering of TFBGA100 package **SOT926-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout





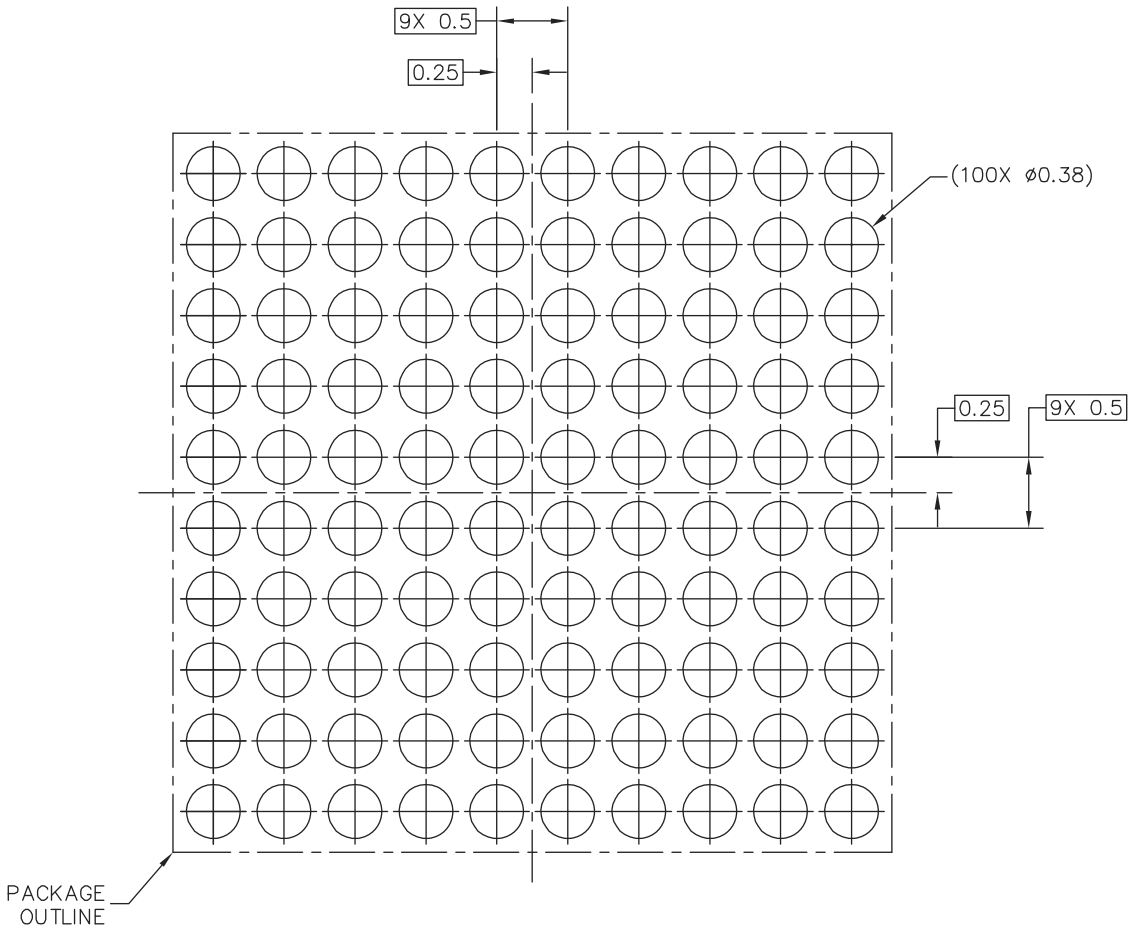
detail X

DIMENSIONS in mm

P	SL	SP	SR	Hx	Hy
0.80	0.330	0.400	0.480	9.400	9.400

sot926-1_fr

Fig 44. Reflow soldering of the TFBGA100 package



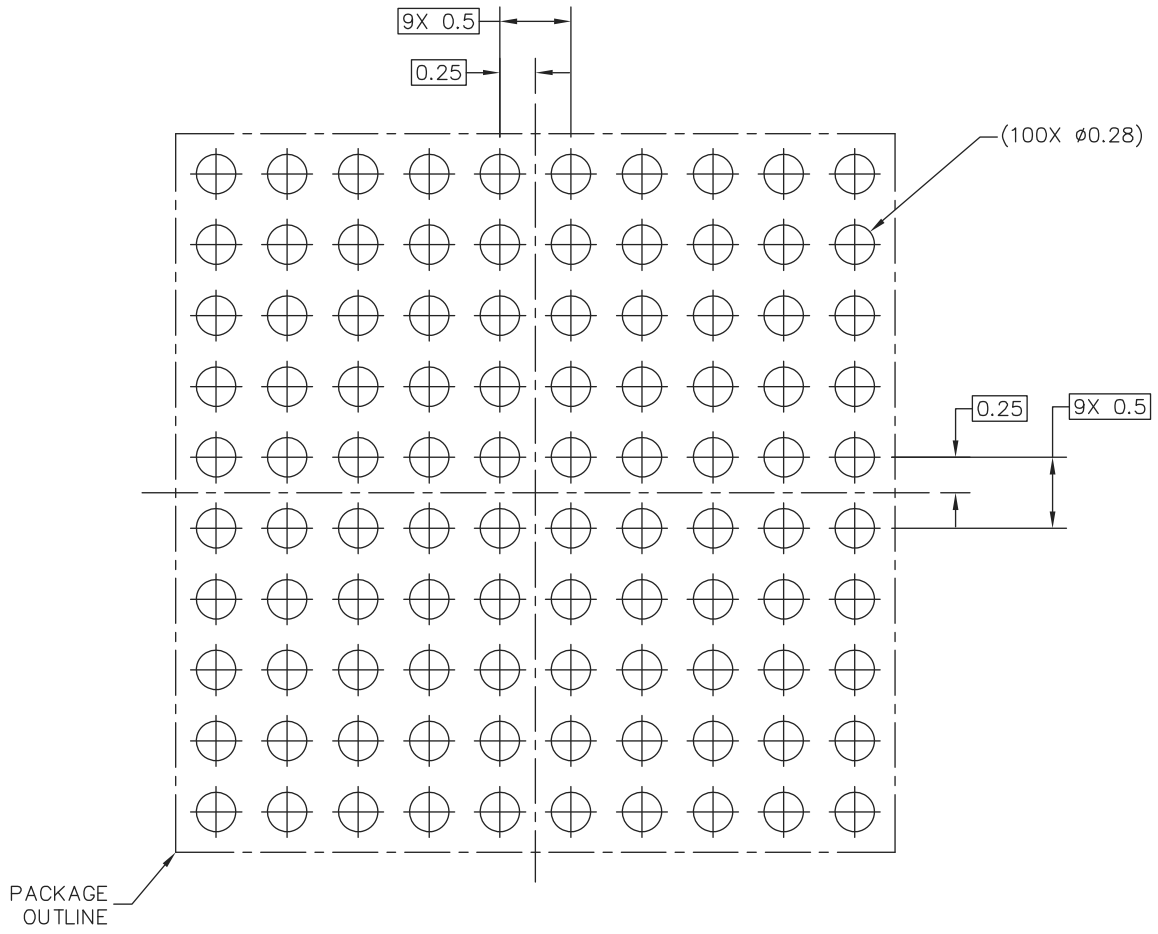
PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

DATE: 06 MAR 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: SOT1450–2	REVISION: 0	

Fig 45. Reflow soldering of the WLCSP100 package (part 1)



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

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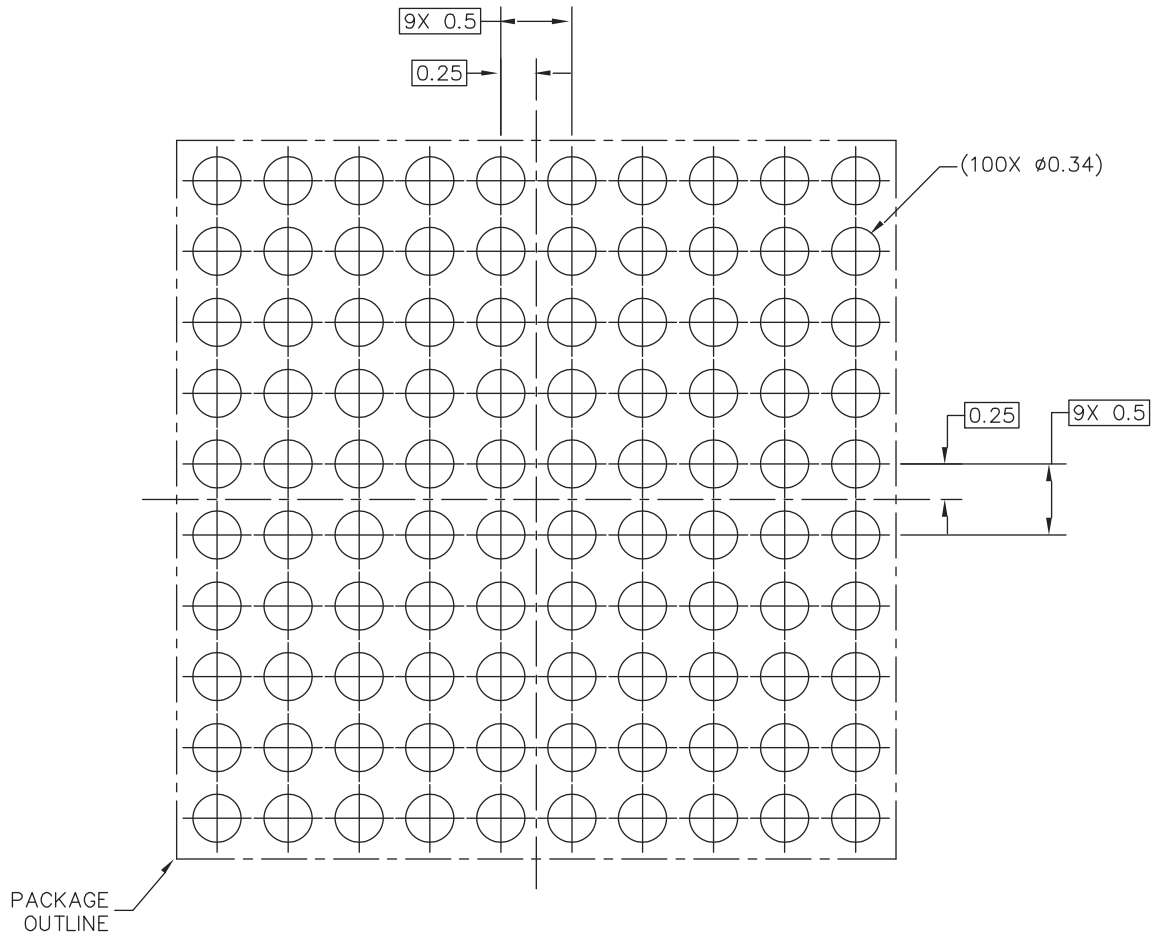
 DATE: 06 MAR 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: SOT1450-2	REVISION: 0	

Fig 46. Reflow soldering of the WLCSP100 package (part 2)



RECOMMENDED STENCIL THICKNESS 0.125

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

 DATE: 06 MAR 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: SOT1450–2	REVISION: 0	

Fig 47. Reflow soldering of the WLCSP100 package (part 3)

Table 27. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC1769_68_67_66_65_64_63 v.9.2	20131021	Product data sheet	-	LPC1769_68_67_66_65_64 v.9.1
Modifications:	• Table 8 “Static characteristics”: – Added Table note 3 “VDDA and VREFP should be tied to VDD(3V3) if the ADC and DAC are not used.” – Added Table note 4 “VDDA for DAC specs are from 2.7 V to 3.6 V.” – V_{DDA}/VREFP spec changed from 2.7 V to 2.5 V. • Table 19 “ADC characteristics (full resolution)”: – Added Table note 1 “VDDA and VREFP should be tied to VDD(3V3) if the ADC and DAC are not used.” – V_{DDA} changed from 2.7 V to 2.5 V. • Table 20 “ADC characteristics (lower resolution)”: Added Table note 1 “VDDA and VREFP should be tied to VDD(3V3) if the ADC and DAC are not used.”			
LPC1769_68_67_66_65_64_63 v.9.1	20130916	Product data sheet	-	LPC1769_68_67_66_65_64 v.9
Modifications:	• Added Table 7 “Thermal resistance”. • Table 6 “Limiting values”: – Updated min/max values for $V_{DD(3V3)}$ and $V_{DD(REG)(3V3)}$. – Updated conditions for V_I. – Updated table notes. • Table 8 “Static characteristics”: Added Table note 15 “TCK/SWDCLK pin needs to be externally pulled LOW.” • Updated Section 15.1 “Suggested USB interface solutions”. • Added Section 5 “Marking”. • Changed title of Figure 31 from “USB interface on a self-powered device” to “USB interface with soft-connect”.			
LPC1769_68_67_66_65_64_63 v.9	20120810	Product data sheet	-	LPC1769_68_67_66_65_64 v.8
Modifications:	• Remove table note “The peak current is limited to 25 times the corresponding maximum current.” from Table 5 “Limiting values”. • Change $V_{DD(3V3)}$ to $V_{DD(REG)(3V3)}$ in Section 11.3 “Internal oscillators”. • Glitch filter constant changed to 10 ns in Table note 6 in Table 4. • Description of $\overline{\text{RESET}}$ function updated in Table 4. • Pull-up value added for GPIO pins in Table 4. • Pin configuration diagram for LQFP100 package corrected (Figure 2).			
LPC1769_68_67_66_65_64_63 v.8	20111114	Product data sheet	-	LPC1769_68_67_66_65_64 v.7
Modifications:	• Pin description of USB_UP_LED pin updated in Table 4. • R_{i1} and R_{i2} labels in Figure 27 updated. • Part LPC1765FET100 added. • Table note 10 updated in Table 4. • Table note 1 updated in Table 12. • Pin description of STCLK pin updated in Table 4. • Electromagnetic compatibility data added in Section 14.6. • Section 16 added.			

Table 27. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC1769_68_67_66_65_64_63 v.7	20110405	Product data sheet	-	LPC1769_68_67_66_65_64 v.6
Modifications:	• Pin description of pins P0[29] and P0[30] updated in Table note 5 of Table 4. Pins are not 5 V tolerant. • Typical value for Parameter N_{endu} added in Table 9. • Parameter V_{hys} for I^2C bus pins: typical value corrected $V_{hys} = 0.05V_{DD(3V3)}$ in Table 7. • Condition 3.0 V ≤ $V_{DD(3V3)}$ ≤ 3.6 V added in Table 16. • Typical values for parameters $I_{DD(REG)(3V3)}$ and I_{BAT} with condition Deep power-down mode corrected in Table 7 and Table note 9, Table note 10, and Table note 11 updated. • For Deep power-down mode, Figure 9 updated and Figure 10 added.			
LPC1769_68_67_66_65_64_63 v.6	20100825	Product data sheet	-	LPC1769_68_67_66_65_64 v.5
Modifications:	• Part LPC1768TFBGA added. • Section 7.30.2; BOD level corrected. • Added Section 10.2.			
LPC1769_68_67_66_65_64_63 v.5	20100716	Product data sheet	-	LPC1769_68_67_66_65_64 v.4
LPC1769_68_67_66_65_64 v.4	20100201	Product data sheet	-	LPC1768_67_66_65_64 v.3
LPC1768_67_66_65_64 v.3	20091119	Product data sheet	-	LPC1768_66_65_64 v.2
LPC1768_66_65_64 v.2	20090211	Objective data sheet	-	LPC1768_66_65_64 v.1
LPC1768_66_65_64 v.1	20090115	Objective data sheet	-	-