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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 100MHz |
| Connectivity | CANbus, Ethernet, I²C, IrDA, Microwire, SPI, SSI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT |
| Number of I/O | 70 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 64K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.4V ~ 3.6V |
| Data Converters | A/D 8x12b; D/A 1x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-TFBGA |
| Supplier Device Package | 100-TFBGA (9x9) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1768fet100y |

**Table 4. Pin allocation table TFBGA100** *…continued*

| Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol |
|---|---|---|---|---|---|---|---|
| **Row J** | | | | | | | |
| 1 | P0[28]/SCL0/ USB_SCL | 2 | P0[27]/SDA0/ USB_SDA | 3 | P0[29]/USB_D+ | 4 | P1[19]/MCOA0/ USB_PPWR/ CAP1[1] |
| 5 | P1[22]/MCOB0/ USB_PWRD/ MAT1[0] | 6 | $V_{SS}$ | 7 | P1[28]/MCOA2/ PCAP1[0]/ MAT0[0] | 8 | P0[1]/TD1/RXD3/SCL1 |
| 9 | P2[13]/EINT3/ I2STX_SDA | 10 | P2[10]/EINT0/NMI | 11 | - | 12 | - |
| **Row K** | | | | | | | |
| 1 | P3[26]/STCLK/ MAT0[1]/PWM1[3] | 2 | $V_{DD(3V3)}$ | 3 | $V_{SS}$ | 4 | P1[20]/MCI0/ PWM1[2]/SCK0 |
| 5 | P1[23]/MCI1/ PWM1[4]/MISO0 | 6 | P1[26]/MCOB1/ PWM1[6]/CAP0[0] | 7 | P1[27]/CLKOUT /USB_OVRCR/ CAP0[1] | 8 | P0[0]/RD1/TXD3/SDA1 |
| 9 | P0[11]/RXD2/ SCL2/MAT3[1] | 10 | P2[12]/EINT2/ I2STX_WS | 11 | - | 12 | - |

## 7.2 Pin description

**Table 5. Pin description**

| Symbol | Pin/ball | | | | Type | Description |
|---|---|---|---|---|---|---|
| | LQFP100 | TFBGA100 | WLCSP100 | | | |
| P0[0] to P0[31] | | | | | I/O | **Port 0:** Port 0 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 0 pins depends upon the pin function selected via the pin connect block. Pins 12, 13, 14, and 31 of this port are not available. |
| P0[0]/RD1/TXD3/ SDA1 | 46 | K8 | H10 | [1] | I/O | **P0[0] —** General purpose digital input/output pin. |
| | | | | | I | **RD1 —** CAN1 receiver input. (LPC1769/68/66/65/64 only). |
| | | | | | O | **TXD3 —** Transmitter output for UART3. |
| | | | | | I/O | **SDA1 —** $I^2C1$ data input/output. (This is not an $I^2C$-bus compliant open-drain pin). |
| P0[1]/TD1/RXD3/ SCL1 | 47 | J8 | H9 | [1] | I/O | **P0[1] —** General purpose digital input/output pin. |
| | | | | | O | **TD1 —** CAN1 transmitter output. (LPC1769/68/66/65/64 only). |
| | | | | | I | **RXD3 —** Receiver input for UART3. |
| | | | | | I/O | **SCL1 —** $I^2C1$ clock input/output. (This is not an $I^2C$-bus compliant open-drain pin). |
| P0[2]/TXD0/AD0[7] | 98 | C4 | B1 | [2] | I/O | **P0[2] —** General purpose digital input/output pin. |
| | | | | | O | **TXD0 —** Transmitter output for UART0. |
| | | | | | I | **AD0[7] —** A/D converter 0, input 7. |
| P0[3]/RXD0/AD0[6] | 99 | A2 | C3 | [2] | I/O | **P0[3] —** General purpose digital input/output pin. |
| | | | | | I | **RXD0 —** Receiver input for UART0. |
| | | | | | I | **AD0[6] —** A/D converter 0, input 6. |

**Table 5. Pin description** *…continued*

| Symbol | Pin/ball | | | | Type | Description |
|---|---|---|---|---|---|---|
| | LQFP100 | TFBGA100 | WLCSP100 | | | |
| P2[11]/$\overline{\text{EINT1}}$/ I2STX_CLK | 52 | H8 | J8 | [6] | I/O | **P2[11] —** General purpose digital input/output pin. |
| | | | | | I | **$\overline{\text{EINT1}}$ —** External interrupt 1 input. |
| | | | | | I/O | **I2STX_CLK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *$I^2S$-bus specification*. (LPC1769/68/67/66/65/63 only). |
| P2[12]/$\overline{\text{EINT2}}$/ I2STX_WS | 51 | K10 | K10 | [6] | I/O | **P2[12] —** General purpose digital input/output pin. |
| | | | | | I | **$\overline{\text{EINT2}}$ —** External interrupt 2 input. |
| | | | | | I/O | **I2STX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *$I^2S$-bus specification*. (LPC1769/68/67/66/65/63 only). |
| P2[13]/$\overline{\text{EINT3}}$/ I2STX_SDA | 50 | J9 | J9 | [6] | I/O | **P2[13] —** General purpose digital input/output pin. |
| | | | | | I | **$\overline{\text{EINT3}}$ —** External interrupt 3 input. |
| | | | | | I/O | **I2STX_SDA —** Transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *$I^2S$-bus specification*. (LPC1769/68/67/66/65/63 only). |
| P3[0] to P3[31] | | | | | I/O | **Port 3:** Port 3 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 3 pins depends upon the pin function selected via the pin connect block. Pins 0 through 24, and 27 through 31 of this port are not available. |
| P3[25]/MAT0[0]/ PWM1[2] | 27 | H3 | D8 | [1] | I/O | **P3[25] —** General purpose digital input/output pin. |
| | | | | | O | **MAT0[0] —** Match output for Timer 0, channel 0. |
| | | | | | O | **PWM1[2] —** Pulse Width Modulator 1, output 2. |
| P3[26]/STCLK/ MAT0[1]/PWM1[3] | 26 | K1 | A10 | [1] | I/O | **P3[26] —** General purpose digital input/output pin. |
| | | | | | I | **STCLK —** System tick timer clock input. The maximum STCLK frequency is 1/4 of the Arm processor clock frequency CCLK. |
| | | | | | O | **MAT0[1] —** Match output for Timer 0, channel 1. |
| | | | | | O | **PWM1[3] —** Pulse Width Modulator 1, output 3. |
| P4[0] to P4[31] | | | | | I/O | **Port 4:** Port 4 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 4 pins depends upon the pin function selected via the pin connect block. Pins 0 through 27, 30, and 31 of this port are not available. |
| P4[28]/RX_MCLK/ MAT2[0]/TXD3 | 82 | C7 | G1 | [1] | I/O | **P4[28] —** General purpose digital input/output pin. |
| | | | | | O | **RX_MCLK —** $I^2S$ receive master clock. (LPC1769/68/67/66/65 only). |
| | | | | | O | **MAT2[0] —** Match output for Timer 2, channel 0. |
| | | | | | O | **TXD3 —** Transmitter output for UART3. |
| P4[29]/TX_MCLK/ MAT2[1]/RXD3 | 85 | E6 | F1 | [1] | I/O | **P4[29] —** General purpose digital input/output pin. |
| | | | | | O | **TX_MCLK —** $I^2S$ transmit master clock. (LPC1769/68/67/66/65 only). |
| | | | | | O | **MAT2[1] —** Match output for Timer 2, channel 1. |
| | | | | | I | **RXD3 —** Receiver input for UART3. |

The MPU allows separating processing tasks by disallowing access to each other's data, disabling access to memory regions, allowing memory regions to be defined as read-only and detecting unexpected memory accesses that could potentially break the system.

The MPU separates the memory into distinct regions and implements protection by preventing disallowed accesses. The MPU supports up to 8 regions each of which can be divided into 8 subregions. Accesses to memory locations that are not defined in the MPU regions, or not permitted by the region setting, will cause the Memory Management Fault exception to take place.

## 8.6 Memory map

The LPC17xx incorporates several distinct memory regions, shown in the following figures. Figure 5 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB peripheral area is 2 MB in size and is divided to allow for up to 128 peripherals. The APB peripheral area is 1 MB in size and is divided to allow for up to 64 peripherals. Each peripheral of either type is allocated 16 kB of space. This allows simplifying the address decoding for each peripheral.

- Enhanced Ethernet features:
  - Receive filtering.
  - Multicast and broadcast frame support for both transmit and receive.
  - Optional automatic Frame Check Sequence (FCS) insertion with Cyclic Redundancy Check (CRC) for transmit.
  - Selectable automatic transmit frame padding.
  - Over-length frame support for both transmit and receive allows any length frames.
  - Promiscuous receive mode.
  - Automatic collision back-off and frame retransmission.
  - Includes power management by clock switching.
  - Wake-on-LAN power management support allows system wake-up: using the receive filters or a magic frame detection filter.
- Physical interface:
  - Attachment of external PHY chip through standard RMII interface.
  - PHY register access is available via the MIIM interface.

## 8.12 USB interface

**Remark:** The USB controller is available as device/Host/OTG controller on parts LPC1769/68/66/65 and as device-only controller on part LPC1764.

The Universal Serial Bus (USB) is a 4-wire bus that supports communication between a host and one or more (up to 127) peripherals. The host controller allocates the USB bandwidth to attached devices through a token-based protocol. The bus supports hot plugging and dynamic configuration of the devices. All transactions are initiated by the host controller.

The USB interface includes a device, Host, and OTG controller with on-chip PHY for device and Host functions. The OTG switching protocol is supported through the use of an external controller. Details on typical USB interfacing solutions can be found in Section 15.1.

### 8.12.1 USB device controller

The device controller enables 12 Mbit/s data exchange with a USB Host controller. It consists of a register interface, serial interface engine, endpoint buffer memory, and a DMA controller. The serial interface engine decodes the USB data stream and writes data to the appropriate endpoint buffer. The status of a completed USB transfer or error condition is indicated via status registers. An interrupt is also generated if enabled. When enabled, the DMA controller transfers data between the endpoint buffer and the on-chip SRAM.

#### 8.12.1.1 Features

- Fully compliant with *USB 2.0 specification (full speed)*.
- Supports 32 physical (16 logical) endpoints with a 4 kB endpoint buffer RAM.
- Supports Control, Bulk, Interrupt and Isochronous endpoints.
- Scalable realization of endpoints at run time.

- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- Up to two match registers can be used to generate timed DMA requests.

## 8.22 Pulse width modulator

The PWM is based on the standard Timer block and inherits all of its features, although only the PWM function is pinned out on the LPC17xx. The Timer is designed to count cycles of the system derived clock and optionally switch pins, generate interrupts or perform other actions when specified timer values occur, based on seven match registers. The PWM function is in addition to these features, and is based on match register events.

The ability to separately control rising and falling edge locations allows the PWM to be used for more applications. For instance, multi-phase motor control typically requires three non-overlapping PWM outputs with individual control of all three pulse widths and positions.

Two match registers can be used to provide a single edge controlled PWM output. One match register (PWMMR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an PWMMR0 match occurs.

Three match registers can be used to provide a PWM output with both edges controlled. Again, the PWMMR0 match register controls the PWM cycle rate. The other match registers control the two PWM edge positions. Additional double edge controlled PWM outputs require only two match registers each, since the repetition rate is the same for all PWM outputs.

With double edge controlled PWM outputs, specific match registers control the rising and falling edge of the output. This allows both positive going PWM pulses (when the rising edge occurs prior to the falling edge), and negative going PWM pulses (when the falling edge occurs prior to the rising edge).

### 8.22.1 Features

- One PWM block with Counter or Timer operation (may use the peripheral clock or one of the capture inputs as the clock source).
- Seven match registers allow up to 6 single edge controlled or 3 double edge controlled PWM outputs, or a mix of both types. The match registers also allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.

### 8.29.2 Main PLL (PLL0)

The PLL0 accepts an input clock frequency in the range of 32 kHz to 25 MHz. The input frequency is multiplied up to a high frequency, then divided down to provide the actual clock used by the CPU and/or the USB block.

The PLL0 input, in the range of 32 kHz to 25 MHz, may initially be divided down by a value ‘N’, which may be in the range of 1 to 256. This input division provides a wide range of output frequencies from the same input frequency.

Following the PLL0 input divider is the PLL0 multiplier. This can multiply the input divider output through the use of a Current Controlled Oscillator (CCO) by a value ‘M’, in the range of 1 through 32768. The resulting frequency must be in the range of 275 MHz to 550 MHz. The multiplier works by dividing the CCO output by the value of M, then using a phase-frequency detector to compare the divided CCO output to the multiplier input. The error value is used to adjust the CCO frequency.

The PLL0 is turned off and bypassed following a chip Reset and by entering Power-down mode. PLL0 is enabled by software only. The program must configure and activate the PLL0, wait for the PLL0 to lock, and then connect to the PLL0 as a clock source.

### 8.29.3 USB PLL (PLL1)

The LPC17xx contain a second, dedicated USB PLL1 to provide clocking for the USB interface.

The PLL1 receives its clock input from the main oscillator only and provides a fixed 48 MHz clock to the USB block only. The PLL1 is disabled and powered off on reset. If the PLL1 is left disabled, the USB clock will be supplied by the 48 MHz clock from the main PLL0.

The PLL1 accepts an input clock frequency in the range of 10 MHz to 25 MHz only. The input frequency is multiplied up the range of 48 MHz for the USB clock using a Current Controlled Oscillators (CCO). It is insured that the PLL1 output has a 50 % duty cycle.

### 8.29.4 RTC clock output

The LPC17xx feature a clock output function intended for synchronizing with external devices and for use during system development to allow checking the internal clocks CCLK, IRC clock, main crystal, RTC clock, and USB clock in the outside world. The RTC clock output allows tuning the RTC frequency without probing the pin, which would distort the results.

### 8.29.5 Wake-up timer

The LPC17xx begin operation at power-up and when awakened from Power-down mode by using the 4 MHz IRC oscillator as the clock source. This allows chip operation to resume quickly. If the main oscillator or the PLL is needed by the application, software will need to enable these features and wait for them to stabilize before they are used as a clock source.

When the main oscillator is initially activated, the wake-up timer allows software to ensure that the main oscillator is fully functional before the processor uses it as a clock source and starts to execute instructions. This is important at power on, all types of Reset, and

### 8.30.5 AHB multilayer matrix

The LPC17xx use an AHB multilayer matrix. This matrix connects the instruction (I-code) and data (D-code) CPU buses of the Arm Cortex-M3 to the flash memory, the main (32 kB) static RAM, and the Boot ROM. The GPDMA can also access all of these memories. The peripheral DMA controllers, Ethernet, and USB can access all SRAM blocks. Additionally, the matrix connects the CPU system bus and all of the DMA controllers to the various peripheral functions.

### 8.30.6 External interrupt inputs

The LPC17xx include up to 46 edge sensitive interrupt inputs combined with up to four level sensitive external interrupt inputs as selectable pin functions. The external interrupt inputs can optionally be used to wake up the processor from Power-down mode.

### 8.30.7 Memory mapping control

The Cortex-M3 incorporates a mechanism that allows remapping the interrupt vector table to alternate locations in the memory map. This is controlled via the Vector Table Offset Register contained in the NVIC.

The vector table may be located anywhere within the bottom 1 GB of Cortex-M3 address space. The vector table must be located on a 128 word (512 byte) boundary because the NVIC on the LPC17xx is configured for 128 total interrupts.

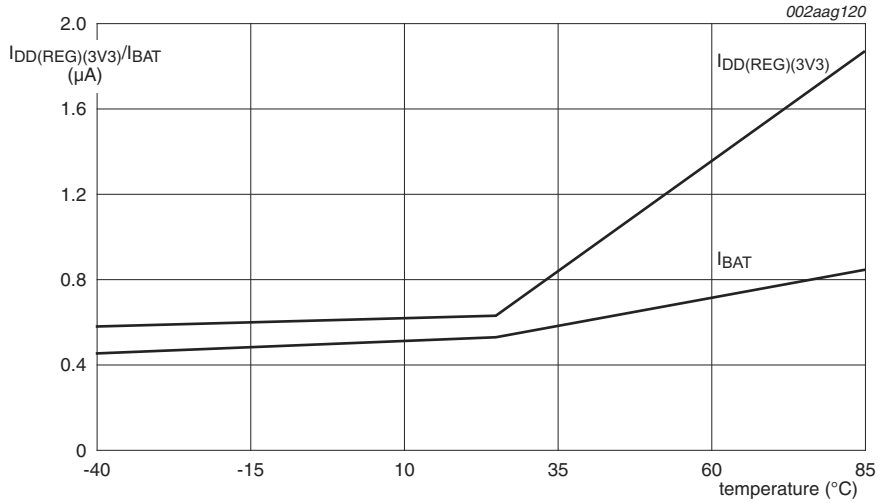
## 8.31 Emulation and debugging

Debug and trace functions are integrated into the Arm Cortex-M3. Serial wire debug and trace functions are supported in addition to a standard JTAG debug and parallel trace functions. The Arm Cortex-M3 is configured to support up to eight breakpoints and four watch points.

**Table 8. Static characteristics** *…continued*

*$T_{amb}$ = −40 °C to +85 °C, unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD(ADC)}$ | ADC supply current | active mode; ADC powered | [16][17] | - | 1.95 | - | mA |
| | | ADC in Power-down mode | [16][18] | - | <0.2 | - | μA |
| | | deep sleep mode | [16] | - | 38 | - | nA |
| | | power-down mode | [16] | - | 38 | - | nA |
| | | deep power-down mode | [16] | - | 24 | - | nA |
| $I_{I(ADC)}$ | ADC input current | on pin VREFP | | | | | |
| | | deep sleep mode | [19] | - | 100 | - | nA |
| | | power-down mode | [19] | - | 100 | - | nA |
| | | deep power-down mode | [19] | - | 100 | - | nA |
| **Standard port pins, $\overline{\text{RESET}}$, RTCK** | | | | | | | |
| $I_{IL}$ | LOW-level input current | $V_I$ = 0 V; on-chip pull-up resistor disabled | | - | 0.5 | 10 | nA |
| $I_{IH}$ | HIGH-level input current | $V_I = V_{DD(3V3)}$; on-chip pull-down resistor disabled | | - | 0.5 | 10 | nA |
| $I_{OZ}$ | OFF-state output current | $V_O$ = 0 V; $V_O = V_{DD(3V3)}$; on-chip pull-up/down resistors disabled | | - | 0.5 | 10 | nA |
| $V_I$ | input voltage | pin configured to provide a digital function | [20][21][22] | 0 | - | 5.0 | V |
| $V_O$ | output voltage | output active | | 0 | - | $V_{DD(3V3)}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | | $0.7V_{DD(3V3)}$ | - | - | V |
| $V_{IL}$ | LOW-level input voltage | | | - | - | $0.3V_{DD(3V3)}$ | V |
| $V_{hys}$ | hysteresis voltage | | | 0.4 | - | - | V |
| $V_{OH}$ | HIGH-level output voltage | $I_{OH}$ = −4 mA | | $V_{DD(3V3)} - 0.4$ | - | - | V |
| $V_{OL}$ | LOW-level output voltage | $I_{OL}$ = 4 mA | | - | - | 0.4 | V |
| $I_{OH}$ | HIGH-level output current | $V_{OH} = V_{DD(3V3)} - 0.4$ V | | −4 | - | - | mA |
| $I_{OL}$ | LOW-level output current | $V_{OL}$ = 0.4 V | | 4 | - | - | mA |
| $I_{OHS}$ | HIGH-level short-circuit output current | $V_{OH}$ = 0 V | [23] | - | - | −45 | mA |
| $I_{OLS}$ | LOW-level short-circuit output current | $V_{OL} = V_{DD(3V3)}$ | [23] | - | - | 50 | mA |
| $I_{pd}$ | pull-down current | $V_I$ = 5 V | | 10 | 50 | 150 | μA |
| $I_{pu}$ | pull-up current | $V_I$ = 0 V | | −15 | −50 | −85 | μA |
| | | $V_{DD(3V3)} < V_I < 5$ V | | 0 | 0 | 0 | μA |




Conditions: $V_{BAT}$ = 3.0 V; $V_{DD(REG)(3V3)}$ = 3.0 V; RTC running.

**Fig 11. Deep power-down mode: Typical regulator supply current $I_{DD(REG)(3V3)}$ and battery supply current $I_{BAT}$ versus temperature**

# 12. Dynamic characteristics

## 12.1 Flash memory

**Table 10. Flash characteristics**

*$T_{amb}$ = −40 °C to +85 °C, unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $N_{endu}$ | endurance | | [1] | 10000 | 100000 | - | cycles |
| $t_{ret}$ | retention time | powered | | 10 | - | - | years |
| | | unpowered | | 20 | - | - | years |
| $t_{er}$ | erase time | sector or multiple consecutive sectors | | 95 | 100 | 105 | ms |
| $t_{prog}$ | programming time | | [2] | 0.95 | 1 | 1.05 | ms |

[1] Number of program/erase cycles.

[2] Programming times are given for writing 256 bytes from RAM to the flash. Data must be written to the flash in blocks of 256 bytes.

## 12.2 External clock

**Table 11. Dynamic characteristic: external clock**

*$T_{amb}$ = −40 °C to +85 °C; $V_{DD(3V3)}$ over specified ranges.*[1]

| Symbol | Parameter | Conditions | | Min | Typ[2] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $f_{osc}$ | oscillator frequency | | | 1 | - | 25 | MHz |
| $T_{cy(clk)}$ | clock cycle time | | | 40 | - | 1000 | ns |
| $t_{CHCX}$ | clock HIGH time | | | $T_{cy(clk)} \times 0.4$ | - | - | ns |
| $t_{CLCX}$ | clock LOW time | | | $T_{cy(clk)} \times 0.4$ | - | - | ns |
| $t_{CLCH}$ | clock rise time | | | - | - | 5 | ns |
| $t_{CHCL}$ | clock fall time | | | - | - | 5 | ns |

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

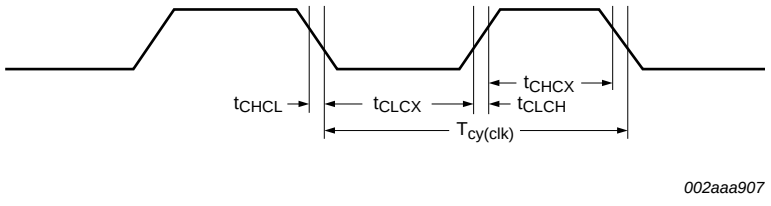



**Fig 16. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)**

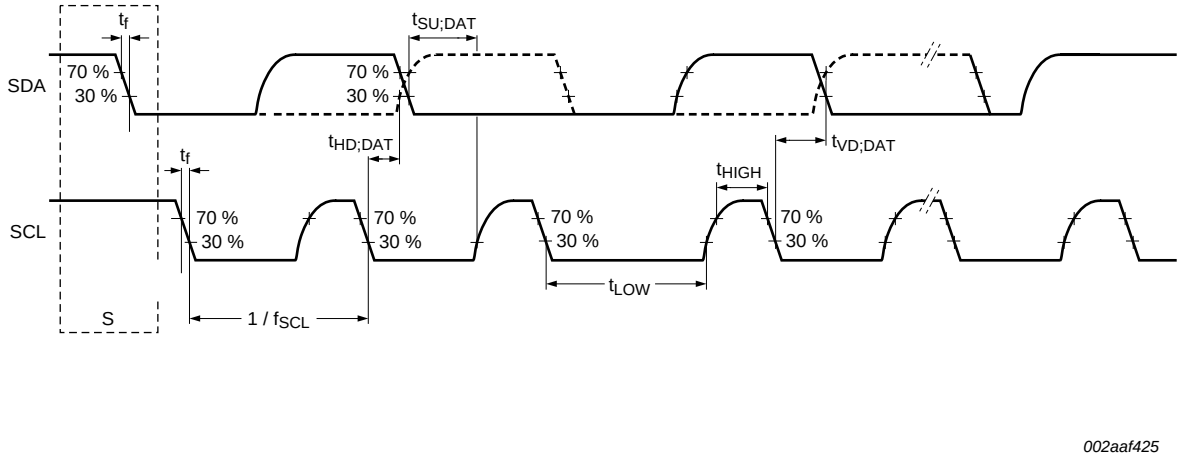



**Fig 18. $I^2C$-bus pins clock timing**

## 12.6 $I^2S$-bus interface

**Remark:** The $I^2S$-bus interface is available on parts LPC1769/68/67/66/65/63. See Table 2.

**Table 15. Dynamic characteristics: $I^2S$-bus interface pins**
*$T_{amb}$ = −40 °C to +85 °C.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **common to input and output** | | | | | | | |
| $t_r$ | rise time | | [1] | - | - | 35 | ns |
| $t_f$ | fall time | | [1] | - | - | 35 | ns |
| $t_{WH}$ | pulse width HIGH | on pins I2STX_CLK and I2SRX_CLK | [1] | 0.495 × $T_{cy(clk)}$ | - | - | - |
| $t_{WL}$ | pulse width LOW | on pins I2STX_CLK and I2SRX_CLK | [1] | - | - | 0.505 × $T_{cy(clk)}$ | ns |
| **output** | | | | | | | |
| $t_{v(Q)}$ | data output valid time | on pin I2STX_SDA | [1] | - | - | 30 | ns |
| | | on pin I2STX_WS | [1] | - | - | 30 | ns |
| **input** | | | | | | | |
| $t_{su(D)}$ | data input set-up time | on pin I2SRX_SDA | [1] | 3.5 | - | - | ns |
| $t_{h(D)}$ | data input hold time | on pin I2SRX_SDA | [1] | 4.0 | - | - | ns |

[1] CCLK = 20 MHz; peripheral clock to the $I^2S$-bus interface PCLK = $CCLK/4$; $I^2S$ clock cycle time $T_{cy(clk)}$ = 1600 ns, corresponds to the SCK signal in the *$I^2S$-bus specification*.

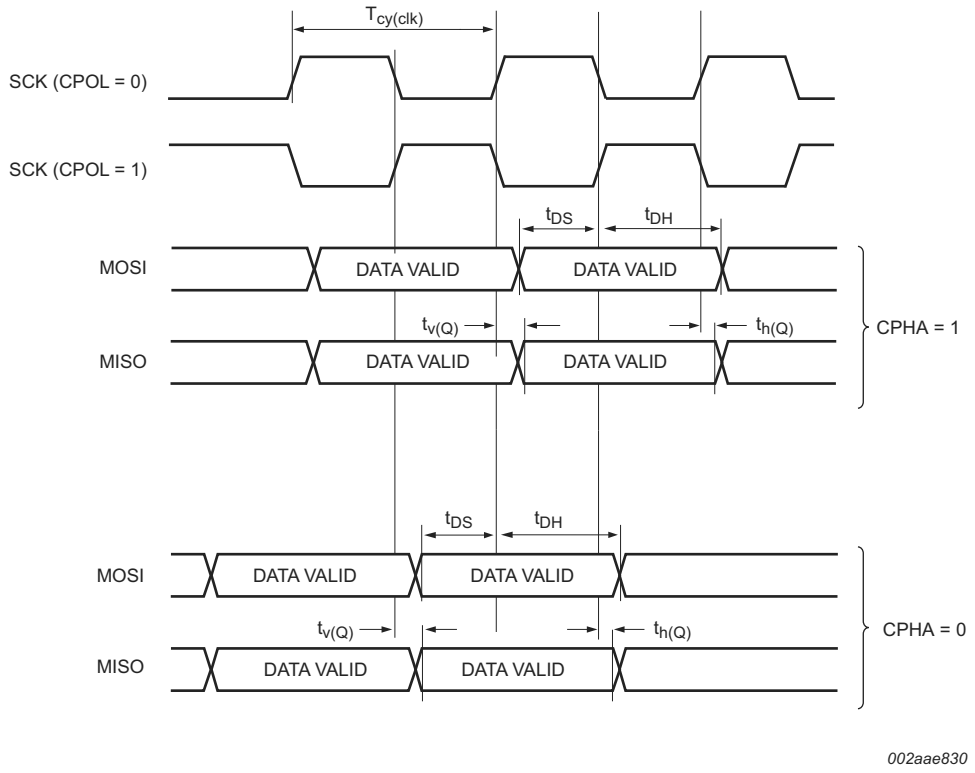
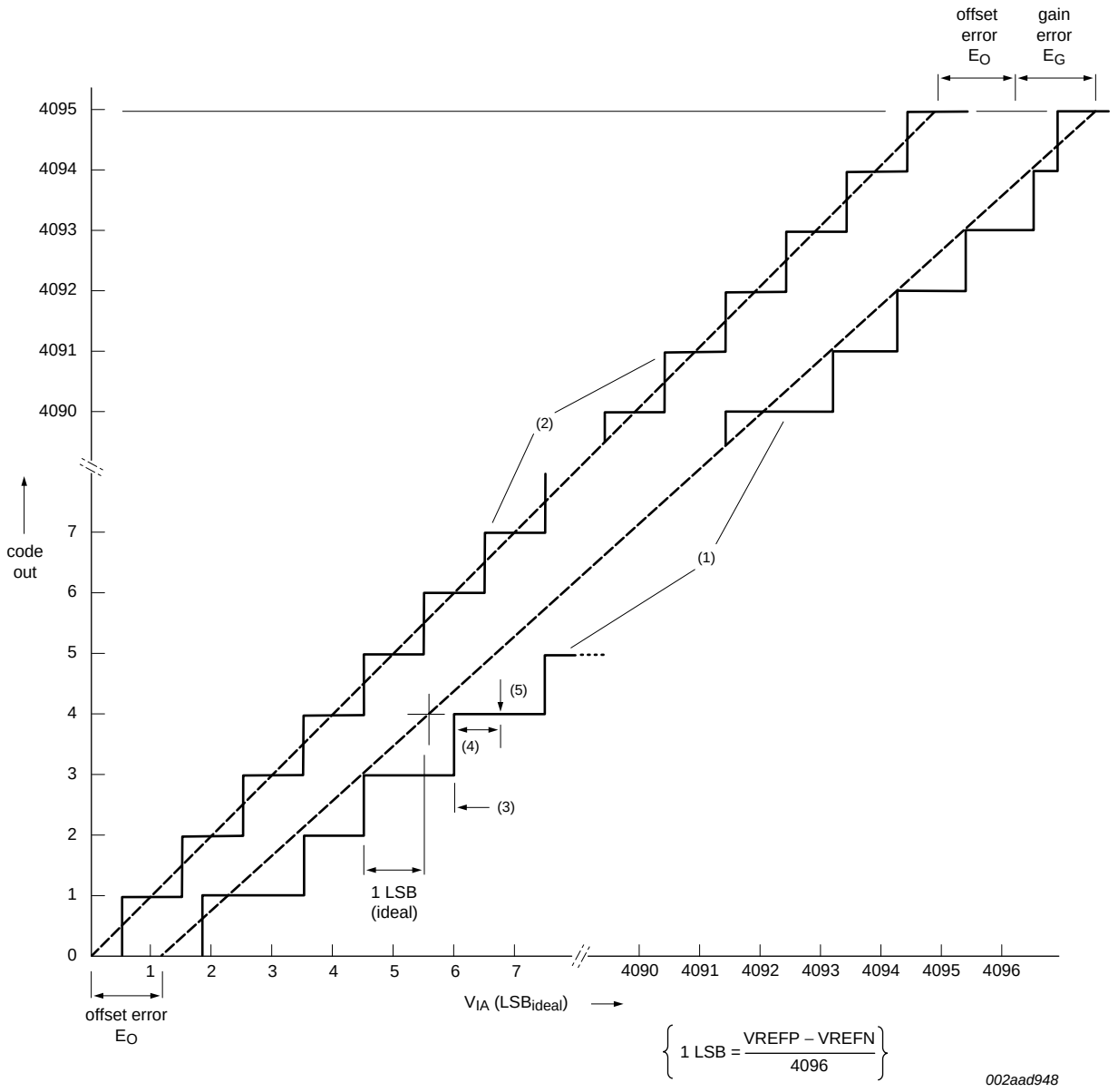



**Fig 22. SSP slave timing in SPI mode**




(1) Example of an actual transfer curve.

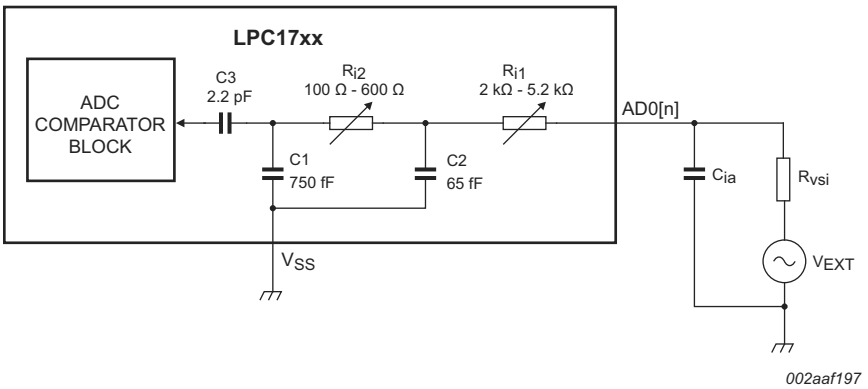
(2) The ideal transfer curve.

(3) Differential linearity error ($E_D$).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

**Fig 28. 12-bit ADC characteristics**




The values of resistor components $R_{i1}$ and $R_{i2}$ vary with temperature and input voltage and are process-dependent (see Table 21).

Parasitic resistance and capacitance from the pad are not included in this figure.

**Fig 29. ADC interface to pins AD0[n]**

**Table 21. ADC interface components**

| Component | Range | Description |
|---|---|---|
| $R_{i1}$ | 2 kΩ to 5.2 kΩ | Switch-on resistance for channel selection switch. Varies with temperature, input voltage, and process. |
| $R_{i2}$ | 100 Ω to 600 Ω | Switch-on resistance for the comparator input switch. Varies with temperature, input voltage, and process. |
| C1 | 750 fF | Parasitic capacitance from the ADC block level. |
| C2 | 65 fF | Parasitic capacitance from the ADC block level. |
| C3 | 2.2 pF | Sampling capacitor. |

# 14. DAC electrical characteristics

**Remark:** The DAC is available on parts LPC1769/68/67/66/65/63. See Table 2.

**Table 22. DAC electrical characteristics**

*$V_{DDA}$ = 2.7 V to 3.6 V; $T_{amb}$ = −40 °C to +85 °C unless otherwise specified*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $E_D$ | differential linearity error | | | - | ±1 | - | LSB |
| $E_{L(adj)}$ | integral non-linearity | | | - | ±1.5 | - | LSB |
| $E_O$ | offset error | | | - | 0.6 | - | % |
| $E_G$ | gain error | | | - | 0.6 | - | % |
| $C_L$ | load capacitance | | | - | 200 | - | pF |
| $R_L$ | load resistance | | | 1 | - | - | kΩ |

# 15. Application information

## 15.1 Suggested USB interface solutions

**Remark:** The USB controller is available as a device/Host/OTG controller on parts LPC1769/68/66/65 and as device-only controller on part LPC1764.

If the LPC1769/68/67/66/65/64/63 $V_{DD}$ is always greater than 0 V while $V_{BUS}$ = 5 V, the $V_{BUS}$ pin can be connected directly to the $V_{BUS}$ pin on the USB connector.

This applies to bus powered devices where the USB cable supplies the system power. For systems where $V_{DD}$ can be 0 V and $V_{BUS}$ is directly applied to the $V_{BUS}$ pin, precautions must be taken to reduce the voltage to below 3.6 V.

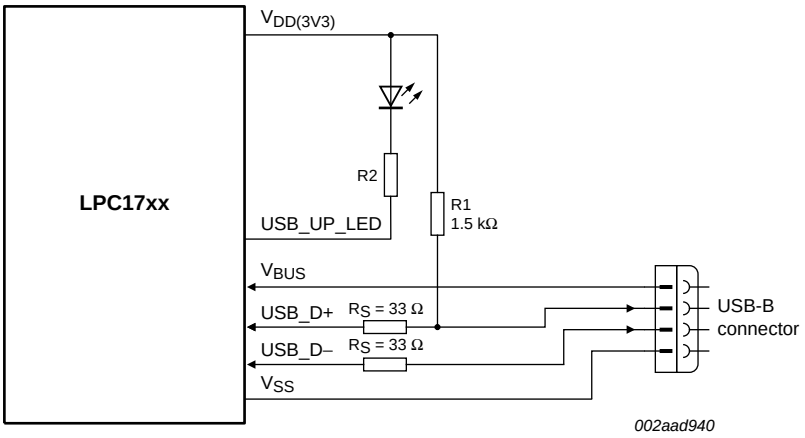



**Fig 30. USB interface on a bus-powered device**

The maximum allowable voltage on the $V_{BUS}$ pin is 3.6 V. One method is to use a voltage divider to connect the $V_{BUS}$ pin to the $V_{BUS}$ on the USB connector.

The voltage divider ratio should be such that the $V_{BUS}$ pin will be greater than $0.7V_{DD}$ to indicate a logic HIGH while below the 3.6 V allowable maximum voltage.

Use the following operating conditions:

$VBUS_{max}$ = 5.25 V

$V_{DD}$ = 3.6 V

The voltage divider would need to provide a reduction of 3.6 V/5.25 V or ~0.686 V.

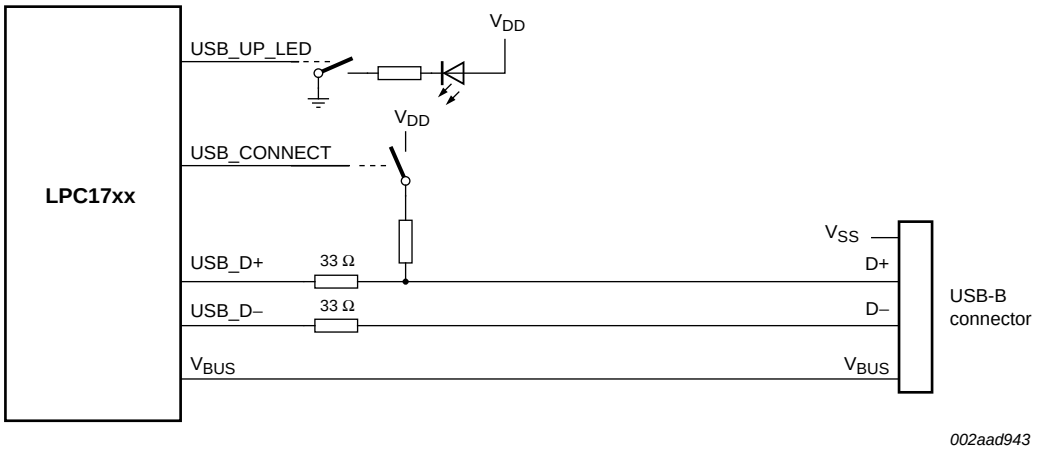



**Fig 35. USB device port configuration**

## 15.2 Crystal oscillator XTAL input and component selection

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with $C_i$ = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground $C_g$ which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV(RMS) is needed.

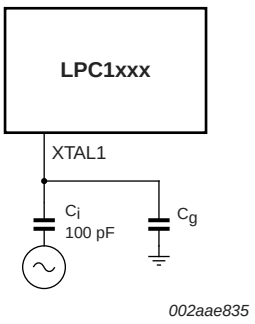
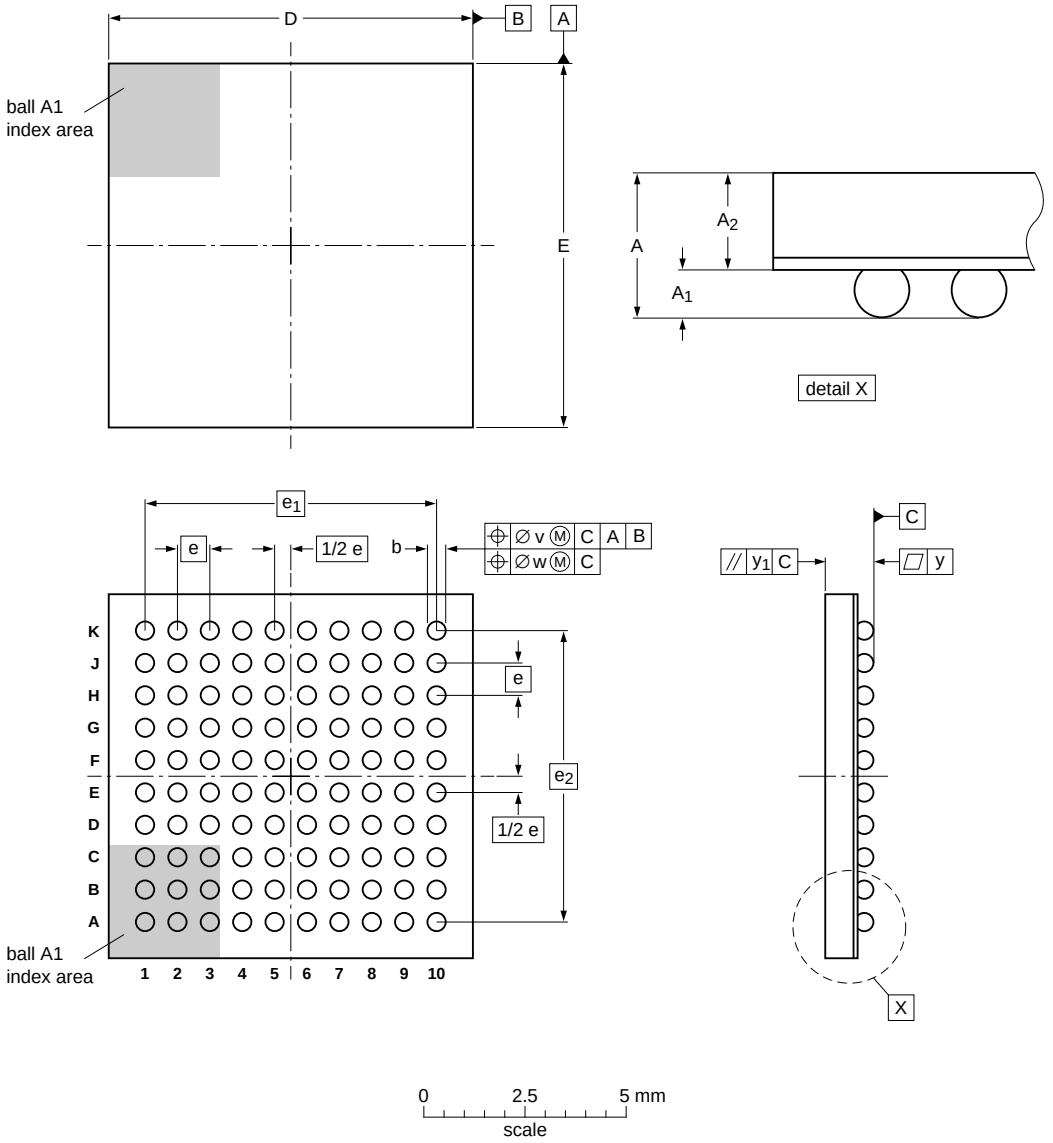



**Fig 36. Slave mode operation of the on-chip oscillator**

In slave mode the input clock signal should be coupled by means of a capacitor of 100 pF (Figure 36), with an amplitude between 200 mV(RMS) and 1000 mV(RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTALOUT pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in Figure 37 and in Table 23 and Table 24. Since the feedback resistance is integrated on chip, only a crystal and the capacitances $C_{X1}$ and $C_{X2}$ need to be connected externally in case of fundamental mode oscillation (the fundamental frequency is represented by L, $C_L$ and $R_S$). Capacitance $C_P$ in Figure 37 represents the parallel package capacitance and should not be larger than 7 pF. Parameters $F_{OSC}$, $C_L$, $R_S$ and $C_P$ are supplied by the crystal manufacturer.

**TFBGA100: plastic thin fine-pitch ball grid array package; 100 balls; body 9 x 9 x 0.7 mm** **SOT926-1**

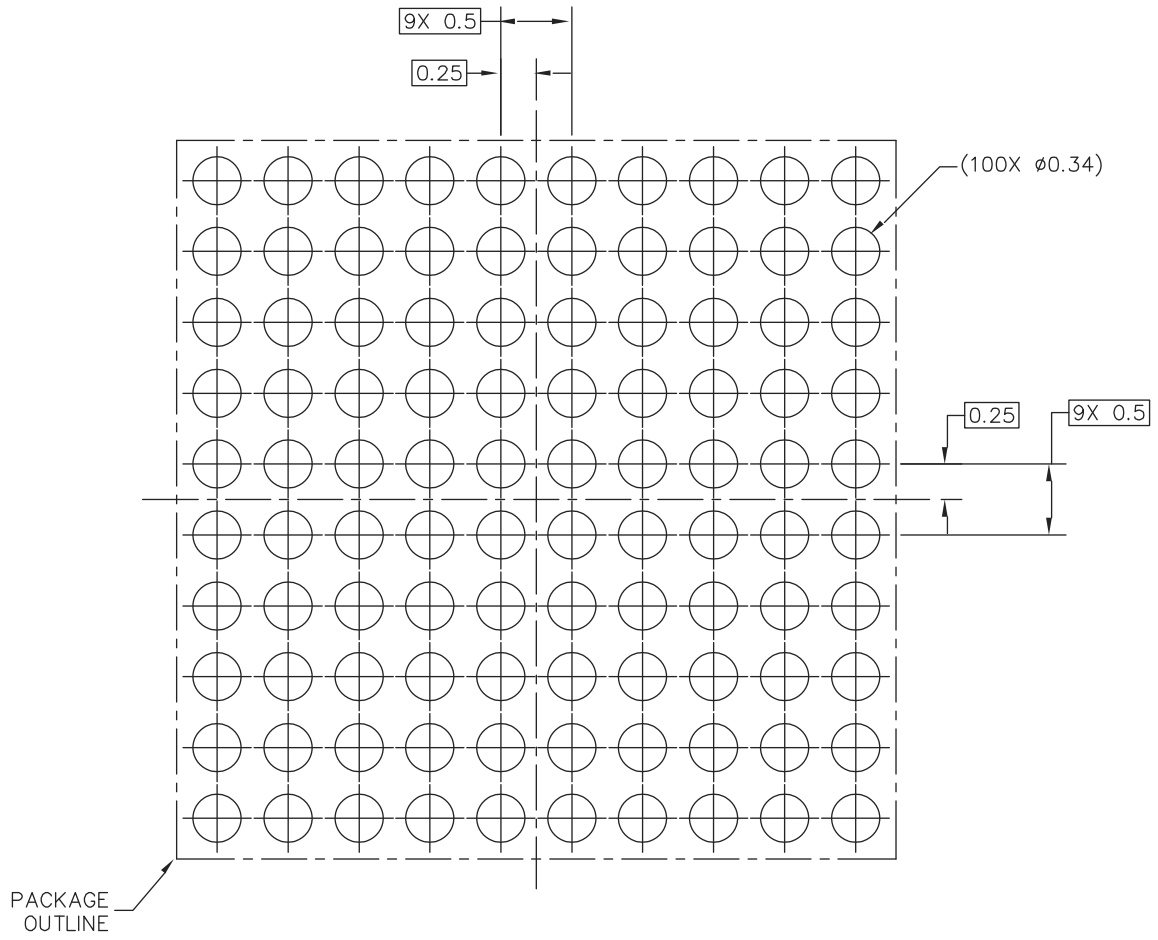



**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max | $A_1$ | $A_2$ | b | D | E | e | $e_1$ | $e_2$ | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.2 | 0.4<br>0.3 | 0.8<br>0.65 | 0.5<br>0.4 | 9.1<br>8.9 | 9.1<br>8.9 | 0.8 | 7.2 | 7.2 | 0.15 | 0.05 | 0.08 | 0.1 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT926-1 | - - - | - - - | - - - | | | ~~05-12-09~~<br>05-12-22 |

**Fig 41. Package outline SOT926-1 (TFBGA100)**




RECOMMENDED STENCIL THICKNESS 0.125

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

 DATE: 06 MAR 2018

| MECHANICAL OUTLINE<br>PRINT VERSION NOT TO SCALE | STANDARD:<br>NON JEDEC | DRAWING NUMBER:<br>SOT1450–2 | REVISION:<br>0 | |
|---|---|---|---|---|

**Fig 47. Reflow soldering of the WLCSP100 package (part 3)**

# 20. Revision history

**Table 27. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| LPC1769_68_67_66_65_64_63 v.9.8 | 20180504 | Product data sheet | - | LPC1769_68_67_66_65_64 v.9.7 |
| Modifications: | • Added Figure 45 “Reflow soldering of the WLCSP100 package (part 1)”, Figure 46 “Reflow soldering of the WLCSP100 package (part 2)”, and Figure 47 “Reflow soldering of the WLCSP100 package (part 3)”. | | | |
| LPC1769_68_67_66_65_64_63 v.9.7 | 20170501 | Product data sheet | - | LPC1769_68_67_66_65_64 v.9.6 |
| Modifications: | • Updated Table 2 “Ordering options”: WLCSP100 with body size 100 balls, 5.07 x 5.07 x 0.53mm; was 5.074 x 5.074 x 0.6mm.<br>• Updated Figure 42 “Package outline SOT1450-2 LPC1768UK (WLCSP100)”. | | | |
| LPC1769_68_67_66_65_64_63 v.9.6 | 20150818 | Product data sheet | - | LPC1769_68_67_66_65_64 v.9.5 |
| Modifications: | • Changed max value of $t_{v(Q)}$ (data output valid time) in SPI mode to $3*T_{cy(PCLK)}$ + 2.5 ns. See Table 16 “Dynamic characteristics: SSP pins in SPI mode”.<br>• Updated Section 2 “Features and benefits”: Added Boundary scan Description Language (BSDL) is not available for this device.<br>• Updated Figure 5 “LPC17xx memory map”: APB0 slot 7 (0x4001C000) was "reserved" and changed it to I2C0.<br>• Changed pins for $V_{DD(REG)(3V3)}$ from F4 and F0 to F4 and F10. See Table 5 “Pin description”.<br>• Removed footnote 1: “5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis. This pin is pulled up to a voltage level of 2.3 V to 2.6 V” from TDO/SWO, TCK/SWDCLK, and RTCK, pins. See Table 5 “Pin description”.<br>• Added a column for GPIO pins and device order part number to the ordering options table. See Table 2 “Ordering options”. | | | |
| LPC1769_68_67_66_65_64_63 v.9.5 | <tbd> | Product data sheet | - | LPC1769_68_67_66_65_64 v.9.4 |
| Modifications: | • SSP timing diagram updated. SSP timing parameters $t_{v(Q)}$, $t_{h(Q)}$, $t_{DS}$, and $t_{DH}$ added. See Section 12.7 “SSP interface”.<br>• Parameter $T_{j(max)}$ added in Table 6 “Limiting values”.<br>• SSP maximum bit rate in master mode corrected to 33 Mbit/s. | | | |
| LPC1769_68_67_66_65_64_63 v.9.4 | 20140404 | Product data sheet | - | LPC1769_68_67_66_65_64 v.9.3 |
| Modifications: | • Added LPC1768UK.<br>• Table 5 “Pin description”: Changed RX_MCLK and TX_MCLK type from INPUT to OUTPUT. | | | |
| LPC1769_68_67_66_65_64_63 v.9.3 | 20140108 | Product data sheet | - | LPC1769_68_67_66_65_64 v.9.2 |
| Modifications: | • Table 7 “Thermal resistance (±15 %)”:<br>– Added TFBGA100.<br>– Added ±15 % to table title. | | | |

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

**Date of release: 4 May 2018**
**Document identifier: LPC1769_68_67_66_65_64_63**