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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, Ethernet, I²C, IrDA, Microwire, SPI, SSI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT
Number of I/O	70
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1769fbd100-551

- ◆ Quadrature encoder interface that can monitor one external quadrature encoder.
- ◆ One standard PWM/timer block with external count input.
- ◆ RTC with a separate power domain and dedicated RTC oscillator. The RTC block includes 20 bytes of battery-powered backup registers.
- ◆ WatchDog Timer (WDT). The WDT can be clocked from the internal RC oscillator, the RTC oscillator, or the APB clock.
- ◆ Arm Cortex-M3 system tick timer, including an external clock input option.
- ◆ Repetitive interrupt timer provides programmable and repeating timed interrupts.
- ◆ Each peripheral has its own clock divider for further power savings.

- Standard JTAG debug interface for compatibility with existing tools. Serial Wire Debug and Serial Wire Trace Port options. Boundary Scan Description Language (BSDL) is not available for this device.
- Emulation trace module enables non-intrusive, high-speed real-time tracing of instruction execution.
- Integrated PMU (Power Management Unit) automatically adjusts internal regulators to minimize power consumption during Sleep, Deep sleep, Power-down, and Deep power-down modes.
- Four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.
- Single 3.3 V power supply (2.4 V to 3.6 V).
- Four external interrupt inputs configurable as edge/level sensitive. All pins on Port 0 and Port 2 can be used as edge sensitive interrupt sources.
- Non-maskable Interrupt (NMI) input.
- Clock output function that can reflect the main oscillator clock, IRC clock, RTC clock, CPU clock, and the USB clock.
- The Wake-up Interrupt Controller (WIC) allows the CPU to automatically wake up from any priority interrupt that can occur while the clocks are stopped in deep sleep, Power-down, and Deep power-down modes.
- Processor wake-up from Power-down mode via any interrupt able to operate during Power-down mode (includes external interrupts, RTC interrupt, USB activity, Ethernet wake-up interrupt, CAN bus activity, Port 0/2 pin interrupt, and NMI).
- Brownout detect with separate threshold for interrupt and forced reset.
- Power-On Reset (POR).
- Crystal oscillator with an operating range of 1 MHz to 25 MHz.
- 4 MHz internal RC oscillator trimmed to 1 % accuracy that can optionally be used as a system clock.
- PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the main oscillator, the internal RC oscillator, or the RTC oscillator.
- USB PLL for added flexibility.
- Code Read Protection (CRP) with different security levels.
- Unique device serial number for identification purposes.
- Available as LQFP100 (14 mm × 14 mm × 1.4 mm), TFBGA100[1] (9 mm × 9 mm × 0.7 mm), and WLCSP100 (5.07 × 5.07 × 0.53 mm) package.

1. LPC1768/65 only.

5. Marking

The LPC176x devices typically have the following top-side marking:

LPC176xxxx

xxxxxxx

xxYYWWR[x]

The last/second to last letter in the third line (field ‘R’) will identify the device revision. This data sheet covers the following revisions of the LPC176x:

Table 3. Device revision table

Revision identifier (R)	Revision description
‘-’	Initial device revision
‘A’	Second device revision
‘B’	Third device revision

Field ‘YY’ states the year the device was manufactured. Field ‘WW’ states the week the device was manufactured during that year.

Table 4. Pin allocation table TFBGA100 *…continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
9	P2[7]/RD2/RTS1	10	P2[8]/TD2/TXD2	11	-	12	-
Row F							
1	VREFN	2	RTCX1	3	$\overline{\text{RESET}}$	4	P1[31]/SCK1/AD0[5]
5	P1[21]/$\overline{\text{MCABORT}}$/PWM1[3]/SSEL0	6	P0[18]/DCD1/MOSI0/MOSI	7	P2[9]/USB_CONNECT/RXD2	8	P0[16]/RXD1/SSEL0/SSEL
9	P0[17]/CTS1/MISO0/MISO	10	P0[15]/TXD1/SCK0/SCK	11	-	12	-
Row G							
1	RTCX2	2	VBAT	3	XTAL2	4	P0[30]/USB_D−
5	P1[25]/MCOA1/MAT1[1]	6	P1[29]/MCOB2/PCAP1[1]/MAT0[1]	7	V_{SS}	8	P0[21]/RI1/RD1
9	P0[20]/DTR1/SCL1	10	P0[19]/DSR1/SDA1	11	-	12	-
Row H							
1	P1[30]/V_{BUS}/AD0[4]	2	XTAL1	3	P3[25]/MAT0[0]/PWM1[2]	4	P1[18]/USB_UP_LED/PWM1[1]/CAP1[0]
5	P1[24]/MCI2/PWM1[5]/MOSI0	6	$V_{DD(REG)(3V3)}$	7	P0[10]/TXD2/SDA2/MAT3[0]	8	P2[11]/$\overline{\text{EINT1}}$/I2STX_CLK
9	$V_{DD(3V3)}$	10	P0[22]/RTS1/TD1	11	-	12	-

Table 5. Pin description *…continued*

Symbol	Pin/ball LQFP100	Pin/ball TFBGA100	Pin/ball WLCSP100		Type	Description
P2[11]/EINT1/ I2STX_CLK	52	H8	J8	[6]	I/O	**P2[11] —** General purpose digital input/output pin.
					I	**EINT1 —** External interrupt 1 input.
					I/O	**I2STX_CLK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I²S-bus specification*. (LPC1769/68/67/66/65/63 only).
P2[12]/EINT2/ I2STX_WS	51	K10	K10	[6]	I/O	**P2[12] —** General purpose digital input/output pin.
					I	**EINT2 —** External interrupt 2 input.
					I/O	**I2STX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*. (LPC1769/68/67/66/65/63 only).
P2[13]/EINT3/ I2STX_SDA	50	J9	J9	[6]	I/O	**P2[13] —** General purpose digital input/output pin.
					I	**EINT3 —** External interrupt 3 input.
					I/O	**I2STX_SDA —** Transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*. (LPC1769/68/67/66/65/63 only).
P3[0] to P3[31]					I/O	**Port 3:** Port 3 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 3 pins depends upon the pin function selected via the pin connect block. Pins 0 through 24, and 27 through 31 of this port are not available.
P3[25]/MAT0[0]/ PWM1[2]	27	H3	D8	[1]	I/O	**P3[25] —** General purpose digital input/output pin.
					O	**MAT0[0] —** Match output for Timer 0, channel 0.
					O	**PWM1[2] —** Pulse Width Modulator 1, output 2.
P3[26]/STCLK/ MAT0[1]/PWM1[3]	26	K1	A10	[1]	I/O	**P3[26] —** General purpose digital input/output pin.
					I	**STCLK —** System tick timer clock input. The maximum STCLK frequency is 1/4 of the Arm processor clock frequency CCLK.
					O	**MAT0[1] —** Match output for Timer 0, channel 1.
					O	**PWM1[3] —** Pulse Width Modulator 1, output 3.
P4[0] to P4[31]					I/O	**Port 4:** Port 4 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 4 pins depends upon the pin function selected via the pin connect block. Pins 0 through 27, 30, and 31 of this port are not available.
P4[28]/RX_MCLK/ MAT2[0]/TXD3	82	C7	G1	[1]	I/O	**P4[28] —** General purpose digital input/output pin.
					O	**RX_MCLK —** I²S receive master clock. (LPC1769/68/67/66/65 only).
					O	**MAT2[0] —** Match output for Timer 2, channel 0.
					O	**TXD3 —** Transmitter output for UART3.
P4[29]/TX_MCLK/ MAT2[1]/RXD3	85	E6	F1	[1]	I/O	**P4[29] —** General purpose digital input/output pin.
					O	**TX_MCLK —** I²S transmit master clock. (LPC1769/68/67/66/65 only).
					O	**MAT2[1] —** Match output for Timer 2, channel 1.
					I	**RXD3 —** Receiver input for UART3.

Table 5. Pin description *…continued*

Symbol	Pin/ball				Type	Description
	LQFP100	**TFBGA100**	**WLCSP100**			
TDO/SWO	1	A1	A1	[7]	O	**TDO —** Test Data out for JTAG interface.
					O	**SWO —** Serial wire trace output.
TDI	2	C3	C4	[1][8]	I	**TDI —** Test Data in for JTAG interface.
TMS/SWDIO	3	B1	B3	[1][8]	I	**TMS —** Test Mode Select for JTAG interface.
					I/O	**SWDIO —** Serial wire debug data input/output.
$\overline{\text{TRST}}$	4	C2	A2	[1][8]	I	**$\overline{\text{TRST}}$ —** Test Reset for JTAG interface.
TCK/SWDCLK	5	C1	D4	[7]	I	**TCK —** Test Clock for JTAG interface.
					I	**SWDCLK —** Serial wire clock.
RTCK	100	B2	B2	[7]	O	**RTCK —** JTAG interface control signal.
$\overline{\text{RSTOUT}}$	14	-	-	-	O	**$\overline{\text{RSTOUT}}$ —** This is a 3.3 V pin. LOW on this pin indicates the microcontroller being in Reset state.
$\overline{\text{RESET}}$	17	F3	C6	[9]	I	**External reset input:** A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. TTL with hysteresis, 5 V tolerant.
XTAL1	22	H2	D7	[10][11]	I	Input to the oscillator circuit and internal clock generator circuits.
XTAL2	23	G3	A9	[10][11]	O	Output from the oscillator amplifier.
RTCX1	16	F2	A7	[10][11]	I	Input to the RTC oscillator circuit.
RTCX2	18	G1	B7	[10]	O	Output from the RTC oscillator circuit.
V_{SS}	31, 41, 55, 72, 83, 97	B3, B7, C9, G7, J6, K3	E5, F5, F6, G5, G6, G7	[10]	I	**ground:** 0 V reference.
V_{SSA}	11	E1	B5	[10]	I	**analog ground:** 0 V reference. This should nominally be the same voltage as V_{SS}, but should be isolated to minimize noise and error.
$V_{DD(3V3)}$	28, 54, 71, 96	K2, H9, C10, A3	E4, E6, F7, G4	[10]	I	**3.3 V supply voltage:** This is the power supply voltage for the I/O ports.
$V_{DD(REG)(3V3)}$	42, 84	H6, A7	F4, F10	[10]	I	**3.3 V voltage regulator supply voltage:** This is the supply voltage for the on-chip voltage regulator only.
V_{DDA}	10	E2	A4	[10]	I	**analog 3.3 V pad supply voltage:** This should be nominally the same voltage as $V_{DD(3V3)}$ but should be isolated to minimize noise and error. This voltage is used to power the ADC and DAC. This pin should be tied to 3.3 V if the ADC and DAC are not used.
VREFP	12	E3	A5	[10]	I	**ADC positive reference voltage:** This should be nominally the same voltage as V_{DDA} but should be isolated to minimize noise and error. Level on this pin is used as a reference for ADC and DAC. This pin should be tied to 3.3 V if the ADC and DAC are not used.

8.7 Nested Vectored Interrupt Controller (NVIC)

The NVIC is an integral part of the Cortex-M3. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

8.7.1 Features

- Controls system exceptions and peripheral interrupts
- In the LPC17xx, the NVIC supports 33 vectored interrupts
- 32 programmable interrupt priority levels, with hardware priority level masking
- Relocatable vector table
- Non-Maskable Interrupt (NMI)
- Software interrupt generation

8.7.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Any pin on Port 0 and Port 2 (total of 42 pins) regardless of the selected function, can be programmed to generate an interrupt on a rising edge, a falling edge, or both.

8.8 Pin connect block

The pin connect block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Peripherals should be connected to the appropriate pins prior to being activated and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

Most pins can also be configured as open-drain outputs or to have a pull-up, pull-down, or no resistor enabled.

8.9 General purpose DMA controller

The GPDMA is an AMBA AHB compliant peripheral allowing selected peripherals to have DMA support.

The GPDMA enables peripheral-to-memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions. The source and destination areas can each be either a memory region or a peripheral, and can be accessed through the AHB master. The GPDMA controller allows data transfers between the USB and Ethernet controllers and the various on-chip SRAM areas. The supported APB peripherals are SSP0/1, all UARTs, the I^{2}S-bus interface, the ADC, and the DAC. Two match signals for each timer can be used to trigger DMA transfers.

Remark: The Ethernet controller is available on parts LPC1769/68/67/66/64. The USB controller is available on parts LPC1769/68/66/65/64. The I^{2}S-bus interface is available on parts LPC1769/68/67/66/65. The DAC is available on parts LPC1769/68/67/66/65/63.

data transfer. The SSP supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

8.18.1 Features

- Maximum SSP speed of 33 Mbit/s (master) or 8 Mbit/s (slave)
- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame
- DMA transfers supported by GPDMA

8.19 I²C-bus serial I/O controllers

The LPC17xx each contain three I²C-bus controllers.

The I²C-bus is bidirectional for inter-IC control using only two wires: a Serial Clock line (SCL) and a Serial DAta line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I²C is a multi-master bus and can be controlled by more than one bus master connected to it.

8.19.1 Features

- I²C0 is a standard I²C compliant bus interface with open-drain pins. I²C0 also supports Fast mode plus with bit rates up to 1 Mbit/s.
- I²C1 and I²C2 use standard I/O pins with bit rates of up to 400 kbit/s (Fast I²C-bus).
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I²C-bus can be used for test and diagnostic purposes.
- All I²C-bus controllers support multiple address recognition and a bus monitor mode.

8.20 I²S-bus serial I/O controllers

Remark: The I²S-bus interface is available on parts LPC1769/68/67/66/65/63. See Table 2.

The I²S-bus provides a standard communication interface for digital audio applications.

The *I²S-bus specification* defines a 3-wire serial bus using one data line, one clock line, and one word select signal. The basic I²S-bus connection has one master, which is always the master, and one slave. The I²S-bus interface provides a separate transmit and receive channel, each of which can operate as either a master or a slave.

8.20.1 Features

- The interface has separate input/output channels each of which can operate in master or slave mode.
- Capable of handling 8-bit, 16-bit, and 32-bit word sizes.
- Mono and stereo audio data supported.
- The sampling frequency can range from 16 kHz to 96 kHz (16, 22.05, 32, 44.1, 48, 96) kHz.
- Support for an audio master clock.
- Configurable word select period in master mode (separately for I²S-bus input and output).
- Two 8-word FIFO data buffers are provided, one for transmit and one for receive.
- Generates interrupt requests when buffer levels cross a programmable boundary.
- Two DMA requests, controlled by programmable buffer levels. These are connected to the GPDMA block.
- Controls include reset, stop and mute options separately for I²S-bus input and I²S-bus output.

8.21 General purpose 32-bit timers/external event counters

The LPC17xx include four 32-bit timer/counters. The timer/counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts, generate timed DMA requests, or perform other actions at specified timer values, based on four match registers. Each timer/counter also includes two capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

8.21.1 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler.
- Counter or timer operation.
- Two 32-bit capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.

- Supports single edge controlled and/or double edge controlled PWM outputs. Single edge controlled PWM outputs all go high at the beginning of each cycle unless the output is a constant low. Double edge controlled PWM outputs can have either edge occur at any position within a cycle. This allows for both positive going and negative going pulses.
- Pulse period and width can be any number of timer counts. This allows complete flexibility in the trade-off between resolution and repetition rate. All PWM outputs will occur at the same repetition rate.
- Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses.
- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must ‘release’ new match values before they can become effective.
- May be used as a standard 32-bit timer/counter with a programmable 32-bit prescaler if the PWM mode is not enabled.

8.23 Motor control PWM

The motor control PWM is a specialized PWM supporting 3-phase motors and other combinations. Feedback inputs are provided to automatically sense rotor position and use that information to ramp speed up or down. An abort input is also provided that causes the PWM to immediately release all motor drive outputs. At the same time, the motor control PWM is highly configurable for other generalized timing, counting, capture, and compare applications.

8.24 Quadrature Encoder Interface (QEI)

A quadrature encoder, also known as a 2-channel incremental encoder, converts angular displacement into two pulse signals. By monitoring both the number of pulses and the relative phase of the two signals, the user can track the position, direction of rotation, and velocity. In addition, a third channel, or index signal, can be used to reset the position counter. The quadrature encoder interface decodes the digital pulses from a quadrature encoder wheel to integrate position over time and determine direction of rotation. In addition, the QEI can capture the velocity of the encoder wheel.

8.24.1 Features

- Tracks encoder position.
- Increments/decrements depending on direction.
- Programmable for 2× or 4× position counting.
- Velocity capture using built-in timer.
- Velocity compare function with “less than” interrupt.
- Uses 32-bit registers for position and velocity.
- Three position compare registers with interrupts.
- Index counter for revolution counting.
- Index compare register with interrupts.
- Can combine index and position interrupts to produce an interrupt for whole and partial revolution displacement.

See Figure 6 for an overview of the LPC17xx clock generation.

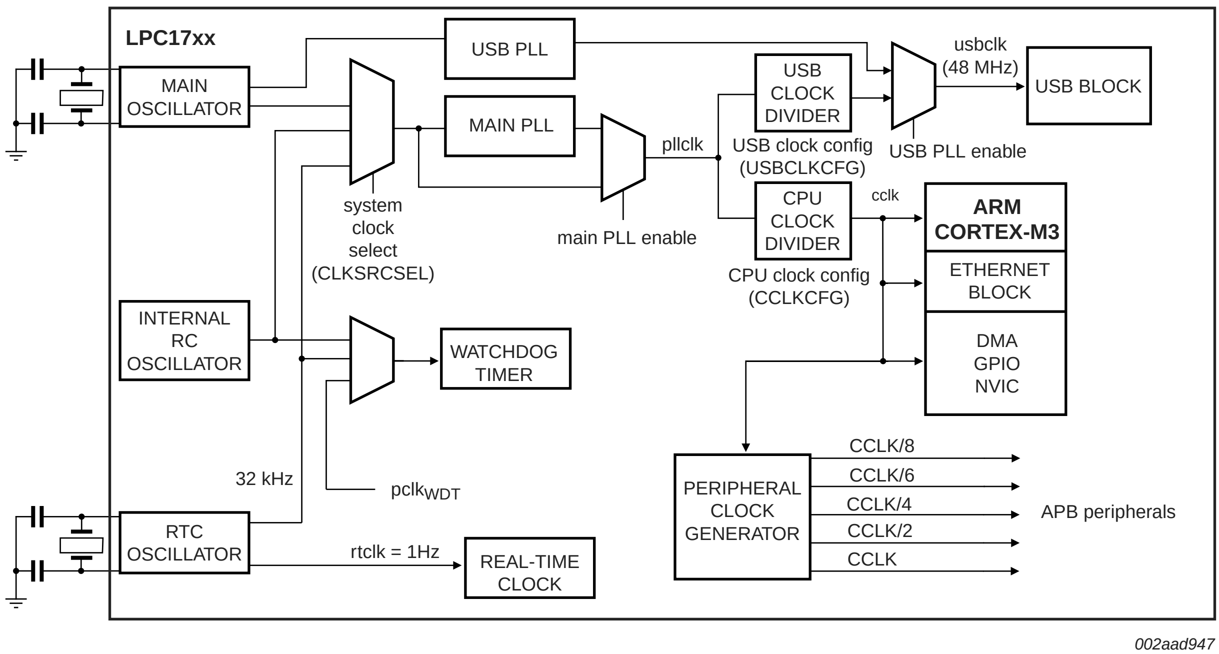


Fig 6. LPC17xx clocking generation block diagram

8.29.1.1 Internal RC oscillator

The IRC may be used as the clock source for the WDT, and/or as the clock that drives the PLL and subsequently the CPU. The nominal IRC frequency is 4 MHz. The IRC is trimmed to 1 % accuracy over the entire voltage and temperature range.

Upon power-up or any chip reset, the LPC17xx use the IRC as the clock source. Software may later switch to one of the other available clock sources.

8.29.1.2 Main oscillator

The main oscillator can be used as the clock source for the CPU, with or without using the PLL. The main oscillator also provides the clock source for the dedicated USB PLL.

The main oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the main PLL. The clock selected as the PLL input is PLLCLKIN. The Arm processor clock frequency is referred to as CCLK elsewhere in this document. The frequencies of PLLCLKIN and CCLK are the same value unless the PLL is active and connected. The clock frequency for each peripheral can be selected individually and is referred to as PCLK. Refer to Section 8.29.2 for additional information.

8.29.1.3 RTC oscillator

The RTC oscillator can be used as the clock source for the RTC block, the main PLL, and/or the CPU.

whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the wake-up timer.

The Wake-up Timer monitors the crystal oscillator to check whether it is safe to begin code execution. When power is applied to the chip, or when some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient amplitude to drive the clock logic. The amount of time depends on many factors, including the rate of $V_{DD(3V3)}$ ramp (in the case of power on), the type of crystal and its electrical characteristics (if a quartz crystal is used), as well as any other external circuitry (e.g., capacitors), and the characteristics of the oscillator itself under the existing ambient conditions.

8.29.6 Power control

The LPC17xx support a variety of power control features. There are four special modes of processor power reduction: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, Peripheral Power Control allows shutting down the clocks to individual on-chip peripherals, allowing fine tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Each of the peripherals has its own clock divider which provides even better power control.

Integrated PMU (Power Management Unit) automatically adjust internal regulators to minimize power consumption during Sleep, Deep sleep, Power-down, and Deep power-down modes.

The LPC17xx also implement a separate power domain to allow turning off power to the bulk of the device while maintaining operation of the RTC and a small set of registers for storing data during any of the power-down modes.

8.29.6.1 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the Arm core.

In Sleep mode, execution of instructions is suspended until either a Reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

8.29.6.2 Deep-sleep mode

In Deep-sleep mode, the oscillator is shut down and the chip receives no internal clocks. The processor state and registers, peripheral registers, and internal SRAM values are preserved throughout Deep-sleep mode and the logic levels of chip pins remain static. The output of the IRC is disabled but the IRC is not powered down for a fast wake-up later. The RTC oscillator is not stopped because the RTC interrupts may be used as the wake-up source. The PLL is automatically turned off and disconnected. The CCLK and USB clock dividers automatically get reset to zero.

8.29.8 Power domains

The LPC17xx provide two independent power domains that allow the bulk of the device to have power removed while maintaining operation of the RTC and the backup Registers.

On the LPC17xx, I/O pads are powered by the 3.3 V ($V_{DD(3V3)}$) pins, while the $V_{DD(REG)(3V3)}$ pin powers the on-chip voltage regulator which in turn provides power to the CPU and most of the peripherals.

Depending on the LPC17xx application, a design can use two power options to manage power consumption.

The first option assumes that power consumption is not a concern and the design ties the $V_{DD(3V3)}$ and $V_{DD(REG)(3V3)}$ pins together. This approach requires only one 3.3 V power supply for both pads, the CPU, and peripherals. While this solution is simple, it does not support powering down the I/O pad ring “on the fly” while keeping the CPU and peripherals alive.

The second option uses two power supplies; a 3.3 V supply for the I/O pads ($V_{DD(3V3)}$) and a dedicated 3.3 V supply for the CPU ($V_{DD(REG)(3V3)}$). Having the on-chip voltage regulator powered independently from the I/O pad ring enables shutting down of the I/O pad power supply “on the fly”, while the CPU and peripherals stay active.

The VBAT pin supplies power only to the RTC domain. The RTC requires a minimum of power to operate, which can be supplied by an external battery. The device core power ($V_{DD(REG)(3V3)}$) is used to operate the RTC whenever $V_{DD(REG)(3V3)}$ is present. Therefore, there is no power drain from the RTC battery when $V_{DD(REG)(3V3)}$ is available.

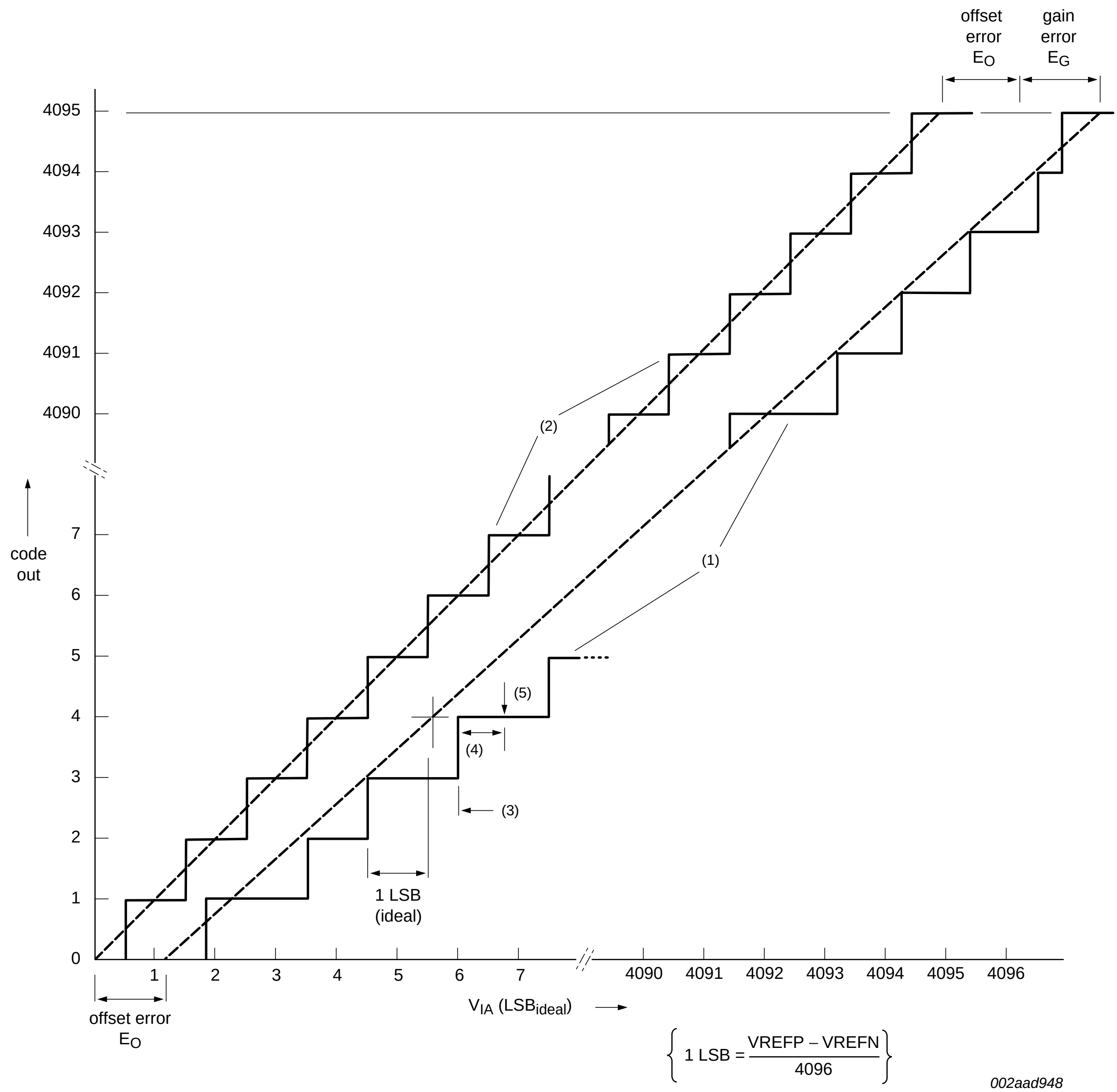
11.2 Peripheral power consumption

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the PCONP register. All other blocks are disabled and no code is executed. Measured on a typical sample at T_{amb} = 25 °C. The peripheral clock PCLK = CCLK/4.

Table 9. Power consumption for individual analog and digital blocks

Peripheral	Conditions	Typical supply current in mA; CCLK =			Notes
		12 MHz	48 MHz	100 MHz	
Timer		0.03	0.11	0.23	Average current per timer
UART		0.07	0.26	0.53	Average current per UART
PWM		0.05	0.20	0.41	
Motor control PWM		0.05	0.21	0.42	
I2C		0.02	0.08	0.16	Average current per I2C
SPI		0.02	0.06	0.13	
SSP1		0.04	0.16	0.32	
ADC	PCLK = 12 MHz for CCLK = 12 MHz and 48 MHz; PCLK = 12.5 MHz for CCLK = 100 MHz	2.12	2.09	2.07	
CAN	PCLK = CCLK/6	0.13	0.49	1.00	Average current per CAN
CAN0, CAN1, acceptance filter	PCLK = CCLK/6	0.22	0.85	1.73	Both CAN blocks and acceptance filter[1]
DMA	PCLK = CCLK	1.33	5.10	10.36	
QEI		0.05	0.20	0.41	
GPIO		0.33	1.27	2.58	
I2S		0.09	0.34	0.70	
USB and PLL1		0.94	1.32	1.94	
Ethernet	Ethernet block enabled in the PCONP register; Ethernet not connected.	0.49	1.87	3.79	
Ethernet connected	Ethernet initialized, connected to network, and running web server example.	-	-	5.19	

[1] The combined current of several peripherals running at the same time can be less than the sum of each individual peripheral current measured separately.



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 28. 12-bit ADC characteristics

order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Values of C_{x1} and C_{x2} should be chosen smaller accordingly to the increase in parasitics of the PCB layout.

15.4 Standard I/O pin configuration

Figure 38 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver: Open-drain mode enabled/disabled
- Digital input: Pull-up enabled/disabled
- Digital input: Pull-down enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Analog input

The default configuration for standard I/O pins is input with pull-up enabled. The weak MOS devices provide a drive capability equivalent to pull-up and pull-down resistors.

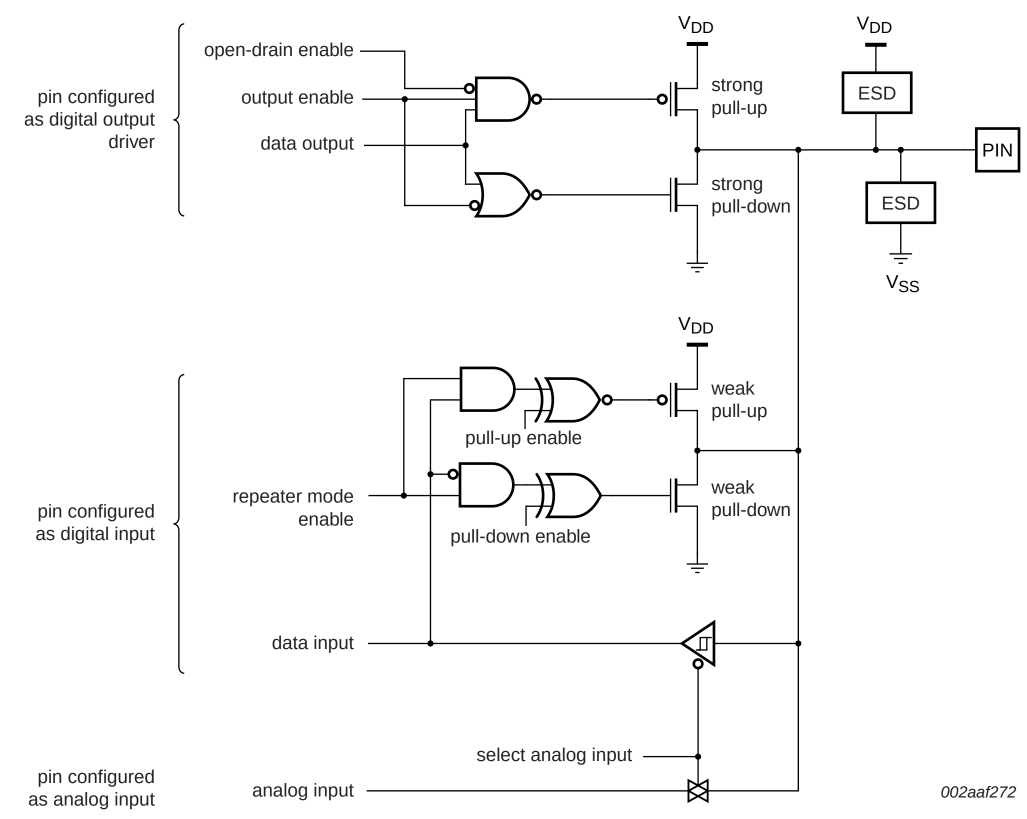


Fig 38. Standard I/O pin configuration with analog input

15.5 Reset pin configuration

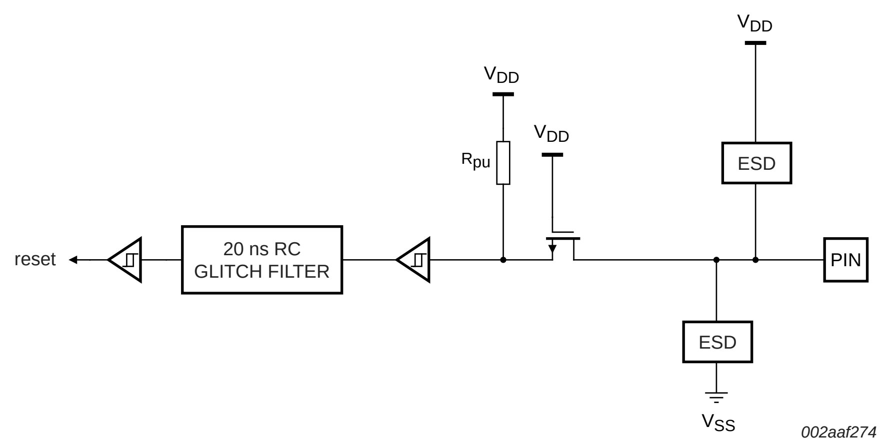
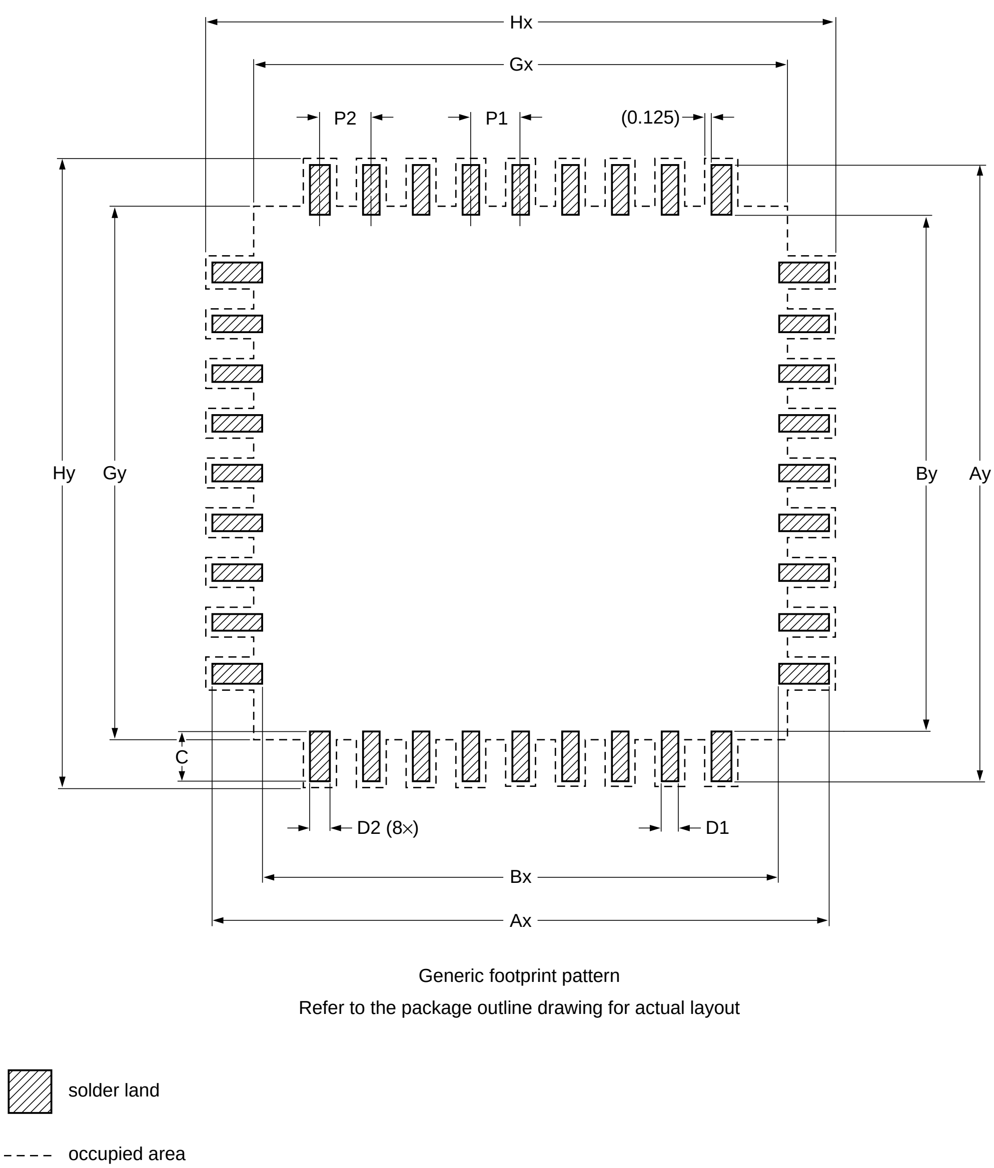


Fig 39. Reset pin configuration

17. Soldering

Footprint information for reflow soldering of LQFP100 package **SOT407-1**



DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	17.300	17.300	14.300	14.300	1.500	0.280	0.400	14.500	14.500	17.550	17.550

sot407-1

Fig 43. Reflow soldering for the LQFP100 package

20. Revision history

Table 27. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC1769_68_67_66_65_64_63 v.9.8	20180504	Product data sheet	-	LPC1769_68_67_66_65_64 v.9.7
Modifications:	• Added Figure 45 “Reflow soldering of the WLCSP100 package (part 1)”, Figure 46 “Reflow soldering of the WLCSP100 package (part 2)”, and Figure 47 “Reflow soldering of the WLCSP100 package (part 3)”.			
LPC1769_68_67_66_65_64_63 v.9.7	20170501	Product data sheet	-	LPC1769_68_67_66_65_64 v.9.6
Modifications:	• Updated Table 2 “Ordering options”: WLCSP100 with body size 100 balls, 5.07 x 5.07 x 0.53mm; was 5.074 x 5.074 x 0.6mm. • Updated Figure 42 “Package outline SOT1450-2 LPC1768UK (WLCSP100)”.			
LPC1769_68_67_66_65_64_63 v.9.6	20150818	Product data sheet	-	LPC1769_68_67_66_65_64 v.9.5
Modifications:	• Changed max value of $t_{v(Q)}$ (data output valid time) in SPI mode to 3*$T_{cy(PCLK)}$ + 2.5 ns. See Table 16 “Dynamic characteristics: SSP pins in SPI mode”. • Updated Section 2 “Features and benefits”: Added Boundary scan Description Language (BSDL) is not available for this device. • Updated Figure 5 “LPC17xx memory map”: APB0 slot 7 (0x4001C000) was "reserved" and changed it to I2C0. • Changed pins for $V_{DD(REG)(3V3)}$ from F4 and F0 to F4 and F10. See Table 5 “Pin description”. • Removed footnote 1: “5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis. This pin is pulled up to a voltage level of 2.3 V to 2.6 V” from TDO/SWO, TCK/SWDCLK, and RTCK, pins. See Table 5 “Pin description”. • Added a column for GPIO pins and device order part number to the ordering options table. See Table 2 “Ordering options”.			
LPC1769_68_67_66_65_64_63 v.9.5	<tbd>	Product data sheet	-	LPC1769_68_67_66_65_64 v.9.4
Modifications:	• SSP timing diagram updated. SSP timing parameters $t_{v(Q)}$, $t_{h(Q)}$, t_{DS}, and t_{DH} added. See Section 12.7 “SSP interface”. • Parameter $T_{j(max)}$ added in Table 6 “Limiting values”. • SSP maximum bit rate in master mode corrected to 33 Mbit/s.			
LPC1769_68_67_66_65_64_63 v.9.4	20140404	Product data sheet	-	LPC1769_68_67_66_65_64 v.9.3
Modifications:	• Added LPC1768UK. • Table 5 “Pin description”: Changed RX_MCLK and TX_MCLK type from INPUT to OUTPUT.			
LPC1769_68_67_66_65_64_63 v.9.3	20140108	Product data sheet	-	LPC1769_68_67_66_65_64 v.9.2
Modifications:	• Table 7 “Thermal resistance (±15 %)”: – Added TFBGA100. – Added ±15 % to table title.			

21. Legal information

21.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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