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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	180MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM, SRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps
SATA	-
USB	USB 2.0 (2)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	217-LFBGA
Supplier Device Package	217-LFBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/atmel/at91sam9260b-cu-100

15.5 Watchdog Timer (WDT) User Interface

Table 15-1. Register Mapping

Offset	Register	Name	Access	Reset
0x00	Control Register	WDT_CR	Write-only	–
0x04	Mode Register	WDT_MR	Read/Write Once	0x3FFF_2FFF
0x08	Status Register	WDT_SR	Read-only	0x0000_0000

20. SDRAM Controller (SDRAMC)

20.1 Description

The SDRAM Controller (SDRAMC) extends the memory capabilities of a chip by providing the interface to an external 16-bit or 32-bit SDRAM device. The page size supports ranges from 2048 to 8192 and the number of columns from 256 to 2048. It supports byte (8-bit), half-word (16-bit) and word (32-bit) accesses.

The SDRAM Controller supports a read or write burst length of one location. It keeps track of the active row in each bank, thus maximizing SDRAM performance, e.g., the application may be placed in one bank and data in the other banks. So as to optimize performance, it is advisable to avoid accessing different rows in the same bank.

The SDRAM controller supports a CAS latency of 1, 2 or 3 and optimizes the read access depending on the frequency.

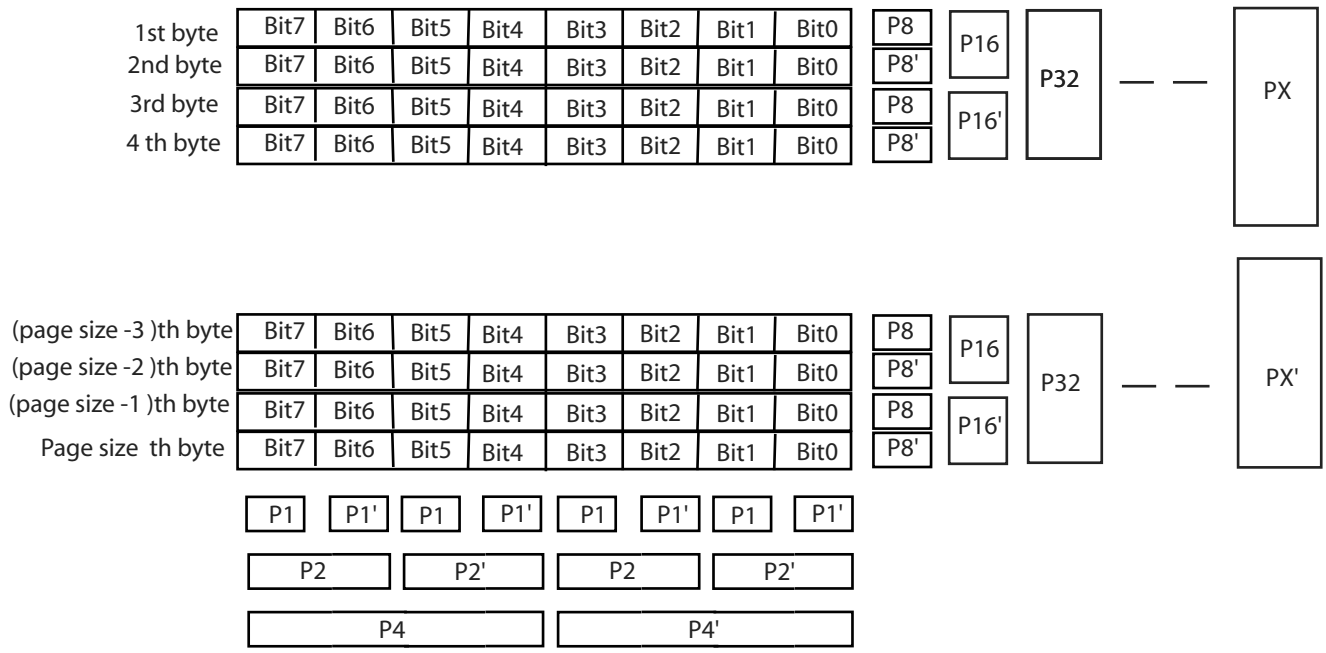
The different modes available - self-refresh, power-down and deep power-down modes - minimize power consumption on the SDRAM device.

20.2 I/O Lines Description

Table 20-1. I/O Line Description

Name	Description	Type	Active Level
SDCK	SDRAM Clock	Output	
SDCKE	SDRAM Clock Enable	Output	High
SDCS	SDRAM Controller Chip Select	Output	Low
BA[1:0]	Bank Select Signals	Output	
RAS	Row Signal	Output	Low
CAS	Column Signal	Output	Low
SDWE	SDRAM Write Enable	Output	Low
NBS[3:0]	Data Mask Enable Signals	Output	Low
SDRAMC_A[12:0]	Address Bus	Output	
D[31:0]	Data Bus	I/O	

Figure 21-2. Parity Generation for 512/1024/2048/4096 8-bit Words1



Page size = 512 Px = 2048
Page size = 1024 Px = 4096
Page size = 2048 Px = 8192
Page size = 4096 Px = 16384

P1=bit7(+)bit5(+)bit3(+)bit1(+)P1
P2=bit7(+)bit6(+)bit3(+)bit2(+)P2
P4=bit7(+)bit6(+)bit5(+)bit4(+)P4
P1'=bit6(+)bit4(+)bit2(+)bit0(+)P1'
P2'=bit5(+)bit4(+)bit1(+)bit0(+)P2'
P4'=bit7(+)bit6(+)bit5(+)bit4(+)P4'

To calculate P8' to PX' and P8 to PX, apply the algorithm that follows.

Page size = 2^n

```
for i =0 to n
begin
 for (j = 0 to page_size_byte)
 begin
  if(j[i] ==1)
   P[2^(i+3)]=bit7(+)bit6(+)bit5(+)bit4(+)bit3(+)
              bit2(+)bit1(+)bit0(+)P[2^(i+3)]
  else
   P[2^(i+3)]'=bit7(+)bit6(+)bit5(+)bit4(+)bit3(+)
               bit2(+)bit1(+)bit0(+)P[2^(i+3)]'
  end
end
```

22.5.2 Receive Counter Register

Name: PERIPH_RCR

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
RXCTR							
7	6	5	4	3	2	1	0
RXCTR							

- **RXCTR: Receive Counter Register**

RXCTR must be set to receive buffer size.

When a half duplex peripheral is connected to the PDC, RXCTR = TXCTR.

0: Stops peripheral data transfer to the receiver

1–65535: Starts peripheral data transfer if corresponding channel is active

24.9.15 PMC Status Register

Name: PMC_SR

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	PCKRDY1	PCKRDY0
7	6	5	4	3	2	1	0
OSC_SEL	–	–	–	MCKRDY	LOCKB	LOCKA	MOSCS

- **MOSCS: MOSCS Flag Status**

0: Main oscillator is not stabilized.

1: Main oscillator is stabilized.

- **LOCKA: PLL A Lock Status**

0: PLL A is not locked

1: PLL A is locked.

- **LOCKB: PLL B Lock Status**

0: PLL B is not locked.

1: PLL B is locked.

- **MCKRDY: Master Clock Status**

0: Master Clock is not ready.

1: Master Clock is ready.

- **OSC_SEL: Slow Clock Oscillator Selection**

0: Internal slow clock RC oscillator.

1: External slow clock 32 kHz oscillator.

- **PCKRDYx: Programmable Clock Ready Status**

0: Programmable Clock x is not ready.

1: Programmable Clock x is ready.

25.9.13 AIC Interrupt Clear Command Register

Name: AIC_ICCR

Access: Write-only

31	30	29	28	27	26	25	24
PID31	PID30	PID29	PID28	PID27	PID26	PID25	PID24
23	22	21	20	19	18	17	16
PID23	PID22	PID21	PID20	PID19	PID18	PID17	PID16
15	14	13	12	11	10	9	8
PID15	PID14	PID13	PID12	PID11	PID10	PID9	PID8
7	6	5	4	3	2	1	0
PID7	PID6	PID5	PID4	PID3	PID2	SYS	FIQ

- **FIQ, SYS, PID2–PID31: Interrupt Clear**

0: No effect.

1: Clears corresponding interrupt.

25.9.15 AIC End of Interrupt Command Register

Name: AIC_EOICR

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	–

The End of Interrupt Command Register is used by the interrupt routine to indicate that the interrupt treatment is complete. Any value can be written because it is only necessary to make a write to this register location to signal the end of interrupt treatment.

28. Serial Peripheral Interface (SPI)

28.1 Description

The Serial Peripheral Interface (SPI) circuit is a synchronous serial data link that provides communication with external devices in Master or Slave Mode. It also enables communication between processors if an external processor is connected to the system.

The Serial Peripheral Interface is essentially a shift register that serially transmits data bits to other SPIs. During a data transfer, one SPI system acts as the “master”' which controls the data flow, while the other devices act as “slaves'' which have data shifted into and out by the master. Different CPUs can take turn being masters (Multiple Master Protocol opposite to Single Master Protocol where one CPU is always the master while all of the others are always slaves) and one master may simultaneously shift data into multiple slaves. However, only one slave may drive its output to write data back to the master at any given time.

A slave device is selected when the master asserts its NSS signal. If multiple slave devices exist, the master generates a separate slave select signal for each slave (NPCS).

The SPI system consists of two data lines and two control lines:

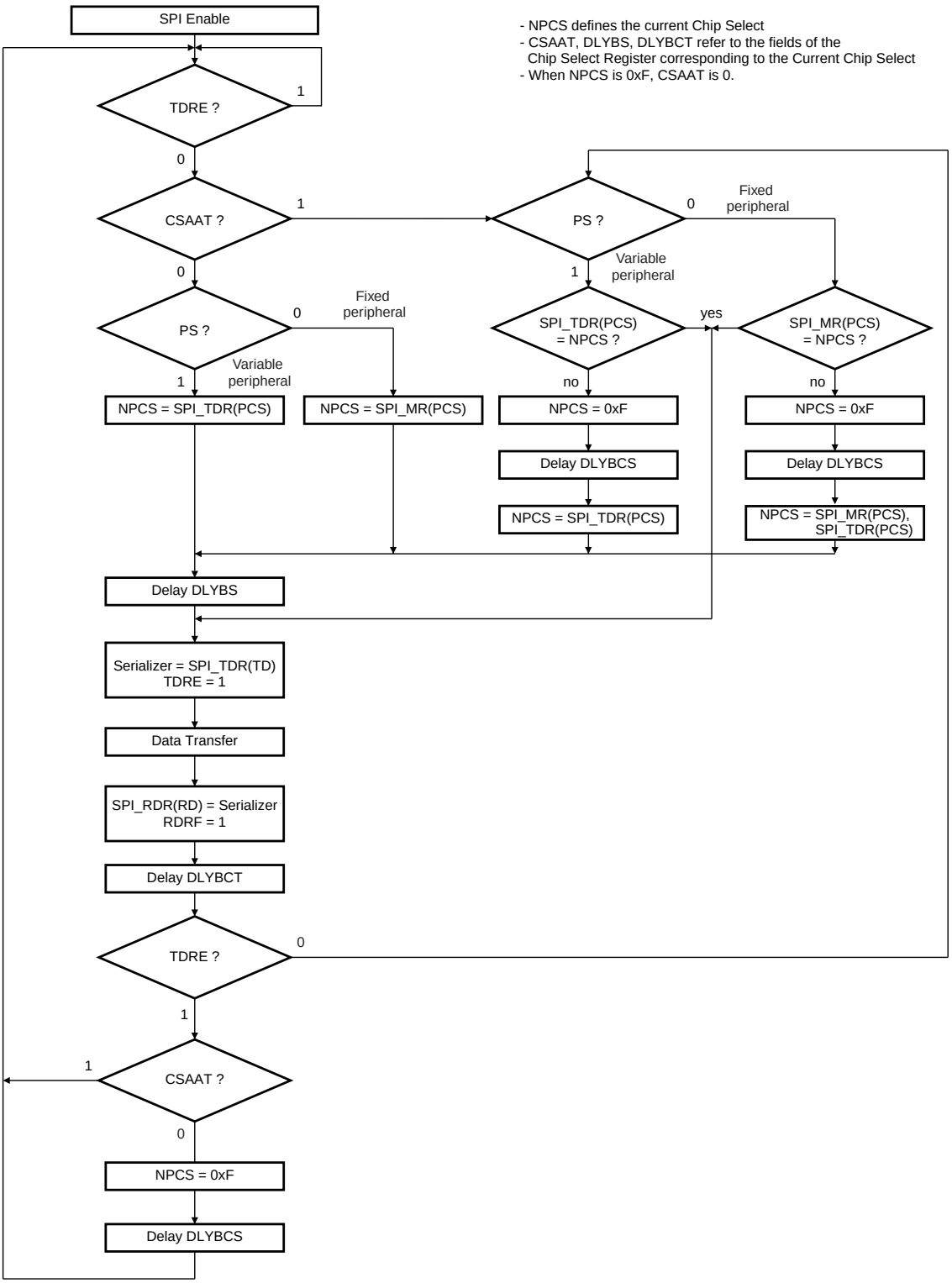
- Master Out Slave In (MOSI): This data line supplies the output data from the master shifted into the input(s) of the slave(s).
- Master In Slave Out (MISO): This data line supplies the output data from a slave to the input of the master. There may be no more than one slave transmitting data during any particular transfer.
- Serial Clock (SPCK): This control line is driven by the master and regulates the flow of the data bits. The master may transmit data at a variety of baud rates; the SPCK line cycles once for each bit that is transmitted.
- Slave Select (NSS): This control line allows slaves to be turned on and off by hardware.

28.2 Embedded Characteristics

- Supports communication with serial external devices
  - Four chip selects with external decoder support allow communication with up to 15 peripherals
  - Serial memories, such as DataFlash and 3-wire EEPROMs
  - Serial peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors
  - External co-processors
- Master or slave serial peripheral bus interface
  - 8- to 16-bit programmable data length per chip select
  - Programmable phase and polarity per chip select
  - Programmable transfer delays between consecutive transfers and between clock and data per chip select
  - Programmable delay between consecutive transfers
  - Selectable mode fault detection
- Very fast transfers supported
  - Transfers with baud rates up to MCK
  - The chip select line may be left active to speed up transfers on the same device

28.7.3.2 Master Mode Flow Diagram

Figure 28-6. Master Mode Flow Diagram S



28.8.1 SPI Control Register

Name: SPI_CR

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	LASTXFER
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
SWRST	–	–	–	–	–	SPIDIS	SPIEN

- **SPIEN: SPI Enable**

0: No effect.

1: Enables the SPI to transfer and receive data.

- **SPIDIS: SPI Disable**

0: No effect.

1: Disables the SPI.

As soon as SPIDIS is set, SPI finishes its transfer.

All pins are set in input mode and no data is received or transmitted.

If a transfer is in progress, the transfer is finished before the SPI is disabled.

If both SPIEN and SPIDIS are equal to one when the control register is written, the SPI is disabled.

- **SWRST: SPI Software Reset**

0: No effect.

1: Reset the SPI. A software-triggered hardware reset of the SPI interface is performed.

The SPI is in slave mode after software reset.

PDC channels are not affected by software reset.

- **LASTXFER: Last Transfer**

0: No effect.

1: The current NPCS will be deasserted after the character written in TD has been transferred. When CSAAT is set, this allows to close the communication with the current serial peripheral by raising the corresponding NPCS line as soon as TD transfer has completed.

28.8.3 SPI Receive Data Register

Name: SPI_RDR

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	PCS			

15	14	13	12	11	10	9	8
RD							

7	6	5	4	3	2	1	0
RD							

- **RD: Receive Data**

Data received by the SPI Interface is stored in this register right-justified. Unused bits read zero.

- **PCS: Peripheral Chip Select**

In Master Mode only, these bits indicate the value on the NPCS pins at the end of a transfer. Otherwise, these bits read zero.

Baud Rate Calculation Example

Table 30-2 shows calculations of CD to obtain a baud rate at 38400 baud for different source clock frequencies. This table also shows the actual resulting baud rate and the error.

Table 30-2. Baud Rate Example (OVER = 0)

Source Clock (MHz)	Expected Baud Rate (bit/s)	Calculation Result	CD	Actual Baud Rate (bit/s)	Error
3 686 400	38 400	6.00	6	38 400.00	0.00%
4 915 200	38 400	8.00	8	38 400.00	0.00%
5 000 000	38 400	8.14	8	39 062.50	1.70%
7 372 800	38 400	12.00	12	38 400.00	0.00%
8 000 000	38 400	13.02	13	38 461.54	0.16%
12 000 000	38 400	19.53	20	37 500.00	2.40%
12 288 000	38 400	20.00	20	38 400.00	0.00%
14 318 180	38 400	23.30	23	38 908.10	1.31%
14 745 600	38 400	24.00	24	38 400.00	0.00%
18 432 000	38 400	30.00	30	38 400.00	0.00%
24 000 000	38 400	39.06	39	38 461.54	0.16%
24 576 000	38 400	40.00	40	38 400.00	0.00%
25 000 000	38 400	40.69	40	38 109.76	0.76%
32 000 000	38 400	52.08	52	38 461.54	0.16%
32 768 000	38 400	53.33	53	38 641.51	0.63%
33 000 000	38 400	53.71	54	38 194.44	0.54%
40 000 000	38 400	65.10	65	38 461.54	0.16%
50 000 000	38 400	81.38	81	38 580.25	0.47%

The baud rate is calculated with the following formula:

$$BaudRate = MCK/CD \times 16$$

The baud rate error is calculated with the following formula. It is not recommended to work with an error higher than 5%.

$$Error = 1 - \left(\frac{ExpectedBaudRate}{ActualBaudRate}\right)$$

When operating in ISO7816, either in T = 0 or T = 1 modes, the character format is fixed. The configuration is 8 data bits, even parity and 1 or 2 stop bits, regardless of the values programmed in the CHRL, MODE9, PAR and CHMODE fields. MSBF can be used to transmit LSB or MSB first. Parity Bit (PAR) can be used to transmit in normal or inverse mode. Refer to “USART Mode Register” on page 474 and “PAR: Parity Type” on page 475.

The USART cannot operate concurrently in both receiver and transmitter modes as the communication is unidirectional at a time. It has to be configured according to the required mode by enabling or disabling either the receiver or the transmitter as desired. Enabling both the receiver and the transmitter at the same time in ISO7816 mode may lead to unpredictable results.

The ISO7816 specification defines an inverse transmission format. Data bits of the character must be transmitted on the I/O line at their negative value. The USART does not support this format and the user has to perform an exclusive OR on the data before writing it in the Transmit Holding Register (US_THR) or after reading it in the Receive Holding Register (US_RHR).

30.7.4.2 Protocol T = 0

In T = 0 protocol, a character is made up of one start bit, eight data bits, one parity bit and one guard time, which lasts two bit times. The transmitter shifts out the bits and does not drive the I/O line during the guard time.

If no parity error is detected, the I/O line remains at 1 during the guard time and the transmitter can continue with the transmission of the next character, as shown in Figure 30-21.

If a parity error is detected by the receiver, it drives the I/O line at 0 during the guard time, as shown in Figure 30-22. This error bit is also named NACK, for Non Acknowledge. In this case, the character lasts 1 bit time more, as the guard time length is the same and is added to the error bit time which lasts 1 bit time.

When the USART is the receiver and it detects an error, it does not load the erroneous character in the Receive Holding Register (US_RHR). It appropriately sets the PARE bit in the Status Register (US_SR) so that the software can handle the error.

Figure 30-21. T = 0 Protocol without Parity Error

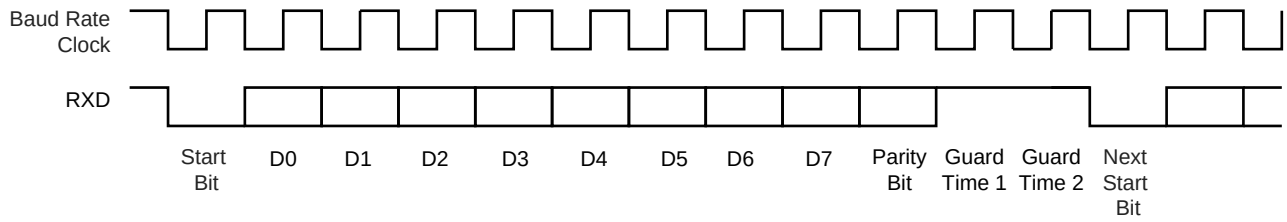
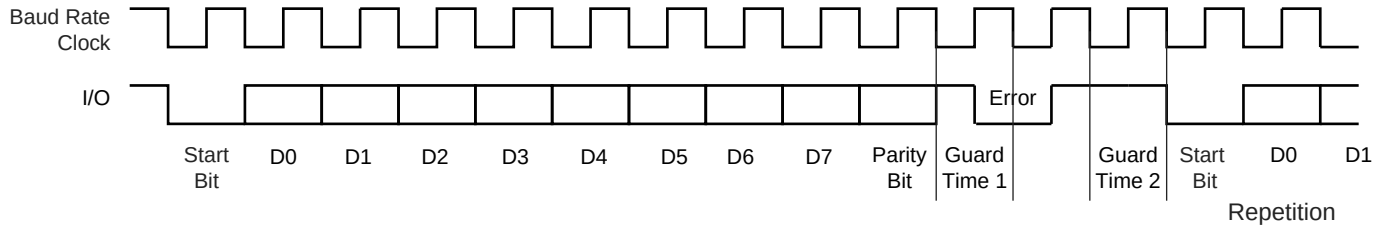


Figure 30-22. T = 0 Protocol with Parity Error



Receive Error Counter

The USART receiver also records the total number of errors. This can be read in the Number of Error (US_NER) register. The NB_ERRORS field can record up to 255 errors. Reading US_NER automatically clears the NB_ERRORS field.

30.8.4 USART Interrupt Disable Register

Name: US_IDR

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	CTSIC	DCDIC	DSRIC	RIIC

15	14	13	12	11	10	9	8
–	–	NACK	RXBUFF	TXBUFE	ITER	TXEMPTY	TIMEOUT

7	6	5	4	3	2	1	0
PARE	FRAME	OVRE	ENDTX	ENDRX	RXBRK	TXRDY	RXRDY

- **RXRDY: RXRDY Interrupt Disable**
- **TXRDY: TXRDY Interrupt Disable**
- **RXBRK: Receiver Break Interrupt Disable**
- **ENDRX: End of Receive Transfer Interrupt Disable**
- **ENDTX: End of Transmit Interrupt Disable**
- **OVRE: Overrun Error Interrupt Disable**
- **FRAME: Framing Error Interrupt Disable**
- **PARE: Parity Error Interrupt Disable**
- **TIMEOUT: Time-out Interrupt Disable**
- **TXEMPTY: TXEMPTY Interrupt Disable**
- **ITER: Iteration Interrupt Enable**
- **TXBUFE: Buffer Empty Interrupt Disable**
- **RXBUFF: Buffer Full Interrupt Disable**
- **NACK: Non Acknowledge Interrupt Disable**
- **RIIC: Ring Indicator Input Change Disable**
- **DSRIC: Data Set Ready Input Change Disable**
- **DCDIC: Data Carrier Detect Input Change Interrupt Disable**
- **CTSIC: Clear to Send Input Change Interrupt Disable**

31.5 Pin Name List

Table 31-1. I/O Lines Description

Pin Name	Pin Description	Type
RF	Receiver Frame Synchro	Input/Output
RK	Receiver Clock	Input/Output
RD	Receiver Data	Input
TF	Transmitter Frame Synchro	Input/Output
TK	Transmitter Clock	Input/Output
TD	Transmitter Data	Output

31.6 Product Dependencies

31.6.1 I/O Lines

The pins used for interfacing the compliant external devices may be multiplexed with PIO lines.

Before using the SSC receiver, the PIO controller must be configured to dedicate the SSC receiver I/O lines to the SSC peripheral mode.

Before using the SSC transmitter, the PIO controller must be configured to dedicate the SSC transmitter I/O lines to the SSC peripheral mode.

31.6.2 Power Management

The SSC is not continuously clocked. The SSC interface may be clocked through the Power Management Controller (PMC), therefore the programmer must first configure the PMC to enable the SSC clock.

31.6.3 Interrupt

The SSC interface has an interrupt line connected to the Advanced Interrupt Controller (AIC). Handling interrupts requires programming the AIC before configuring the SSC.

All SSC interrupts can be enabled/disabled configuring the SSC Interrupt mask register. Each pending and unmasked SSC interrupt will assert the SSC interrupt line. The SSC interrupt service routine can get the interrupt origin by reading the SSC interrupt status register.

31.7.1 Clock Management

The transmitter clock can be generated by:

- an external clock received on the TK I/O pad
- the receiver clock
- the internal clock divider

The receiver clock can be generated by:

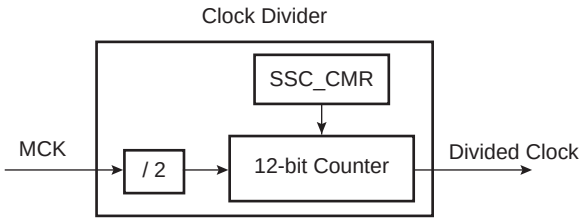
- an external clock received on the RK I/O pad
- the transmitter clock
- the internal clock divider

Furthermore, the transmitter block can generate an external clock on the TK I/O pad, and the receiver block can generate an external clock on the RK I/O pad.

This allows the SSC to support many Master and Slave Mode data transfers.

31.7.1.1 Clock Divider

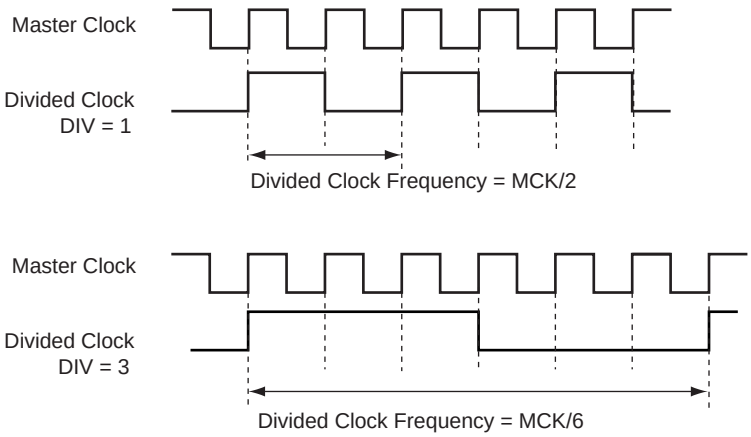
Figure 31-4. Divided Clock Block Diagram



The Master Clock divider is determined by the 12-bit field DIV counter and comparator (so its maximal value is 4095) in the Clock Mode Register SSC_CMR, allowing a Master Clock division by up to 8190. The Divided Clock is provided to both the Receiver and Transmitter. When this field is programmed to 0, the Clock Divider is not used and remains inactive.

When DIV is set to a value equal to or greater than 1, the Divided Clock has a frequency of Master Clock divided by 2 times DIV. Each level of the Divided Clock has a duration of the Master Clock multiplied by DIV. This ensures a 50% duty cycle for the Divided Clock regardless of whether the DIV value is even or odd.

Figure 31-5. Divided Clock Generation



31.9.15 SSC Interrupt Disable Register

Name: SSC_IDR

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	RXSYN	TXSYN	CP1	CP0
7	6	5	4	3	2	1	0
RXBUFF	ENDRX	OVRUN	RXRDY	TXBUFE	ENDTX	TXEMPTY	TXRDY

- **TXRDY: Transmit Ready Interrupt Disable**

0: No effect.

1: Disables the Transmit Ready Interrupt.

- **TXEMPTY: Transmit Empty Interrupt Disable**

0: No effect.

1: Disables the Transmit Empty Interrupt.

- **ENDTX: End of Transmission Interrupt Disable**

0: No effect.

1: Disables the End of Transmission Interrupt.

- **TXBUFE: Transmit Buffer Empty Interrupt Disable**

0: No effect.

1: Disables the Transmit Buffer Empty Interrupt.

- **RXRDY: Receive Ready Interrupt Disable**

0: No effect.

1: Disables the Receive Ready Interrupt.

- **OVRUN: Receive Overrun Interrupt Disable**

0: No effect.

1: Disables the Receive Overrun Interrupt.

- **ENDRX: End of Reception Interrupt Disable**

0: No effect.

1: Disables the End of Reception Interrupt.

- **RXBUFF: Receive Buffer Full Interrupt Disable**

0: No effect.

1: Disables the Receive Buffer Full Interrupt.

- **FRATE: Frame rate [0..7]**

0: All the frames are captured, else one frame every FRATE + 1 is captured.

- **FULL: Full mode is allowed**

1: Both codec and preview datapaths are working simultaneously.

- **THMASK: Threshold mask**

0: 4, 8 and 16 AHB bursts are allowed.

1: 8 and 16 AHB bursts are allowed.

2: Only 16 AHB bursts are allowed.

- **CODEC_ON: Enable the codec path enable bit**

Write-only.

0: The codec path is disabled.

1: The codec path is enabled and the next frame is captured. Refer to bit CDC_PND in “ISI Status Register” on page 725.

- **SLD: Start of Line Delay**

SLD pixel clock periods to wait before the beginning of a line.

- **SFD: Start of Frame Delay**

SFD lines are skipped at the beginning of the frame.

Table 44-1. Revision History - SAM9620 Datasheet Revision 6221M (Continued)

Date	Comments
13-Jan-16	Section 22. “Peripheral DMA Controller (PDC)” Table 22-1 “Register Mapping”: removed reset value from PERIPH_PTCR (register is write-only)
	Section 24. “Power Management Controller (PMC)” Table 24-3 “Register Mapping”: access for PMC_PLLICPR changed from “Write-only” to “Read/Write” Section 24.9.17 “PLL Charge Pump Current Register”: access changed from “Write-only” to “Read/Write”
	Section 25. “Advanced Interrupt Controller (AIC)” Removed reset value from register description sections (reset values are provided in Table 25-2 “Register Mapping”)
	Section 29. “Two-wire Interface (TWI)” Table 29-4 “Register Mapping”: removed reset value from TW_THR (register is write-only) Removed reset value from register description sections (reset values are provided in Table 29-4 “Register Mapping”) Section 29.8.11 “TWI Transmit Holding Register”: access “Read-write” corrected to “Write-only”
	Section 30. “Universal Synchronous Asynchronous Receiver Transmitter (USART)” Table 30-5 “Possible Values for the Fi/Di Ratio”: in top row, replaced “774” with “744” Table 30-10 “IrDA Baud Rate Error”: in header row, added “bit/s” to Baud Rate and added “µs” to Pulse Time Table 30-12 “Register Mapping”: added reset value 0x0 to US_MR, US_CSR, US_NER Removed reset value from Section 30.8.12 “USART FI DI RATIO Register” (reset values are provided in Table 30-12 “Register Mapping”)
	Section 31. “Synchronous Serial Controller (SSC)” Section 31.7.1.1 “Clock Divider”: deleted irrelevant and untitled Table 31-2 from end of section
	Section 32. “Timer Counter (TC)” Updated Table 32-2 “Channel Signal Description”
	Section 33. “MultiMedia Card Interface (MCI)” Section 33.1 “Description”: “MultiMedia Card (MMC) Specification V3.11” updated to “MultiMedia Card (MMC) Specification V3.31” Updated Section 33.2 “Embedded Characteristics” Section 33.8.1 “Command - Response Operation”: updated text and Figure 33-9 ”Command/Response Functional Flow Diagram” with “busy indication” and “NOTBUSY” flag
	Section 34. “Ethernet MAC 10/100 (EMAC)” Section 34.6.2 “Network Configuration Register”: updated EFRHD bit description
	Section 37. “Image Sensor Interface (ISI)” Table 37-9 “Register Mapping”: - ISI_SR: access “Read” corrected to “Read-only” - ISI_IER and ISI_IDR: access “Read/Write” corrected to “Write-only”; removed reset value - ISI_IMR: access “Read/Write” corrected to “Read-only” Removed reset value from register description sections (reset values are provided in Table 37-9 “Register Mapping”) Section 37.5.3 “ISI Status Register”: access “Read” corrected to “Read-only” Section 37.5.4 “Interrupt Enable Register” and Section 37.5.5 “ISI Interrupt Disable Register”: access “Read/Write” corrected to “Write-only” Section 37.5.6 “ISI Interrupt Mask Register”: access “Read/Write” corrected to “Read-only”

Revision 6221I	Comments (Continued)	Change Request Ref
	‘selectable by software’ removed from Table 39-2 on page 760	6402
	VDDPLL value range for t_{st} changed in Table 39-11 on page 765	6425
	- Features shortened and reorganized, from new structure in Datasheet AT91SAM9G45 - Section 7.5 “Backup Section” on page 26 added - Information from sections 7.1 to 7.4 moved to sections 11.2, 19.2, 24.2 and 12.2, with ‘Embedded Characteristics’ header - Information from sections 9.2 to 9.4, 9.6 to 9.8 and 9.10 to 9.11to 7.4 moved to sections 13.2, 18.2, 25.2, 17.2, 16.2, 15.2, 27.2 and 28.2, with ‘Embedded Characteristics’ header - Information from sections 10.4.1 to 10.4.11 moved to sections 30.2 to 35.2, 38.2, 37.2, 36.2, 39.2 and 4.2, with ‘Embedded Characteristics’ header - Sections 41.5.3 and 41.5.4 moved after Section 39.6.4 “Crystal Characteristics” on page 766	RFO

Revision 6221H	Comments	Change Request Ref
	**Section 42. “SAM9260 Ordering Information”,** Ordering codes updated for revision B of the device.	5686
6221H	Table 8-3, “Multiplexing on PIO Controller B”, PB31 line, removed ISI_MCK. Table 2-1, “Signal Description List”, Reset/Test, BMS line, added comments.	5330 5422
	AT91SAM9260 Boot Program Figure 11-2 ”Clocks and DBGU Configurations”, flow chart replaced.	 5441
	Section 17.6 “Bus Matrix User Interface” Table 17-4, “Register Mapping”; MATRIX_MCFG0 reset is 0x2, MATRIX_MCFG5 is Read-only. Section 17.6.1 “Bus Matrix Master Configuration Registers”, added note, “MATRIX_MCFG5 is write only....”	5489
	Table 16.7, “Shutdown Controller (SHDWC) User Interface” SHDW_MR address is 0x0000_0303	5703
	Section 39. “SAM9260 Electrical Characteristics” Table 39-11, “Main Oscillator Characteristics”, C_{LEXT} typ values updated and typo fixed in Unit column. Figure 39-10 ”SPI Master Mode 1 and 2”, title fixed. Figure 39-11 ”SPI Master Mode 0 and 3”, title fixed. Figure 39-16 ”USB Data Signal Timing Diagram”, R_{EXT} = 27 ohms.	 5331 5261
	Section 43.1 “SAM9260 Errata - Revision “A” Parts” Section 43.1.3 “Bus Matrix”, added to errata. Section 43.1.10.3 “SPI: PDC Data Loss”, added to errata. Section 43.1.5 “I/O Considerations”, was formerly SMC errata Section 43.1.5.1 “I/O High Drive Strength”, was formerly listed under SMC errata	 rfo 5328 5548
	Section 43.2 “SAM9260 Errata - Revision “B” Parts” Section 43.2.2 “Bus Matrix”,	 rfo