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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	180MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM, SRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps
SATA	-
USB	USB 2.0 (2)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at91sam9260b-qu

11.5 NAND Flash Boot

The NAND Flash Boot program searches for a valid application in the NAND Flash memory. The first block must be guaranteed by the manufacturer. There is no ECC.

The NAND Flash Boot program searches for a valid application in the NAND Flash memory. If a valid application is found, this application is loaded into internal SRAM and executed by branching at address 0x0000_0000 after remap. See “DataFlash Boot” on page 71 for more information on Valid Image Detection.

Note: It is not necessary to indicate size to download in ARM vector 6 as 4096 bytes are downloaded in every case.

11.5.1 Supported NAND Flash Devices

Any 8 or 16-bits NAND Flash Devices from 1 Mbit to 16 Gbit density are supported.

Table 11-6. Supported NAND Flash Manufacturers

Manufacturer	Identifier
TOSHIBA	0x98
SAMSUNG	0xEC
FUJITSU	0x04
NATIONAL Semiconductor	0x8F
RENESAS	0x07
ST Microelectronics	0x20
MICRON	0x2C

17.6.4 Bus Matrix Master Remap Control Register

Name: MATRIX_MRCR

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	–	RCB1	RCB0

- **RCBx: Remap Command Bit for AHB Master x**

0: Disable remapped address decoding for the selected Master

1: Enable remapped address decoding for the selected Master

Table 18-4. EBI Pins and External Device Connections (Continued)

	Pins of the Interfaced Device			
	SDRAMC	SMC		
Signals: EBI_	SDRAM	CompactFlash (EBI only)	CompactFlash True IDE Mode (EBI only)	NAND Flash
CFCE2	–	CE2	CS1	–
SDCK	CLK	–	–	–
SDCKE	CKE	–	–	–
RAS	RAS	–	–	–
CAS	CAS	–	–	–
SDWE	WE	–	–	–
NWAIT	–	WAIT	WAIT	–
Pxx [2]	–	CD1 or CD2	CD1 or CD2	–
Pxx [2]	–	–	–	CE [3]
Pxx [2]	–	–	–	RDY

Notes:
1. Not directly connected to the CompactFlash slot. Permits the control of the bidirectional buffer between the EBI data bus and the CompactFlash slot.
2. Any PIO line.
3. CE connection depends on the NAND Flash. For standard NAND Flash devices, it must be connected to any free PIO line. For “CE don't care” NAND Flash devices, it can be either connected to NCS3/NANDCS or to any free PIO line.

21.3 Functional Description

A page in NAND Flash and SmartMedia memories contains an area for main data and an additional area used for redundancy (ECC). The page is organized in 8-bit or 16-bit words. The page size corresponds to the number of words in the main area plus the number of words in the extra area used for redundancy.

The only configuration required for ECC is the NAND Flash or the SmartMedia page size (528/1056/2112/4224). Page size is configured setting the PAGESIZE field in the ECC Mode Register (ECC_MR).

ECC is automatically computed as soon as a read (00h)/write (80h) command to the NAND Flash or the SmartMedia is detected. Read and write access must start at a page boundary.

ECC results are available as soon as the counter reaches the end of the main area. Values in the ECC Parity Register (ECC_PR) and ECC NParity Register (ECC_NPR) are then valid and locked until a new start condition occurs (read/write command followed by address cycles).

21.3.1 Write Access

Once the flash memory page is written, the computed ECC code is available in the ECC Parity Error (ECC_PR) and ECC_NParity Error (ECC_NPR) registers. The ECC code value must be written by the software application in the extra area used for redundancy.

21.3.2 Read Access

After reading the whole data in the main area, the application must perform read accesses to the extra area where ECC code has been previously stored. Error detection is automatically performed by the ECC controller. Please note that it is mandatory to read consecutively the entire main area and the locations where Parity and NParity values have been previously stored to let the ECC controller perform error detection.

The application can check the ECC Status Register (ECC_SR) for any detected errors.

It is up to the application to correct any detected error. ECC computation can detect four different circumstances:

- No error: XOR between the ECC computation and the ECC code stored at the end of the NAND Flash or SmartMedia page is equal to 0. No error flags in the ECC Status Register (ECC_SR).
- Recoverable error: Only the RECERR flag in the ECC Status register (ECC_SR) is set. The corrupted word offset in the read page is defined by the WORDADDR field in the ECC Parity Register (ECC_PR). The corrupted bit position in the concerned word is defined in the BITADDR field in the ECC Parity Register (ECC_PR).
- ECC error: The ECCERR flag in the ECC Status Register is set. An error has been detected in the ECC code stored in the Flash memory. The position of the corrupted bit can be found by the application performing an XOR between the Parity and the NParity contained in the ECC code stored in the flash memory.
- Non correctable error: The MULERR flag in the ECC Status Register is set. Several unrecoverable errors have been detected in the flash memory page.

ECC Status Register, ECC Parity Register and ECC NParity Register are cleared when a read/write command is detected or a software reset is performed.

For Single-bit Error Correction and Double-bit Error Detection (SEC-DED) hsiao code is used. 32-bit ECC is generated in order to perform one bit correction per 512/1024/2048/4096 8- or 16-bit words. Of the 32 ECC bits, 26 bits are for line parity and 6 bits are for column parity. They are generated according to the schemes shown in Figure 21-2 and Figure 21-3.

To calculate P8’ to PX’ and P8 to PX, apply the algorithm that follows.

Page size = 2^n

```
for i =0 to n
begin
 for (j = 0 to page_size_word)
 begin
  if(j[i] ==1)
   P[2^(i+3)]= bit15(+)bit14(+)bit13(+)bit12(+)
               bit11(+)bit10(+)bit9(+)bit8(+)
               bit7(+)bit6(+)bit5(+)bit4(+)bit3(+)
               bit2(+)bit1(+)bit0(+)P[2^(n+3)]
  else
   P[2^(i+3)]’=bit15(+)bit14(+)bit13(+)bit12(+)
               bit11(+)bit10(+)bit9(+)bit8(+)
               bit7(+)bit6(+)bit5(+)bit4(+)bit3(+)
               bit2(+)bit1(+)bit0(+)P[2^(i+3)]'
  end
end
```

22. Peripheral DMA Controller (PDC)

22.1 Description

The Peripheral DMA Controller (PDC) transfers data between on-chip serial peripherals and the on- and/or off-chip memories. The link between the PDC and a serial peripheral is operated by the AHB to ABP bridge.

The PDC contains 22 channels. The full-duplex peripherals feature 21 mono directional channels used in pairs (transmit only or receive only). The half-duplex peripherals feature 1 bi-directional channels.

The user interface of each PDC channel is integrated into the user interface of the peripheral it serves. The user interface of mono directional channels (receive only or transmit only), contains two 32-bit memory pointers and two 16-bit counters, one set (pointer, counter) for current transfer and one set (pointer, counter) for next transfer. The bi-directional channel user interface contains four 32-bit memory pointers and four 16-bit counters. Each set (pointer, counter) is used by current transmit, next transmit, current receive and next receive.

Using the PDC removes processor overhead by reducing its intervention during the transfer. This significantly reduces the number of clock cycles required for a data transfer, which improves microcontroller performance.

To launch a transfer, the peripheral triggers its associated PDC channels by using transmit and receive signals. When the programmed data is transferred, an end of transfer interrupt is generated by the peripheral itself.

24.9.13 PMC Interrupt Enable Register

Name: PMC_IER

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	PCKRDY1	PCKRDY0
7	6	5	4	3	2	1	0
–	–	–	–	MCKRDY	LOCKB	LOCKA	MOSCS

- **MOSCS: Main Oscillator Status Interrupt Enable**
- **LOCKA: PLL A Lock Interrupt Enable**
- **LOCKB: PLL B Lock Interrupt Enable**
- **MCKRDY: Master Clock Ready Interrupt Enable**
- **PCKRDYx: Programmable Clock Ready x Interrupt Enable**

0: No effect.

1: Enables the corresponding interrupt.

27.6.26 PIO Peripheral A B Status Register

Name: PIO_ABSR

Access: Read-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

- **P0–P31: Peripheral A B Status**

0: The I/O line is assigned to the Peripheral A.

1: The I/O line is assigned to the Peripheral B.

28.8.8 SPI Interrupt Mask Register

Name: SPI_IMR

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	TXEMPTY	NSSR
7	6	5	4	3	2	1	0
TXBUFE	RXBUFF	ENDTX	ENDRX	OVRES	MODF	TDRE	RDRF

- **RDRF: Receive Data Register Full Interrupt Mask**
- **TDRE: SPI Transmit Data Register Empty Interrupt Mask**
- **MODF: Mode Fault Error Interrupt Mask**
- **OVRES: Overrun Error Interrupt Mask**
- **ENDRX: End of Receive Buffer Interrupt Mask**
- **ENDTX: End of Transmit Buffer Interrupt Mask**
- **RXBUFF: Receive Buffer Full Interrupt Mask**
- **TXBUFE: Transmit Buffer Empty Interrupt Mask**
- **TXEMPTY: Transmission Registers Empty Mask**
- **NSSR: NSS Rising Interrupt Mask**

0: The corresponding interrupt is not enabled.

1: The corresponding interrupt is enabled.

29.8.4 TWI Internal Address Register

Name: TWI_IADR

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
IADR							

15	14	13	12	11	10	9	8
IADR							

7	6	5	4	3	2	1	0
IADR							

- **IADR: Internal Address**

0, 1, 2 or 3 bytes depending on IADRSZ.

30.7.5.2 IrDA Baud Rate

Table 30-10 gives some examples of CD values, baud rate error and pulse duration. Note that the requirement on the maximum acceptable error of ±1.87% must be met.

Table 30-10. IrDA Baud Rate Error

Peripheral Clock	Baud Rate (bit/s)	CD	Baud Rate Error	Pulse Time (µs)
3 686 400	115 200	2	0.00%	1.63
20 000 000	115 200	11	1.38%	1.63
32 768 000	115 200	18	1.25%	1.63
40 000 000	115 200	22	1.38%	1.63
3 686 400	57 600	4	0.00%	3.26
20 000 000	57 600	22	1.38%	3.26
32 768 000	57 600	36	1.25%	3.26
40 000 000	57 600	43	0.93%	3.26
3 686 400	38 400	6	0.00%	4.88
20 000 000	38 400	33	1.38%	4.88
32 768 000	38 400	53	0.63%	4.88
40 000 000	38 400	65	0.16%	4.88
3 686 400	19 200	12	0.00%	9.77
20 000 000	19 200	65	0.16%	9.77
32 768 000	19 200	107	0.31%	9.77
40 000 000	19 200	130	0.16%	9.77
3 686 400	9 600	24	0.00%	19.53
20 000 000	9 600	130	0.16%	19.53
32 768 000	9 600	213	0.16%	19.53
40 000 000	9 600	260	0.16%	19.53
3 686 400	2 400	96	0.00%	78.13
20 000 000	2 400	521	0.03%	78.13
32 768 000	2 400	853	0.04%	78.13

32.3 Block Diagram

Figure 32-1. Timer Counter Block Diagram

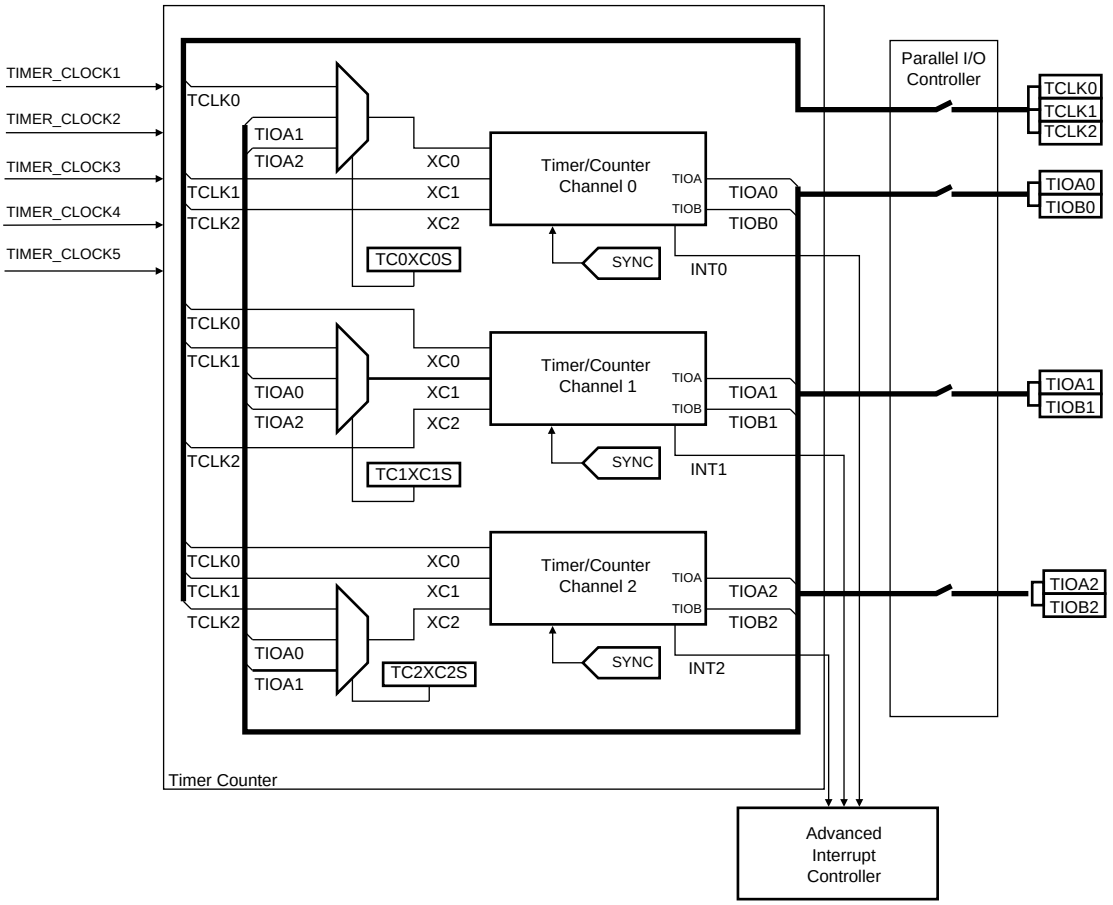


Table 32-2. Channel Signal Description

Signal Name	Description
XC0, XC1, XC2	External Clock Inputs
TIOA	Capture Mode: Timer Counter Input Waveform Mode: Timer Counter Output
TIOB	Capture Mode: Timer Counter Input Waveform Mode: Timer Counter Input/Output
INT	Interrupt Signal Output
SYNC	Synchronization Input Signal

32.4 Pin Name List

Table 32-3. TC Pin List

Pin Name	Description	Type
TCLK0–TCLK2	External Clock Input	Input
TIOA0–TIOA2	I/O Line A	I/O
TIOB0–TIOB2	I/O Line B	I/O

34.6.16 Specific Address 1 Bottom Register

Name: EMAC_SA1B

Access: Read/Write

31	30	29	28	27	26	25	24
ADDR							

23	22	21	20	19	18	17	16
ADDR							

15	14	13	12	11	10	9	8
ADDR							

7	6	5	4	3	2	1	0
ADDR							

- **ADDR**

Least significant bits of the destination address. Bit zero indicates whether the address is multicast or unicast and corresponds to the least significant bit of the first byte received.

- **EXTRSM: UDP External Resume Interrupt Status**

0: No UDP External Resume Interrupt pending.

1: UDP External Resume Interrupt has been raised.

- **SOFINT: Start of Frame Interrupt Status**

0: No Start of Frame Interrupt pending.

1: Start of Frame Interrupt has been raised.

This interrupt is raised each time a SOF token has been detected. It can be used as a synchronization signal by using isochronous endpoints.

- **ENDBUSRES: End of BUS Reset Interrupt Status**

0: No End of Bus Reset Interrupt pending.

1: End of Bus Reset Interrupt has been raised.

This interrupt is raised at the end of a UDP reset sequence. The USB device must prepare to receive requests on the endpoint 0. The host starts the enumeration, then performs the configuration.

- **WAKEUP: UDP Resume Interrupt Status**

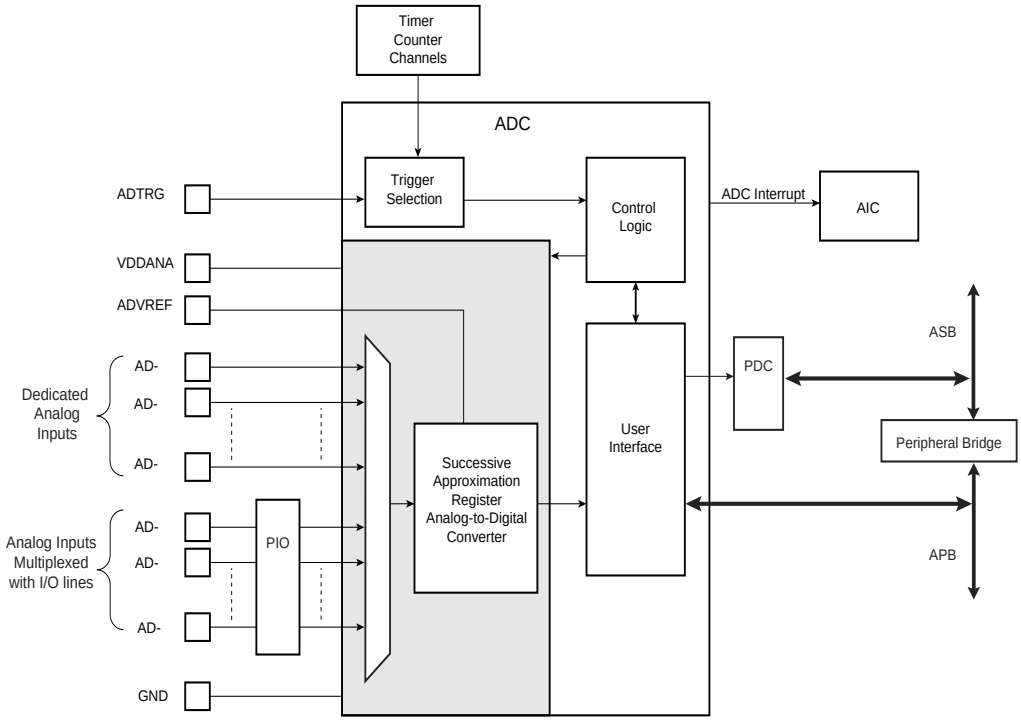
0: No Wakeup Interrupt pending.

1: A Wakeup Interrupt (USB Host Sent a RESUME or RESET) occurred since the last clear.

After reset the state of this bit is undefined, the application must clear this bit by setting the WAKEUP flag in the UDP_ICR.

38.3 Block Diagram

Figure 38-1. Analog-to-Digital Converter Block Diagram



38.4 Signal Description

Table 38-1. ADC Pin Description

Pin Name	Description
VDDANA	Analog power supply
ADVREF	Reference voltage
AD0–AD3	Analog input channels
ADTRG	External trigger

38.5 Product Dependencies

38.5.1 Power Management

The ADC is automatically clocked after the first conversion in Normal Mode. In Sleep Mode, the ADC clock is automatically stopped after each conversion. As the logic is small and the ADC cell can be put into Sleep Mode, the Power Management Controller has no effect on the ADC behavior.

38.5.2 Interrupt Sources

The ADC interrupt line is connected on one of the internal sources of the Advanced Interrupt Controller. Using the ADC interrupt requires the AIC to be programmed first.

38.5.3 Analog Inputs

The analog input pins can be multiplexed with PIO lines. In this case, the assignment of the ADC input is automatically done as soon as the corresponding channel is enabled by writing the register ADC_CHER. By default, after reset, the PIO line is configured as input with its pull-up enabled and the ADC input is connected to the GND.

38.5.4 I/O Lines

The pin ADTRG may be shared with other peripheral functions through the PIO Controller. In this case, the PIO Controller should be set accordingly to assign the pin ADTRG to the ADC function.

38.5.5 Timer Triggers

Timer Counters may or may not be used as hardware triggers depending on user requirements. Thus, some or all of the timer counters may be non-connected.

38.5.6 Conversion Performances

For performance and electrical characteristics of the ADC, see the DC Characteristics section.

Figure 40-3. 208-lead PQFP: Pin 1 Position

One or two ink (or laser) dots may be present on top of the package.

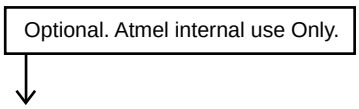
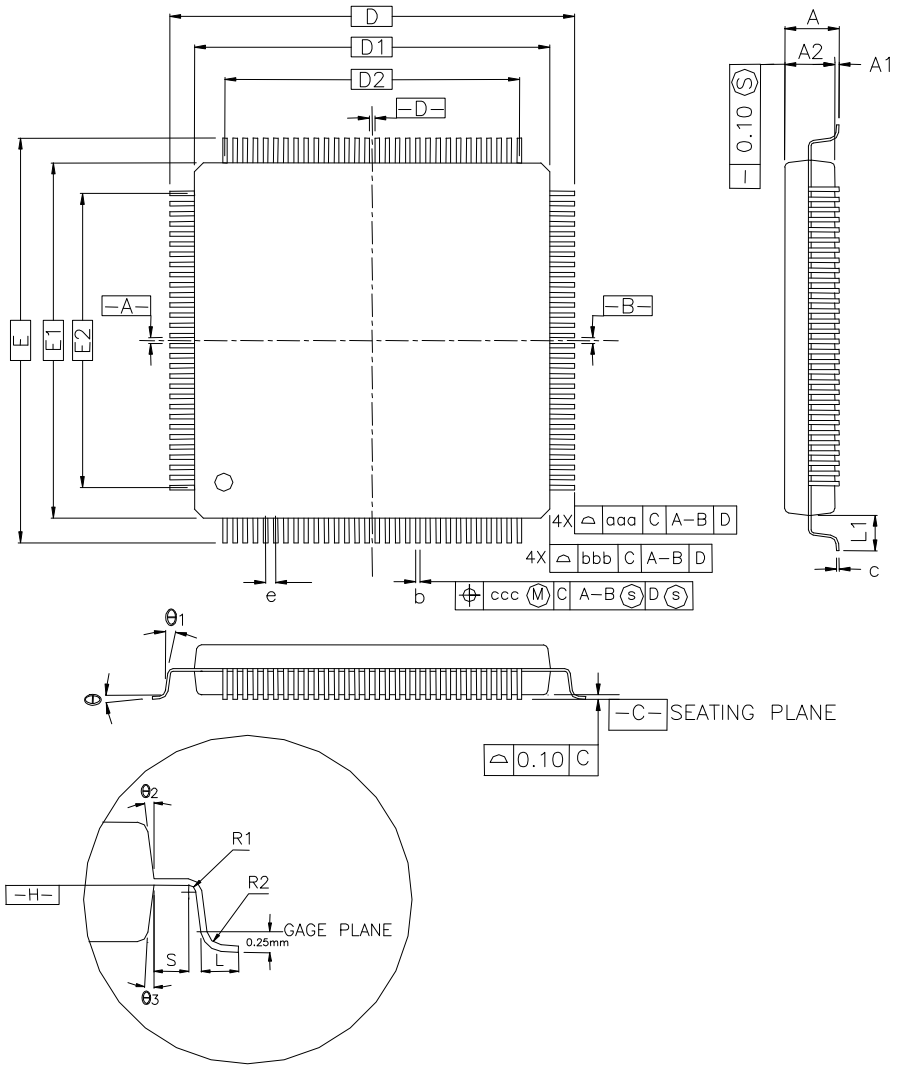


Figure 40-4. 208-lead PQFP Package Drawing



CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	4.10	—	—	0.161
A1	0.25	—	—	0.010	—	—
A2	3.20	3.32	3.60	0.126	0.131	0.142
D	31.20 BASIC			1.228 BASIC		
D1	28.00 BASIC			1.102 BASIC		
E	31.20 BASIC			1.228 BASIC		
E1	28.00 BASIC			1.102 BASIC		
R2	0.13	—	0.30	0.005	—	0.012
R1	0.13	—	—	0.005	—	—
θ	0°	—	7°	0°	—	7°
θ1	0°	—	—	0°	—	—
θ2	8° REF			8° REF		
θ3	8° REF			8° REF		
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L1	1.60 REF			0.063 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	25.50			1.004		
E2	25.50			1.004		
TOLERANCES OF FORM AND POSITION						
aaa	0.25			0.010		
bbb	0.20			0.008		
ccc	0.08			0.003		

43.1.17 USART

43.1.17.1 USART: TXD Signal is Floating in Modem and Hardware Handshaking Mode.

TXD signal should be pulled up in Modem and Hardware Handshaking mode.

Problem Fix/Workaround

TXD is multiplexed with PIO which integrates a pull up resistor. This internal pull-up must be enabled.

43.1.17.2 USART: DCD is Active High Instead of Low

The DCD signal is active at High level in the USART Modem Mode.

DCD should be active at Low level.

Problem Fix/Workaround

Add an inverter.

43.1.17.3 USART: RXBRK Flag Error in Asynchronous Mode

In receiver mode, when two characters are consecutive (without timeguard in between) the RXBRK is not taken into account. As a result the RXBRK flag is not enabled correctly and the frame error flag is set.

Problem Fix/Workaround

Constraints on the transmitter device connected to the SAM9260 USART receiver side.

The transmitter may use the timeguard feature or send 2 STOP conditions. Only one STOP condition is taken into account by the receiver state machine. After this STOP condition, as there is no valid data the receiver state machine will go into idle mode and enable the RXBRK condition.

43.1.17.4 USART: CTS Signal in Hardware Handshake

When Hardware Handshaking is used and if CTS goes low near the end of the starting bit of the transmitter, a character is lost.

Problem Fix/Workaround

CTS must not go low during a time slot comprised between 2 Master Clock periods before the rising edge of the starting bit and 16 Master Clock periods after the rising edge of the starting bit.

43.1.17.5 USART: RTS Not Expected Behavior

1. Setting the receiver to hardware handshaking mode drops RTS line to low level even if the receiver is still turned off. USART needs to be completely configured and started before setting the receiver to hardware handshaking mode.
2. Disabling the receiver during a PDC transfer while RXBUFF flag is '0' has no effect on RTS. The only way to get the RTS line to rise to high level is to reset both PDMA buffers by writing the value '0' in both counter registers.

Problem Fix/Workaround

None.

43.1.17.6 USART: Two Characters Sent if CTS Rises During Emission

If CTS rises to 1 during a character transmit, the Transmit Holding Register is also transmitted if not empty.

Problem Fix/Workaround

None.

43.2.11 System Controller

43.2.11.1 Possible Event Loss when Reading RTT_SR

If an event (RTTINC or ALMS) occurs within the same slow clock cycle as when the RTT_SR is read, the corresponding bit might be cleared. This can lead to the loss of this event.

Problem Fix/Workaround

The software must handle an RTT event as an interrupt and should not poll RTT_SR.

43.2.12 Two-wire Interface (TWI)

43.2.12.1 TWI: Switch from Slave to Master Mode

At the end of transfer in slave mode, the slave mode is disabled, the master mode is enabled and thus a transfer in master mode can be performed. In the current device, the start event is correctly generated but the SCL line is stuck at 1, so no transfer is possible.

Problem Fix/Workaround

Two workarounds are possible:

1. Perform a software reset before going to master mode (TWI must be reconfigured).

or

2. Perform a slave read access before switching to master mode.

43.2.13 UHP

43.2.13.1 UHP: Non-ISO IN Transfers

Conditions:

Consider the following sequence:

1. The Host controller issues an IN token.
2. The Device provides the IN data in a short packet.
3. The Host controller writes the received data to the system memory.
4. The Host controller is now supposed to carry out two Write transactions (TD status write and TD retirement write) to the system memory in order to complete the status update.
5. The Host controller raises the request for the first write transaction. By the time the transaction is completed, a frame boundary is crossed.
6. After completing the first write transaction, the Host controller skips the second write transaction.

Consequence: When this error occurs, the Host controller tries the same IN token again.

Problem Fix/Workaround

This problem can be avoided if the system guarantees that the status update can be completed within the same frame.

43.2.13.2 UHP: ISO OUT Transfers

Conditions:

Consider the following sequence:

1. The Host controller sends an ISO OUT token after fetching 16 bytes of data from the system memory.
2. When the Host controller is sending the ISO OUT data, because of system latencies, remaining bytes of the packet are not available. This results in a buffer underrun condition.
3. While there is an underrun condition, if the Host controller is in the process of bit-stuffing, it causes the Host controller to hang.

Revision	Comments	Change Request Ref.
6221D continued	TC: Added information on compare register B and waveform generation in Section 32.6.12 “External Event/Trigger Conditions” on page 545. Added Note (1) to Register Bit Description“EEVT: External Event Selection” on page 553 in “TC Channel Mode Register: Waveform Mode” to further clarify. Added Figure 32-2, ”Clock Chaining Selection” on page 535 to demonstrate clock chaining.	2704 3342
	EMAC: ”Interrupt Enable Register” on page 609, access changed to Write-only. ”Interrupt Disable Register” on page 610, access changed to Write-only. ”Interrupt Mask Register” on page 611, access changed to Read-only.	1725
	UHP: Corrected signal name in block diagram Figure 37-1 on page 655 to UHPCK. Updated schematic Figure 37-4 ”Board Schematic to Interface UHP Device Controller” on page 659 and updated Section 37.5 ”Typical Connection” on page 659.	2924 3365 4203
	UDP: All sections and information on wake-up/remote wake-up updated. Section 38.6.10 ”UDP Endpoint Control and Status Register” on page 693, changes to Write and Read values in FORCESTALL bit . Section 38.6.2 ”UDP Global State Register” on page 681 activity of ESR and RMWUPE bits updated. Note added to TXVDIS bit description in Section 38.6.12 ”UDP Transceiver Control Register” on page 699 describing USB pullup effect on USB reset.	3048 3055
	ISI: Added information to CODEC_ON bit description in Section 37.5.1 “ISI Control 1 Register” on page 721. Added Bit 3 CDC_PND to Section 37.5.3 “ISI Status Register” on page 725. Correction to name of Section 37.5.8 “ISI Preview Decimation Factor Register” on page 732. Added note on ISI_PCK to Table 37-9, “Register Mapping,” on page 720. Updated ISI_RST bit description in Section 37.5.1 “ISI Control 1 Register” on page 721.	3518 3519 3520 3524
	ADC: Updated Figure 40-1, ”Analog-to-Digital Converter Block Diagram” on page 731.	3052
	Updated Table 41-1, “Absolute Maximum Ratings*,” on page 749 with new Maximum Operating Voltages.	3449
	Table 41-2, “DC Characteristics,” on page 749 updated with new information on RPULLUP and IO parameters.	3972
	Table 41-5, “Processor Clock Waveform Parameters,” on page 752: Removed values for processor clock frequency at T = 25°C.	3873
	Updated Table 41-9, “32 kHz Oscillator Characteristics,” on page 754 and added Note(2).	3384 + review
	In Table 41-12, “Main Oscillator Characteristics,” on page 755, changed and added information on capacitances. Added Note (6) and schematic in Note (7).	3863, 4026 + review
	Changed Figure 41-10, ”ISI Timing Diagram” on page 773 and timings in tables.	review
	In Table 41-33, “External Voltage Reference Input,” on page 776, updated ADVREF Input Voltage Range max.	3407
	Errata: Added Section 44.2.2 ”Boot ROM” on page 784 with errata on problem with RTT. Added Section 44.2.4 ”EMAC” on page 784 with errata on possible TX underrun.	3975 4114