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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	25MHz
Connectivity	SCI, SmartCard
Peripherals	DMA, POR, PWM, WDT
Number of I/O	106
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 12x10b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	144-BFQFP
Supplier Device Package	144-QFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2338vfc25v

Item	Page	Revision (See Manual for Details)
19.13.1 Features	789	Description amended • Reprogramming capability The flash memory can be reprogrammed min. 100 times.
22.2.6 Flash Memory Characteristics Table 22.21 Flash Memory Characteristics	910	Table 22.21 amended

Item		Symbol	Min	Typ	Max	Unit
Erase time*1*3*6		t_E	—	50	1000	ms/block
Reprogramming count		N_{WEC}	100*7	10000*8	—	Times
Data retention time*9		t_{DRP}	10	—	—	Years
Programming	Wait time after SWE bit x setting*1		1	—	—	µs

	911	Notes 7 to 9 added Notes: 7. Minimum number of times for which all characteristics are guaranteed after rewriting (Guarantee range is 1 to minimum value). 8. Reference value for 25°C (as a guideline, rewriting should normally function up to this value). 9. Data retention characteristic when rewriting is performed within the specification range, including the minimum value.
D.1 Port States in Each Mode Table D.1 I/O Port States in Each Processing State	1207	Note *1 deleted (Before) $\overline{\text{WDTOVF}}$*1 → (After) $\overline{\text{WDTOVF}}$
	1208	Note 1 shown below deleted Note: 1. The $\overline{\text{WDTOVF}}$ pin function cannot be used in the F-ZTAT version.

Table 8.3 DTC Functions

Transfer Mode	Activation Source	Address Registers	
		Transfer Source	Transfer Destination
• Normal mode — One transfer request transfers one byte or one word — Memory addresses are incremented or decremented by 1 or 2 — Up to 65,536 transfers possible • Repeat mode — One transfer request transfers one byte or one word — Memory addresses are incremented or decremented by 1 or 2 — After the specified number of transfers (1 to 256), the initial state resumes and operation continues • Block transfer mode — One transfer request transfers a block of the specified size — Block size is from 1 to 256 bytes or words — Up to 65,536 transfers possible — A block area can be designated at either the source or destination	• IRQ • TPU TGI • 8-bit timer CMI • SCI TXI or RXI • A/D converter ADI • DMAC DEND • Software	24 bits	24 bits

9.6.2 Register Configuration

Table 9.9 shows the port 5 register configuration.
Bits 7 to 4 of port 5 are input ports, and have no data direction register or data register.

Table 9.9 Port 5 Registers

Name	Abbreviation	R/W	Initial Value	Address*1
Port 5 data direction register	P5DDR	W	H'0*2	H'FEB4
Port 5 data register	P5DR	R/W	H'0*2	H'FF64
Port 5 register	PORT5	R	Undefined	H'FF54
Port function control register 2	PFCR2	R/W	H'30	H'FFAC
System control register	SYSCR	R/W	H'01	H'FF39

Notes: 1. Lower 16 bits of the address.
2. Value of bits 3 to 0.

Port 5 Data Direction Register (P5DDR)

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	—	P53DDR	P52DDR	P51DDR	P50DDR
Initial value	:	Undefined	Undefined	Undefined	Undefined	0	0	0	0
R/W	:	—	—	—	—	W	W	W	W

P5DDR is an 8-bit write-only register, the individual bits of which specify input or output for the pins of port 5. Bits 7 to 4 are reserved. P5DDR cannot be read; if it is, an undefined value will be read.

Setting a P5DDR bit to 1 makes the corresponding port 5 pin an output pin, while clearing the bit to 0 makes the pin an input pin.

P5DDR is initialized to H'0 (bits 3 to 0) by a reset, and in hardware standby mode. It retains its prior state in software standby mode. As the SCI is initialized, the pin states are determined by the P5DDR and P5DR specifications.

9.10.3 Pin Functions

Port 9 pins also function as interrupt input pins ($\overline{IRQ_2}$, $\overline{IRQ_3}$, $\overline{IRQ_4}$, $\overline{IRQ_5}$, $\overline{IRQ_6}$, and $\overline{IRQ_7}$). Port 9 pin functions are shown in table 9.18.

Table 9.18 Port 9 Pin Functions

Pin	Selection Method and Pin Functions
$P9_7/\overline{IRQ_7}$	The pin function is switched as shown below according to the combination of bits P97DDR and IRQPAS.

P97DDR	0	1
Pin function	$P9_7$ input pin	$P9_7$ output pin
	$\overline{IRQ_7}$ interrupt input pin*	

Note: * $\overline{IRQ_7}$ input when IRQPAS = 0.

$P9_6/\overline{IRQ_6}$	The pin function is switched as shown below according to the combination of bits P96DDR and IRQPAS.

P96DDR	0	1
Pin function	$P9_6$ input pin	$P9_6$ output pin
	$\overline{IRQ_6}$ interrupt input pin*	

Note: * $\overline{IRQ_6}$ input when IRQPAS = 0.

$P9_5/\overline{IRQ_5}$	The pin function is switched as shown below according to the combination of bits P95DDR and IRQPAS.

P95DDR	0	1
Pin function	$P9_5$ input pin	$P9_5$ output pin
	$\overline{IRQ_5}$ interrupt input pin*	

Note: * $\overline{IRQ_5}$ input when IRQPAS = 0.

$P9_4/\overline{IRQ_4}$	The pin function is switched as shown below according to the combination of bits P94DDR and IRQPAS.

P94DDR	0	1
Pin function	$P9_4$ input pin	$P9_4$ output pin
	$\overline{IRQ_4}$ interrupt input pin*	

Note: * $\overline{IRQ_4}$ input when IRQPAS = 0.

9.15.4 MOS Input Pull-Up Function

Port E has a built-in MOS input pull-up function that can be controlled by software. This MOS input pull-up function can be used in modes 4, 5, and 6 when 8-bit bus mode is selected, or in mode 7, and can be specified as on or off on an individual bit basis.

When a PEDDR bit is cleared to 0 in mode 4, 5, or 6 when 8-bit bus mode is selected, or in mode 7, setting the corresponding PEPCR bit to 1 turns on the MOS input pull-up for that pin.

The MOS input pull-up function is in the off state after a reset, and in hardware standby mode. The prior state is retained in software standby mode.

Table 9.29 summarizes the MOS input pull-up states.

Table 9.29 MOS Input Pull-Up States (Port E)

Modes		Reset	Hardware Standby Mode	Software Standby Mode	In Other Operations
7		Off	Off	On/off	On/off
4 to 6	8-bit bus				
	16-bit bus			Off	Off

Legend

Off: MOS input pull-up is always off.

On/off: On when PEDDR = 0 and PEPCR = 1; otherwise off.

Channel	Bit 3 IOC3	Bit 2 IOC2	Bit 1 IOC1	Bit 0 IOC0	Description		
3	0	0	0	0	TGR3C is output compare register*[1]	Output disabled	(Initial value)
				1		Initial output is 0 output	0 output at compare match
			1	0			1 output at compare match
				1			Toggle output at compare match
		1	0	0		Output disabled	
				1		Initial output is 1 output	0 output at compare match
			1	0			1 output at compare match
				1			Toggle output at compare match
	1	0	0	0	TGR3C is input capture register*[1]	Capture input source is TIOCC3 pin	Input capture at rising edge
				1			Input capture at falling edge
			1	*			Input capture at both edges
		1	*	*		Capture input source is channel 4/count clock	Input capture at TCNT4 count-up/count-down

*: Don't care

Note: 1. When the BFA bit in TMDR3 is set to 1 and TGR3C is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

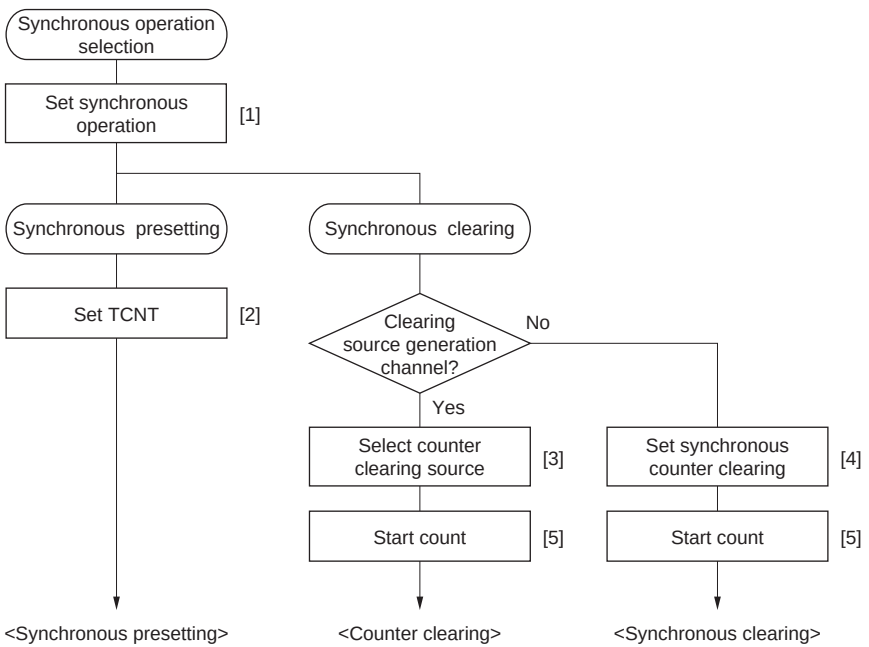
10.4.3 Synchronous Operation

In synchronous operation, the values in a number of TCNT counters can be rewritten simultaneously (synchronous presetting). Also, a number of TCNT counters can be cleared simultaneously by making the appropriate setting in TCR (synchronous clearing).

Synchronous operation enables TGR to be incremented with respect to a single time base.

Channels 0 to 5 can all be designated for synchronous operation.

Example of Synchronous Operation Setting Procedure: Figure 10.14 shows an example of the synchronous operation setting procedure.



[1] Set to 1 the SYNC bits in TSYR corresponding to the channels to be designated for synchronous operation.

[2] When the TCNT counter of any of the channels designated for synchronous operation is written to, the same value is simultaneously written to the other TCNT counters.

[3] Use bits CCLR2 to CCLR0 in TCR to specify TCNT clearing by input capture/output compare, etc.

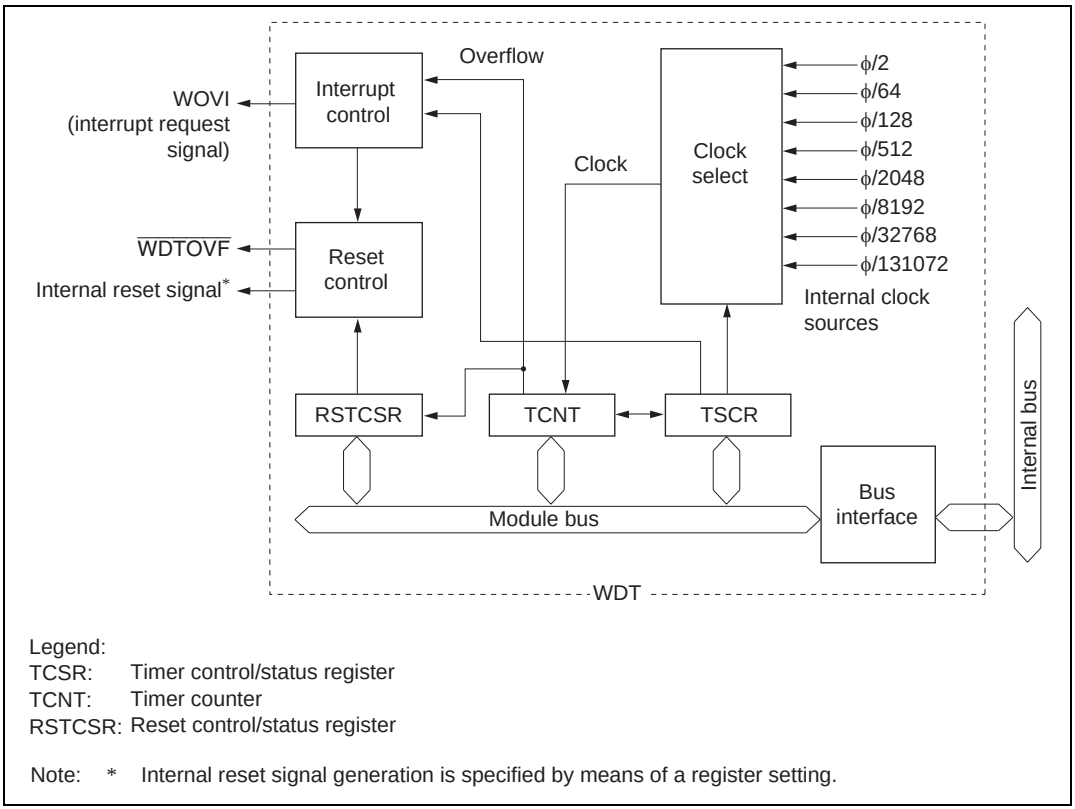
[4] Use bits CCLR2 to CCLR0 in TCR to designate synchronous clearing for the counter clearing source.

[5] Set to 1 the CST bits in TSTR for the relevant channels, to start the count operation.

Figure 10.14 Example of Synchronous Operation Setting Procedure

13.1.2 Block Diagram

Figure 13.1 shows a block diagram of the WDT.



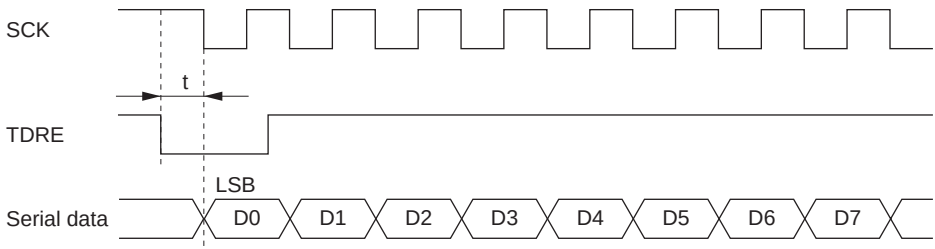
Legend:
TCSR: Timer control/status register
TCNT: Timer counter
RSTCSR: Reset control/status register

Note: * Internal reset signal generation is specified by means of a register setting.

Figure 13.1 Block Diagram of WDT

Restrictions on Use of DMAC or DTC

- When an external clock source is used as the serial clock, the transmit clock should not be input until at least 5 ϕ clock cycles after TDR is updated by the DMAC or DTC. Misoperation may occur if the transmit clock is input within 4 ϕ clocks after TDR is updated. (Figure 14.22)
- When RDR is read by the DMAC or DTC, be sure to set the activation source to the relevant SCI receive-data-full interrupt (RXI).



Note: When operating on an external clock, set t > 4 clocks.

Figure 14.22 Example of Synchronous Transmission Using DTC

Section 16 A/D Converter (12 Analog Input Channel Version)

16.1 Overview

The chip incorporates a successive-approximations type 10-bit A/D converter that allows up to twelve analog input channels to be selected.

16.1.1 Features

A/D converter features are listed below.

- 10-bit resolution
- Twelve input channels
- Settable analog conversion voltage range
  - — Conversion of analog voltages with the reference voltage pin (V_{ref}) as the analog reference voltage
- High-speed conversion
  - — Minimum conversion time: 6.7 µs per channel (at 20-MHz operation)
- Choice of single mode or scan mode
  - — Single mode: Single-channel A/D conversion
  - — Scan mode: Continuous A/D conversion on 1 to 4 channels
- Four data registers
  - — Conversion results are held in a 16-bit data register for each channel
- Sample and hold function
- Three kinds of conversion start
  - — Choice of software or timer conversion start trigger (TPU or 8-bit timer), or $\overline{\text{ADTRG}}$ pin
- A/D conversion end interrupt generation
  - — A/D conversion end interrupt (ADI) request can be generated at the end of A/D conversion
  - — The DMA controller (DMAC) or data transfer controller (DTC) can be activated for data transfer by an interrupt
- Module stop mode can be set
  - — As the initial setting, A/D converter operation is halted. Register access is enabled by exiting module stop mode.

19.13.9 Register Configuration

The registers used to control the on-chip flash memory when enabled are shown in table 19.27. In order to access the FLMCR1, FLMCR2, EBR1, and EBR2 registers, the FLSHE bit must be set to 1 in SYSCR2 (except RAMER).

Table 19.27 Flash Memory Registers

Register Name	Abbreviation	R/W	Initial Value	Address*1
Flash memory control register 1	FLMCR1*6	R/W*3	H'00/H'80*4	H'FFC8*2
Flash memory control register 2	FLMCR2*6	R/W*3	H'00	H'FFC9*2
Erase block register 1	EBR1*6	R/W*3	H'00*5	H'FFCA*2
Erase block register 2	EBR2*6	R/W*3	H'00*5	H'FFCB*2
System control register 2	SYSCR2*7	R/W	H'00	H'FF42
RAM emulation register	RAMER	R/W	H'00	H'FEDB

Notes: 1. Lower 16 bits of the address.
2. Flash memory. Registers selection is performed by the FLSHE bit in system control register 2 (SYSCR2).
3. In modes in which the on-chip flash memory is disabled, a read will return H'00, and writes are invalid. Writes are also disabled when the FWE bit is cleared to 0 in FLMCR1.
4. When a high level is input to the FWE pin, the initial value is H'80.
5. When a low level is input to the FWE pin, or if a high level is input and the SWE bit in FLMCR1 is not set, these registers are initialized to H'00.
6. FLMCR1, FLMCR2, EBR1, and EBR2 are 8-bit registers. Only byte accesses are valid for these registers, the access requiring 2 states.
7. The SYSCR2 register can only be used in the F-ZTAT version. In the mask ROM version this register will return an undefined value if read, and cannot be modified.

Table 19.28 Flash Memory Erase Blocks

Block (Size)	Address
EB0 (4 kbytes)	H'000000 to H'000FFF
EB1 (4 kbytes)	H'001000 to H'001FFF
EB2 (4 kbytes)	H'002000 to H'002FFF
EB3 (4 kbytes)	H'003000 to H'003FFF
EB4 (4 kbytes)	H'004000 to H'004FFF
EB5 (4 kbytes)	H'005000 to H'005FFF
EB6 (4 kbytes)	H'006000 to H'006FFF
EB7 (4 kbytes)	H'007000 to H'007FFF
EB8 (32 kbytes)	H'008000 to H'00FFFF
EB9 (64 kbytes)	H'010000 to H'01FFFF
EB10 (64 kbytes)	H'020000 to H'02FFFF
EB11 (64 kbytes)	H'030000 to H'03FFFF

19.14.5 System Control Register 2 (SYSCR2)

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	—	FLSHE	—	—	—
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	—	—	—	—	R/W	—	—	—

SYSCR2 is an 8-bit readable/writable register that performs on-chip flash memory control.

SYSCR2 is initialized to H'00 by a reset and in hardware standby mode.

SYSCR2 can only be used in the F-ZTAT versions. In the mask ROM versions this register will return an undefined value if read, and cannot be modified.

Bits 7 to 4—Reserved: These bits cannot be modified and are always read as 0.

Software standby mode is then cleared at the rising edge on the NMI pin.

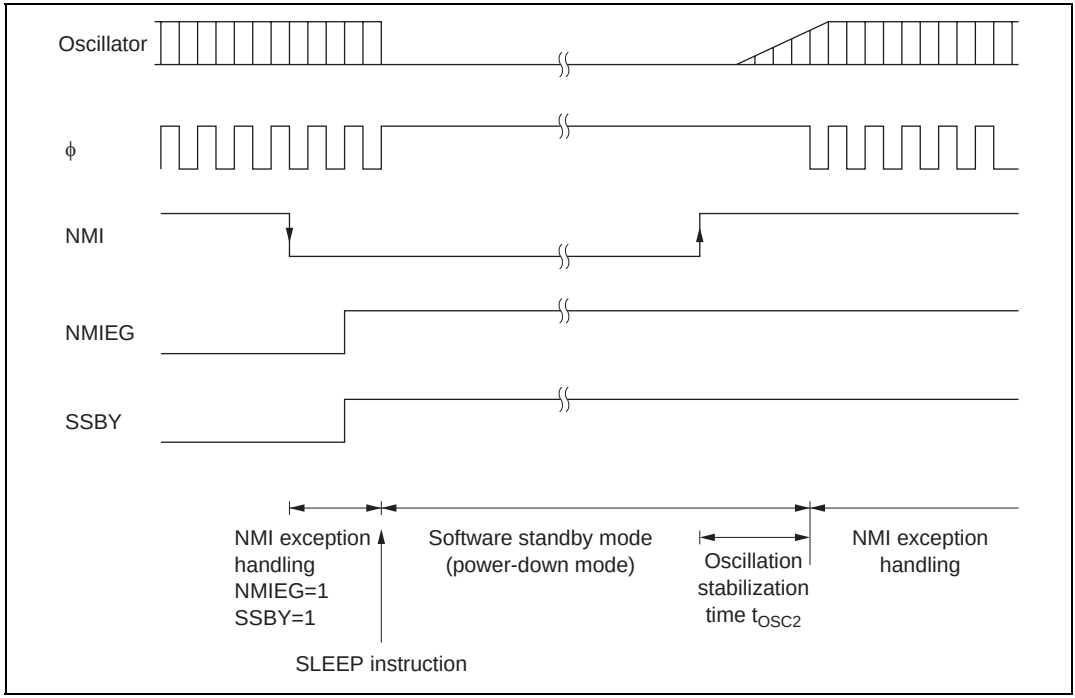


Figure 21.2 Software Standby Mode Application Example

21.6.5 Usage Notes

I/O Port Status: In software standby mode, I/O port states are retained. If the OPE bit is set to 1, the address bus and bus control signal output is also retained. Therefore, there is no reduction in current dissipation for the output current when a high-level signal is output.

Current Dissipation during Oscillation Stabilization Wait Period: Current dissipation increases during the oscillation stabilization wait period.

Write Data Buffer Function: The write data buffer function and software standby mode cannot be used at the same time. When the write data buffer function is used, the WDBE bit in BCRL should be cleared to 0 to cancel the write data buffer function before entering software standby mode. Also check that external writes have finished, by reading external addresses, etc., before executing a SLEEP instruction to enter software standby mode. See section 6.9, Write Data Buffer Function, for details of the write data buffer function.

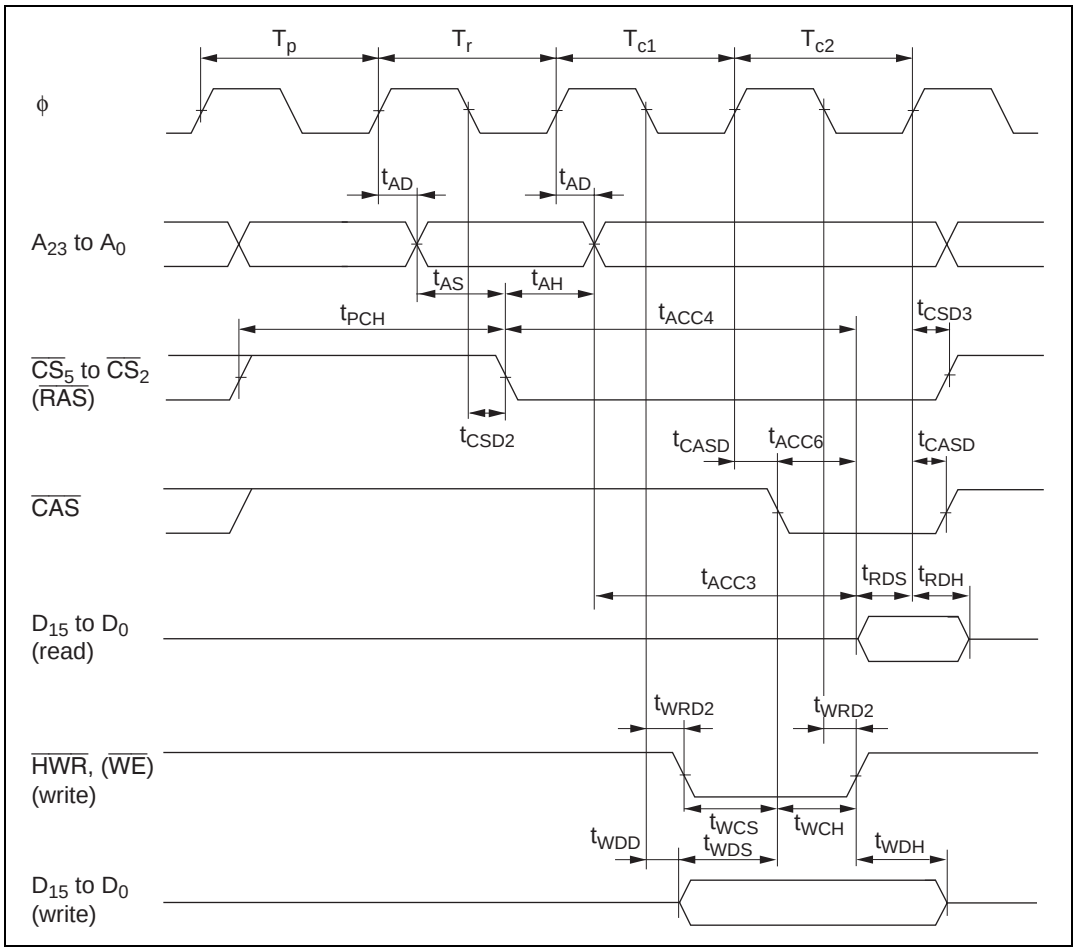


Figure 22.9 DRAM Bus Timing

Item			Symbol	Condition A Min	Condition A Max	Condition B Min	Condition B Max	Unit	Test Conditions
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	—	4	—	t_{cyc}	Figure 22.28
		Synchronous		6	—	6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	1.5	—	1.5	t_{cyc}	
	Input clock fall time		t_{SCKf}	—	1.5	—	1.5		
	Transmit data delay time		t_{TXD}	—	50	—	40	ns	Figure 22.29
	Receive data setup time (synchronous)		t_{RXS}	50	—	40	—	ns	
	Receive data hold time (synchronous)		t_{RXH}	50	—	40	—	ns	
A/D converter	Trigger input setup time		t_{TRGS}	30	—	30	—	ns	Figure 22.30

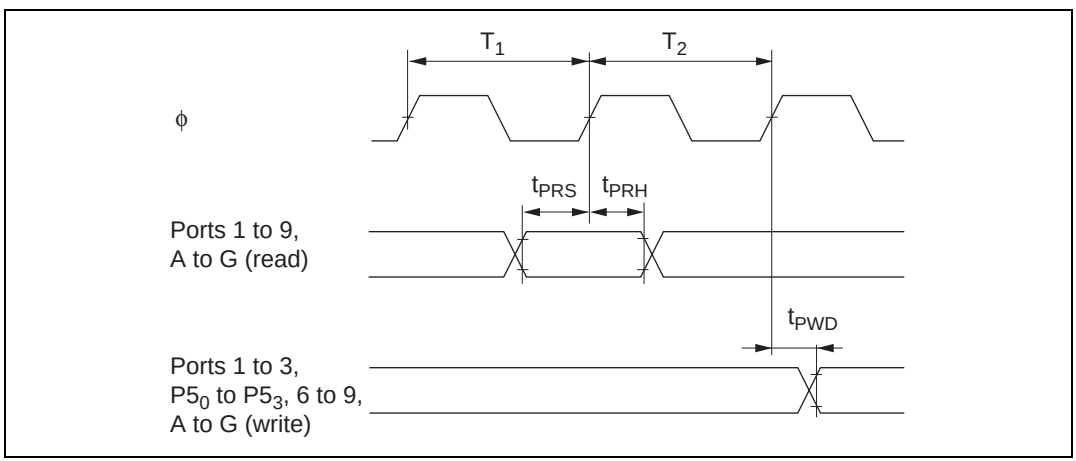


Figure 22.20 I/O Port Input/Output Timing

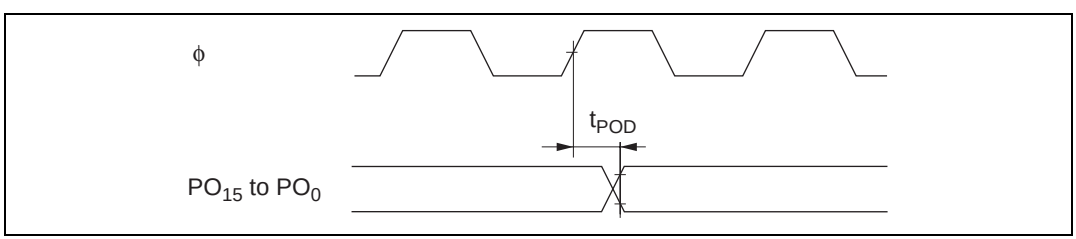


Figure 22.21 PPG Output Timing

22.1.5 D/A Conversion Characteristics

Table 22.10 D/A Conversion Characteristics

Condition A: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 2 MHz to 20 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 2 MHz to 25 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

	Condition A			Condition B				
Item	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Resolution	8	8	8	8	8	8	Bits	
Conversion time	—	—	10	—	—	10	µs	20 pF-capacitive load
Absolute accuracy	—	±2.0	±3.0	—	±2.0	±3.0	LSB	2 MΩ resistive load
	—	—	±2.0	—	—	±2.0	LSB	4 MΩ resistive load

Instruction	1	2	3	4	5	6	7	8	9
BCLR #xx:3,@aa:32	R:W 2nd	R:W 3rd	R:W 4th	R:B:M EA	R:W:M NEXT	W:B EA			
BCLR Rn,Rd	R:W NEXT								
BCLR Rn,@ERd	R:W 2nd	R:B:M EA	R:W:M NEXT	W:B EA					
BCLR Rn,@aa:8	R:W 2nd	R:B:M EA	R:W:M NEXT	W:B EA					
BCLR Rn,@aa:16	R:W 2nd	R:W 3rd	R:B:M EA	R:W:M NEXT	W:B EA				
BCLR Rn,@aa:32	R:W 2nd	R:W 3rd	R:W 4th	R:B:M EA	R:W:M NEXT	W:B EA			
BIAND #xx:3,Rd	R:W NEXT								
BIAND #xx:3,@ERd	R:W 2nd	R:B EA	R:W:M NEXT						
BIAND #xx:3,@aa:8	R:W 2nd	R:B EA	R:W:M NEXT						
BIAND #xx:3,@aa:16	R:W 2nd	R:W 3rd	R:B EA	R:W:M NEXT					
BIAND #xx:3,@aa:32	R:W 2nd	R:W 3rd	R:W 4th	R:B EA	R:W:M NEXT				
BILD #xx:3,Rd	R:W NEXT								
BILD #xx:3,@ERd	R:W 2nd	R:B EA	R:W:M NEXT						
BILD #xx:3,@aa:8	R:W 2nd	R:B EA	R:W:M NEXT						
BILD #xx:3,@aa:16	R:W 2nd	R:W 3rd	R:B EA	R:W:M NEXT					
BILD #xx:3,@aa:32	R:W 2nd	R:W 3rd	R:W 4th	R:B EA	R:W:M NEXT				
BIOR #xx:3,Rd	R:W NEXT								
BIOR #xx:3,@ERd	R:W 2nd	R:B EA	R:W:M NEXT						
BIOR #xx:3,@aa:8	R:W 2nd	R:B EA	R:W:M NEXT						
BIOR #xx:3,@aa:16	R:W 2nd	R:W 3rd	R:B EA	R:W:M NEXT					
BIOR #xx:3,@aa:32	R:W 2nd	R:W 3rd	R:W 4th	R:B EA	R:W:M NEXT				
BIST #xx:3,Rd	R:W NEXT								
BIST #xx:3,@ERd	R:W 2nd	R:B:M EA	R:W:M NEXT	W:B EA					
BIST #xx:3,@aa:8	R:W 2nd	R:B:M EA	R:W:M NEXT	W:B EA					
BIST #xx:3,@aa:16	R:W 2nd	R:W 3rd	R:B:M EA	R:W:M NEXT	W:B EA				
BIST #xx:3,@aa:32	R:W 2nd	R:W 3rd	R:W 4th	R:B:M EA	R:W:M NEXT	W:B EA			
BIXOR #xx:3,Rd	R:W NEXT								
BIXOR #xx:3,@ERd	R:W 2nd	R:B EA	R:W:M NEXT						
BIXOR #xx:3,@aa:8	R:W 2nd	R:B EA	R:W:M NEXT						
BIXOR #xx:3,@aa:16	R:W 2nd	R:W 3rd	R:B EA	R:W:M NEXT					
BIXOR #xx:3,@aa:32	R:W 2nd	R:W 3rd	R:W 4th	R:B EA	R:W:M NEXT				
BLD #xx:3,Rd	R:W NEXT								
BLD #xx:3,@ERd	R:W 2nd	R:B EA	R:W:M NEXT						
BLD #xx:3,@aa:8	R:W 2nd	R:B EA	R:W:M NEXT						
BLD #xx:3,@aa:16	R:W 2nd	R:W 3rd	R:B EA	R:W:M NEXT					
BLD #xx:3,@aa:32	R:W 2nd	R:W 3rd	R:W 4th	R:B EA	R:W:M NEXT				
BNOT #xx:3,Rd	R:W NEXT								

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Data Bus Width
H'FFC0	TSTR	—	—	CST5	CST4	CST3	CST2	CST1	CST0	TPU	16 bits
H'FFC1	TSYR	—	—	SYNC5	SYNC4	SYNC3	SYNC2	SYNC1	SYNC0		
H'FFC8*10	FLMCR1	FWE	SWE	ESU	PSU	EV	PV	E	P	Flash memory (H8S/2338 F-ZTAT)	8 bits
H'FFC9*10	FLMCR2	FLER	—	—	—	—	—	—	—		
H'FFCA*10	EBR1	EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0		
H'FFCB*10	EBR2	—	—	—	—	EB11	EB10	EB9	EB8		
H'FFC8*9	FLMCR1	FWE	SWE	ESU	PSU	EV	PV	E	P	Flash memory (H8S/2339 F-ZTAT)	8 bits
H'FFC9*9	FLMCR2	FLER	—	—	—	—	—	—	—		
H'FFCA*9	EBR1	EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0		
H'FFCB*9	EBR2	—	—	EB13	EB12	EB11	EB10	EB9	EB8		
H'FFD0	TCR0	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	TPU0	16 bits
H'FFD1	TMDR0	—	—	BFB	BFA	MD3	MD2	MD1	MD0		
H'FFD2	TIOR0H	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0		
H'FFD3	TIOR0L	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0		
H'FFD4	TIER0	TTGE	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA		
H'FFD5	TSR0	—	—	—	TCFV	TGFD	TGFC	TGFB	TGFA		
H'FFD6	TCNT0										
H'FFD7											
H'FFD8	TGR0A										
H'FFD9											
H'FFDA	TGR0B										
H'FFDB											
H'FFDC	TGR0C										
H'FFDD											
H'FFDE	TGR0D										
H'FFDF											
H'FFE0	TCR1	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	TPU1	16 bits
H'FFE1	TMDR1	—	—	—	—	MD3	MD2	MD1	MD0		
H'FFE2	TIOR1	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0		
H'FFE4	TIER1	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA		
H'FFE5	TSR1	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA		
H'FFE6	TCNT1										
H'FFE7											

TIER2—Timer Interrupt Enable Register 2 H'FFF4 TPU2

Bit	7	6	5	4	3	2	1	0
	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA
Initial value	0	1	0	0	0	0	0	0
Read/Write	R/W	—	R/W	R/W	—	—	R/W	R/W

TGR Interrupt Enable A

0	Interrupt request (TGIA) by TGFA bit disabled
1	Interrupt request (TGIA) by TGFA bit enabled

TGR Interrupt Enable B

0	Interrupt request (TGIB) by TGFB bit disabled
1	Interrupt request (TGIB) by TGFB bit enabled

Overflow Interrupt Enable

0	Interrupt request (TCIV) by TCFV disabled
1	Interrupt request (TCIV) by TCFV enabled

Underflow Interrupt Enable

0	Interrupt request (TCIU) by TCFU disabled
1	Interrupt request (TCIU) by TCFU enabled

A/D Conversion Start Request Enable

0	A/D conversion start request generation disabled
1	A/D conversion start request generation enabled

Appendix E Product Lineup

Table E.1 H8S/2339 Group Product Lineup

Product Type		Model	Marking	Package (Package Code)
H8S/2339	F-ZTAT version	HD64F2339	HD64F2339VFC	144-pin QFP (FP-144G)
		HD64F2339E*	HD64F2339EVFC	144-pin QFP (FP-144G)
H8S/2338	Mask ROM version	HD6432338	HD6432338FC	144-pin QFP (FP-144G)
	F-ZTAT version	HD64F2338	HD64F2338VFC	144-pin QFP (FP-144G)
H8S/2337	Mask ROM version	HD6432337	HD6432337FC	144-pin QFP (FP-144G)
H8S/2332	ROMless version	HD6412332	HD6412332VFC	144-pin QFP (FP-144G)

Note: * The on-chip debug function can be used with the E10-A emulator (E10-A compatible version). However, some function modules and pin functions are unavailable when the on-chip debug function is in use. Refer to figure 1.3.