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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2000
Core Size	16-Bit
Speed	25MHz
Connectivity	SCI, SmartCard
Peripherals	DMA, POR, PWM, WDT
Number of I/O	106
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 12x10b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	144-BFQFP
Supplier Device Package	144-QFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2339vfc25v

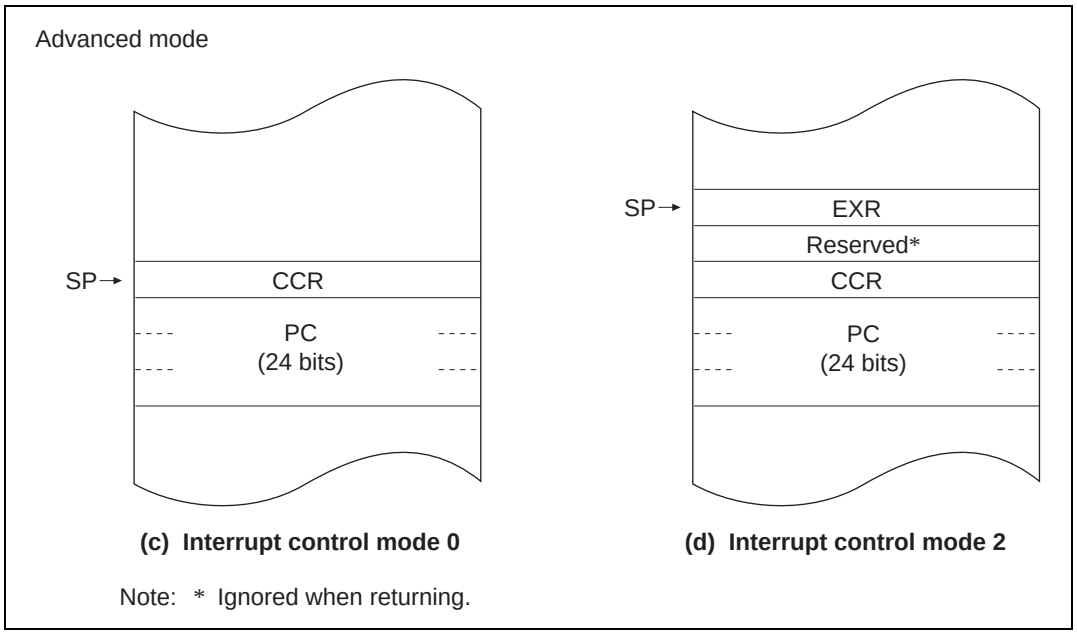


Figure 2.13 Stack Structure after Exception Handling (Examples)

2.8.4 Program Execution State

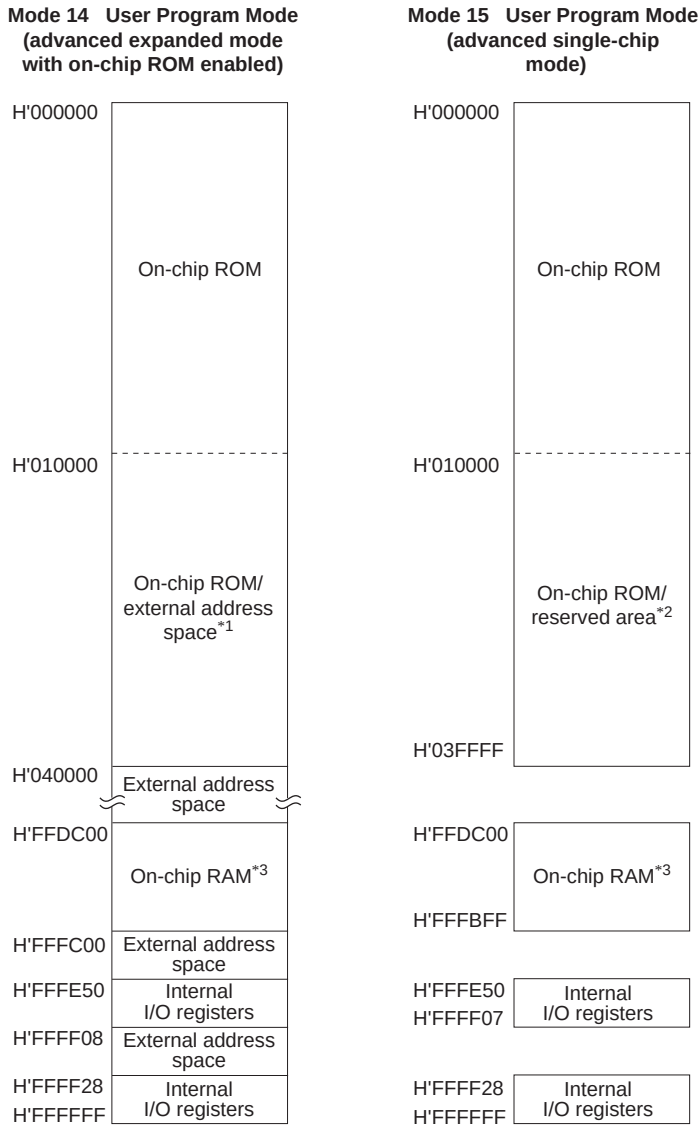
In this state the CPU executes program instructions in sequence.

2.8.5 Bus-Released State

This is a state in which the bus has been released in response to a bus request from a bus master other than the CPU. While the bus is released, the CPU halts.

There is one other bus master in addition to the CPU: the DMA controller (DMAC) and data transfer controller (DTC).

For further details, refer to section 6, Bus Controller.



Notes: 1. External addresses when EAE = 1 in BCRL; on-chip ROM when EAE = 0.
2. Reserved area when EAE = 1 in BCRL; on-chip ROM when EAE = 0.
3. On-chip RAM is used for flash memory programming. Do not clear the RAME bit in SYSCR to 0.

Figure 3.2 H8S/2338 Memory Map in Each Operating Mode (cont)
(F-ZTAT Version Only)

6.2.2 Access State Control Register (ASTCR)

Bit	:	7	6	5	4	3	2	1	0
		AST7	AST6	AST5	AST4	AST3	AST2	AST1	AST0
Initial value	:	1	1	1	1	1	1	1	1
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ASTCR is an 8-bit readable/writable register that designates each area as either 2-state access space or 3-state access space.

ASTCR sets the number of access states for the external memory space. The number of access states for on-chip memory and internal I/O registers is fixed regardless of the settings in ASTCR.

ASTCR is initialized to H'FF by a reset, and in hardware standby mode. It is not initialized in software standby mode.

Bits 7 to 0—Area 7 to 0 Access State Control (AST7 to AST0): These bits select whether the corresponding area is to be designated as 2-state access space or 3-state access space.

Wait state insertion is enabled or disabled at the same time.

Bit n ASTn	Description	
0	Area n is designated for 2-state access Wait state insertion in area n external space access is disabled	
1	Area n is designated for 3-state access Wait state insertion in area n external space access is enabled	(Initial value)

(n = 7 to 0)

6.2.3 Wait Control Registers H and L (WCRH, WCRL)

WCRH and WCRL are 8-bit readable/writable registers that select the number of program wait states for each area.

Program waits are not inserted in on-chip memory or internal I/O register access.

WCRH and WCRL are initialized to H'FF by a reset, and in hardware standby mode. They are not initialized in software standby mode.

7.3 Register Descriptions (2) (Full Address Mode)

Full address mode transfer is performed with channels A and B together. For details of full address mode setting, see table 7.4.

7.3.1 Memory Address Register (MAR)

Bit	:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		—	—	—	—	—	—	—	—								
Initial value	:	0	0	0	0	0	0	0	0	*	*	*	*	*	*	*	*
R/W	:	—	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	:	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

*: Undefined

MAR is a 32-bit readable/writable register; MARA functions as the transfer source address register, and MARB as the destination address register.

MAR is composed of two 16-bit registers, MARH and MARL. The upper 8 bits of MARH are reserved: they are always read as 0, and cannot be modified.

MAR is incremented or decremented each time a byte or word transfer is executed, so that the source or destination memory address can be updated automatically. For details, see section 7.3.4, DMA Control Register (DMACR).

MAR is not initialized by a reset or in standby mode.

7.3.2 I/O Address Register (IOAR)

IOAR is not used in full address transfer.

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	—	WE1B	WE1A	WE0B	WE0A
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	—	—	—	—	R/W	R/W	R/W	R/W

DMAWER is an 8-bit readable/writable register that controls enabling or disabling of writes to DMACR, DMABCR, and DMATCR by the DTC.

DMAWER is initialized to H'00 by a reset, and in hardware standby mode.

Bits 7 to 4—Reserved: Read-only bits, always read as 0.

Bit 3—Write Enable 1B (WE1B): Enables or disables writes to all bits in DMACR1B, bits 11, 7, and 3 in DMABCR, and bit 5 in DMATCR, by the DTC.

Bit 3 WE1B	Description
0	Writes to all bits in DMACR1B, bits 11, 7, and 3 in DMABCR, and bit 5 in DMATCR are disabled (Initial value)
1	Writes to all bits in DMACR1B, bits 11, 7, and 3 in DMABCR, and bit 5 in DMATCR are enabled

Bit 2—Write Enable 1A (WE1A): Enables or disables writes to all bits in DMACR1A, and bits 10, 6, and 2 in DMABCR, by the DTC.

Bit 2 WE1A	Description
0	Writes to all bits in DMACR1A, and bits 10, 6, and 2 in DMABCR are disabled (Initial value)
1	Writes to all bits in DMACR1A, and bits 10, 6, and 2 in DMABCR are enabled

Port Function Control Register 2 (PFCR2)

Bit	:	7	6	5	4	3	2	1	0
		WAITPS	BREQOPS	CS167E	CS25E	ASOD	—	—	—
Initial value	:	0	0	1	1	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R	R	R

PFCR2 is an 8-bit readable/writable register that performs I/O port control. PFCR2 is initialized to H'30 by a reset, and in hardware standby mode.

Bit 7—WAIT Pin Select (WAITPS): Selects the $\overline{\text{WAIT}}$ input pin. For details, see section 9.6, Port 5.

Bit 6—BREQO Pin Select (BREQOPS): Selects the $\overline{\text{BREQO}}$ output pin. For details, see section 9.6, Port 5.

Bit 5—CS167 Enable (CS167E): Enables or disables $\overline{\text{CS}}_1$, $\overline{\text{CS}}_6$, and $\overline{\text{CS}}_7$ output. Only change the CS167E bit setting when the DDR bits are cleared to 0.

Bit 5 CS167E	Description	
0	$\overline{\text{CS}}_1$, $\overline{\text{CS}}_6$, and $\overline{\text{CS}}_7$ output disabled (can be used as I/O ports)	
1	$\overline{\text{CS}}_1$, $\overline{\text{CS}}_6$, and $\overline{\text{CS}}_7$ output enabled	(Initial value)

Bit 4—CS25 Enable (CS25E): Enables or disables $\overline{\text{CS}}_2$, $\overline{\text{CS}}_3$, $\overline{\text{CS}}_4$, and $\overline{\text{CS}}_5$ output. Only change the CS25E bit setting when the DDR bits are cleared to 0.

Bit 4 CS25E	Description	
0	$\overline{\text{CS}}_2$, $\overline{\text{CS}}_3$, $\overline{\text{CS}}_4$, and $\overline{\text{CS}}_5$ output disabled (can be used as I/O ports)	
1	$\overline{\text{CS}}_2$, $\overline{\text{CS}}_3$, $\overline{\text{CS}}_4$, and $\overline{\text{CS}}_5$ output enabled	(Initial value)

Bit 3—AS Output Disable (ASOD): Enables or disables $\overline{\text{AS}}$ output. For details, see section 9.16, Port F.

Bits 2 to 0—Reserved: These bits are always read as 0.

9.10 Port 9

9.10.1 Overview

Port 9 is a 6-bit I/O port. Port 9 pins also function as interrupt input pins ($\overline{IRQ_2}$, $\overline{IRQ_3}$, $\overline{IRQ_4}$, $\overline{IRQ_5}$, $\overline{IRQ_6}$, and $\overline{IRQ_7}$). When the IRQPAS bit is set to 1, inputs $\overline{IRQ_4}$ to $\overline{IRQ_7}$ are switched to $P5_0$ to $P5_3$. Port 9 pin functions are the same in all operating modes. Port 9 uses Schmitt-triggered input. Figure 9.9 shows the port 9 pin configuration.

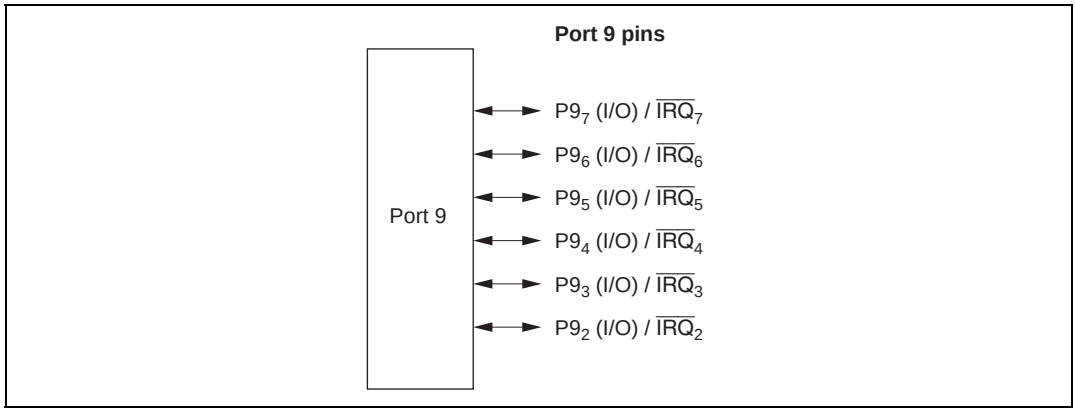


Figure 9.9 Port 9 Pin Functions

Mode 6: In mode 6, port B pins function as address outputs or input ports. Input or output can be specified on an individual bit basis. Setting a PBDDR bit to 1 makes the corresponding port B pin an address output, while clearing the bit to 0 makes the pin an input port.

Port B pin functions in mode 6 are shown in figure 9.13

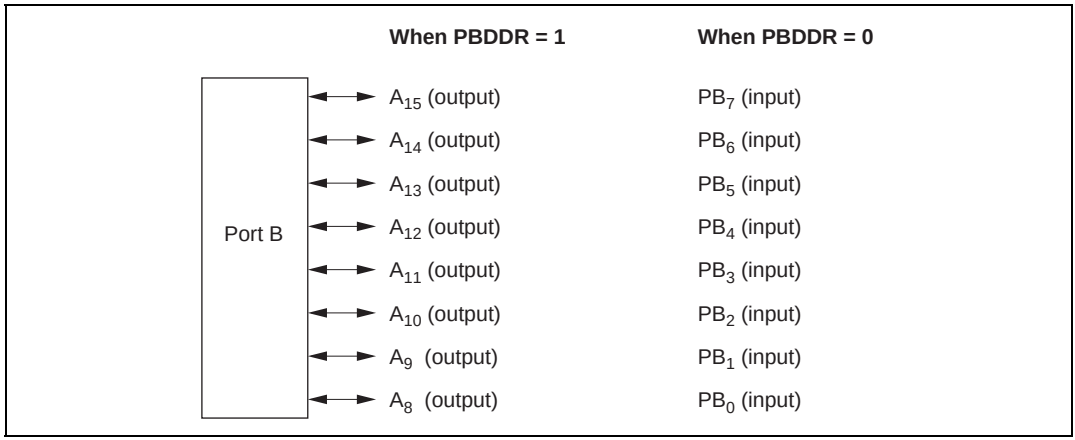


Figure 9.13 Port B Pin Functions (Mode 6)

Mode 7: In mode 7, port B pins function as I/O ports. Input or output can be specified for each pin on an individual bit basis. Setting a PBDDR bit to 1 makes the corresponding port B pin an output port, while clearing the bit to 0 makes the pin an input port.

Port B pin functions in mode 7 are shown in figure 9.14.

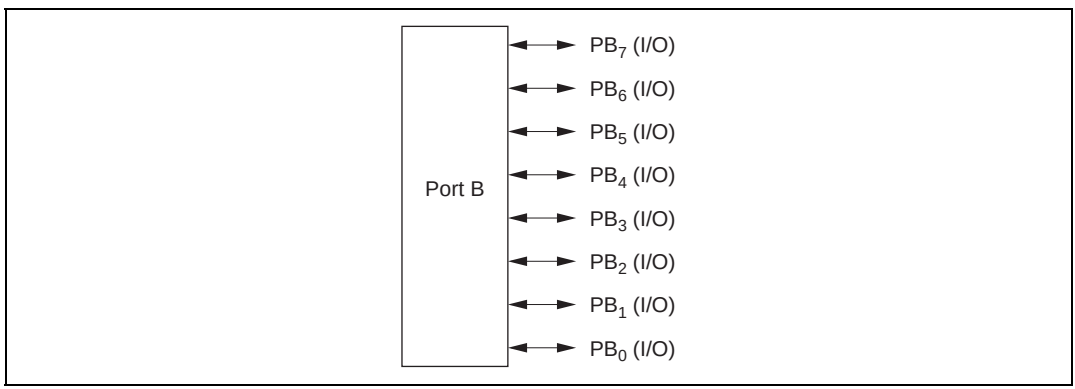


Figure 9.14 Port B Pin Functions (Mode 7)

Mode 7: In mode 7, port D pins function as I/O ports. Input or output can be specified for each pin on an individual bit basis. Setting a PDDDR bit to 1 makes the corresponding port D pin an output port, while clearing the bit to 0 makes the pin an input port.

Port D pin functions in mode 7 are shown in figure 9.21.

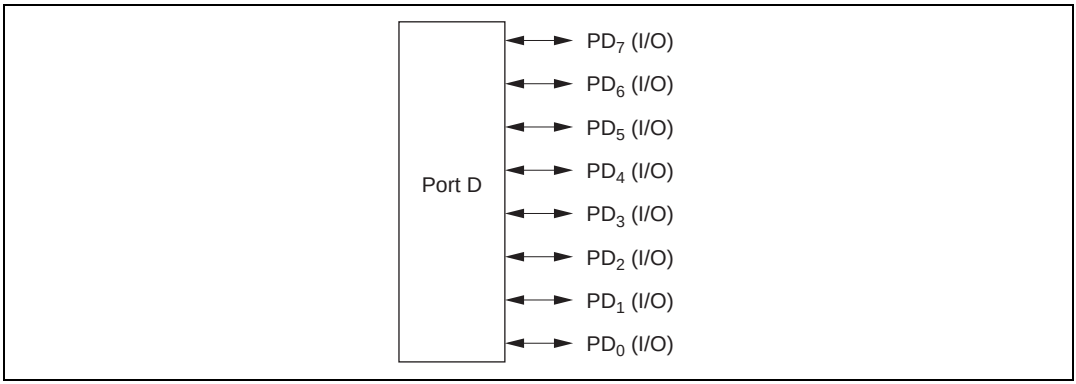


Figure 9.21 Port D Pin Functions (Mode 7)

Channel	Bit 3 IOC3	Bit 2 IOC2	Bit 1 IOC1	Bit 0 IOC0	Description		
0	0	0	0	0	TGR0C is output compare register*[1]	Output disabled	(Initial value)
				1		Initial output is 0 output	0 output at compare match
			1	0			1 output at compare match
				1			Toggle output at compare match
		1	0	0		Output disabled	
				1		Initial output is 1 output	0 output at compare match
			1	0			1 output at compare match
				1			Toggle output at compare match
	1	0	0	0	TGR0C is input capture register*[1]	Capture input source is TIOCC0 pin	Input capture at rising edge
				1			Input capture at falling edge
			1	*			Input capture at both edges
		1	*	*		Capture input source is channel 1/count clock	Input capture at TCNT1 count-up/count-down

*: Don't care

Note: 1. When the BFA bit in TMDR0 is set to 1 and TGR0C is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

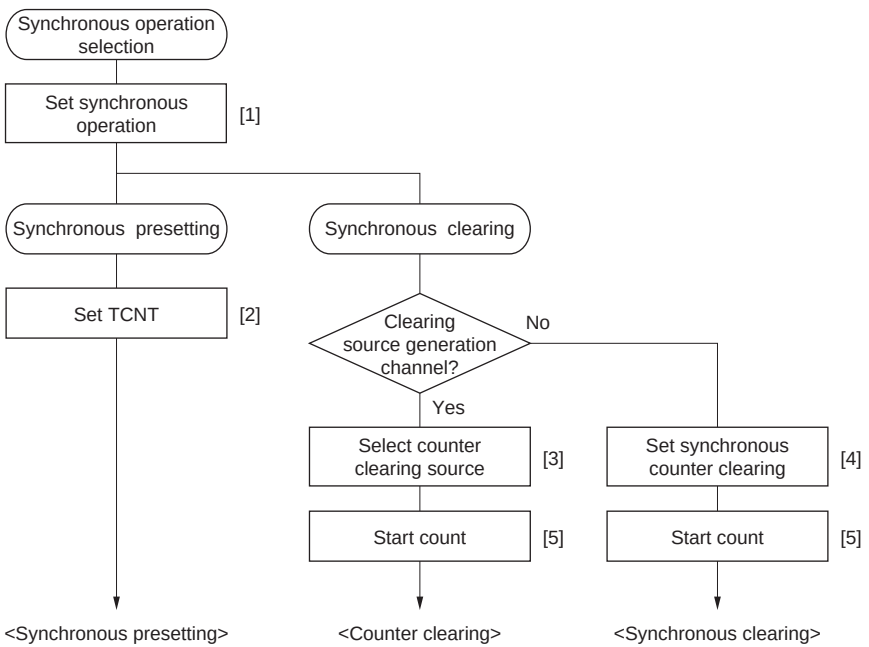
10.4.3 Synchronous Operation

In synchronous operation, the values in a number of TCNT counters can be rewritten simultaneously (synchronous presetting). Also, a number of TCNT counters can be cleared simultaneously by making the appropriate setting in TCR (synchronous clearing).

Synchronous operation enables TGR to be incremented with respect to a single time base.

Channels 0 to 5 can all be designated for synchronous operation.

Example of Synchronous Operation Setting Procedure: Figure 10.14 shows an example of the synchronous operation setting procedure.



[1] Set to 1 the SYNC bits in TSYR corresponding to the channels to be designated for synchronous operation.

[2] When the TCNT counter of any of the channels designated for synchronous operation is written to, the same value is simultaneously written to the other TCNT counters.

[3] Use bits CCLR2 to CCLR0 in TCR to specify TCNT clearing by input capture/output compare, etc.

[4] Use bits CCLR2 to CCLR0 in TCR to designate synchronous clearing for the counter clearing source.

[5] Set to 1 the CST bits in TSTR for the relevant channels, to start the count operation.

Figure 10.14 Example of Synchronous Operation Setting Procedure

Bit 6—Block Transfer Mode (BLK): Selects block transfer mode.

Bit 6 BLK	Description
0	Normal smart card interface mode operation (Initial value) • Error signal transmission/detection and automatic data retransmission performed • TXI interrupt generated by TEND flag • TEND flag set 12.5 etu after start of transmission (11.0 etu in GSM mode)
1	Block transfer mode operation • Error signal transmission/detection and automatic data retransmission not performed • TXI interrupt generated by TDRE flag • TEND flag set 11.5 etu after start of transmission (11.0 etu in GSM mode)

Note: etu: Elementary time unit (time for transfer of 1 bit)

Bits 3 and 2—Base Clock Pulse 1 and 2 (BCP1, BCP0): These bits specify the number of base clock periods in a 1-bit transfer interval on the smart card interface.

Bit 3 BCP1	Bit 2 BCP0	Description
0	0	32 clock periods (Initial value)
	1	64 clock periods
1	0	372 clock periods
	1	256 clock periods

Bits 5, 4, 1, and 0—Operate in the same way as for the normal SCI. For details, see section 14.2.5, Serial Mode Register (SMR).

19.6 On-Board Programming Modes

When pins are set to on-board programming mode, program/erase/verify operations can be performed on the on-chip flash memory. There are two on-board programming modes: boot mode and user program mode. The pin settings for transition to each of these modes are shown in table 19.9. For a diagram of the transitions to the various flash memory modes, see figure 19.3.

Table 19.9 Setting On-Board Programming Modes

Mode		Pins		
MCU Mode	**CPU Operating Mode**	**MD2**	**MD1**	**MD0**
Boot mode	Advanced expanded mode with on-chip ROM enabled	0	1	0
	Advanced single-chip mode			1
User program mode*	Advanced expanded mode with on-chip ROM enabled	1	1	0
	Advanced single-chip mode			1

Note: * Normally, user mode should be used. Set the SWE bit to 1 to make a transition to user program mode before performing a program/erase/verify operation.

19.20.3 PROM Mode Operation

Table 19.35 shows how the different operating modes are set when using PROM mode, and table 19.36 lists the commands used in PROM mode. Details of each mode are given below.

Memory Read Mode: Memory read mode supports byte reads.

Auto-Program Mode: Auto-program mode supports programming of 128 bytes at a time. Status polling is used to confirm the end of auto-programming.

Auto-Erase Mode: Auto-erase mode supports automatic erasing of the entire flash memory. Status polling is used to confirm the end of auto-erasing.

Status Read Mode: Status polling is used for auto-programming and auto-erasing, and normal termination can be confirmed by reading the I/O_6 signal. In status read mode, error information is output if an error occurs.

Table 19.35 Settings for Each Operating Mode in PROM Mode

	Pin Names					
Mode	**FWE**	**$\overline{CE}$**	**$\overline{OE}$**	**$\overline{WE}$**	**I/O_7 to I/O_0**	**A_{18} to A_0**
Read	H or L	L	L	H	Data output	Ain
Output disable	H or L	L	H	H	Hi-Z	X
Command write	H or L*3	L	H	L	Data input	Ain*2
Chip disable*1	H or L	H	X	X	Hi-Z	X

Legend:

H: High level

L: Low level

Hi-Z: High impedance

X: Don't care

Notes: 1. Chip disable is not a standby state; internally, it is an operation state.

2. Ain indicates that there is also address input in auto-program mode.

3. For command writes when making a transition to auto-program or auto-erase mode, input a high level to the FWE pin.

21.7 Hardware Standby Mode

21.7.1 Hardware Standby Mode

When the $\overline{\text{STBY}}$ pin is driven low, a transition is made to hardware standby mode from any mode.

In hardware standby mode, all functions enter the reset state and stop operation, resulting in a significant reduction in power dissipation. As long as the prescribed voltage is supplied, on-chip RAM data is retained. I/O ports are set to the high-impedance state.

In order to retain on-chip RAM data, the RAME bit in SYSCR should be cleared to 0 before driving the $\overline{\text{STBY}}$ pin low.

Do not change the state of the mode pins (MD2 to MD0) while the chip is in hardware standby mode.

Hardware standby mode is cleared by means of the $\overline{\text{STBY}}$ pin and the $\overline{\text{RES}}$ pin. When the $\overline{\text{STBY}}$ pin is driven high while the $\overline{\text{RES}}$ pin is low, the reset state is set and clock oscillation is started. Ensure that the $\overline{\text{RES}}$ pin is held low until the clock oscillator stabilizes (at least 8 ms—the oscillation stabilization time—when using a crystal oscillator). When the $\overline{\text{RES}}$ pin is subsequently driven high, a transition is made to the program execution state via the reset exception handling state.

21.7.2 Hardware Standby Mode Timing

Figure 21.3 shows an example of hardware standby mode timing.

When the $\overline{\text{STBY}}$ pin is driven low after the $\overline{\text{RES}}$ pin has been driven low, a transition is made to hardware standby mode. Hardware standby mode is cleared by driving the $\overline{\text{STBY}}$ pin high, waiting for the oscillation stabilization time, then changing the $\overline{\text{RES}}$ pin from low to high.

A.6 Condition Code Modification

This section indicates the effect of each CPU instruction on the condition code. The notation used in the table is defined below.

m = { 31 for longword operands / 15 for word operands / 7 for byte operands

Si	The i-th bit of the source operand
Di	The i-th bit of the destination operand
Ri	The i-th bit of the result
Dn	The specified bit in the destination operand
—	Not affected
↕	Modified according to the result of the instruction (see definition)
0	Always cleared to 0
1	Always set to 1
*	Undetermined (no guaranteed value)
Z'	Z flag before instruction execution
C'	C flag before instruction execution

Module	Register	Abbreviation	R/W	Initial Value	Address[*1]
WDT	Timer control/status register	TCSR	R/(W)[*10]	H'18	H'FFBC: Write[*9] H'FFBC: Read
	Timer counter	TCNT	R/W	H'00	H'FFBC: Write[*9] H'FFBD: Read
	Reset control/status register	RSTCSR	R/(W)[*10]	H'1F	H'FFBE: Write[*9] H'FFBF: Read
SCI0	Serial mode register 0	SMR0	R/W	H'00	H'FF78
	Bit rate register 0	BRR0	R/W	H'FF	H'FF79
	Serial control register 0	SCR0	R/W	H'00	H'FF7A
	Transmit data register 0	TDR0	R/W	H'FF	H'FF7B
	Serial status register 0	SSR0	R/(W)[*2]	H'84	H'FF7C
	Receive data register 0	RDR0	R	H'00	H'FF7D
	Smart card mode register 0	SCMR0	R/W	H'F2	H'FF7E
SCI1	Serial mode register 1	SMR1	R/W	H'00	H'FF80
	Bit rate register 1	BRR1	R/W	H'FF	H'FF81
	Serial control register 1	SCR1	R/W	H'00	H'FF82
	Transmit data register 1	TDR1	R/W	H'FF	H'FF83
	Serial status register 1	SSR1	R/(W)[*2]	H'84	H'FF84
	Receive data register 1	RDR1	R	H'00	H'FF85
	Smart card mode register 1	SCMR1	R/W	H'F2	H'FF86
SCI2	Serial mode register 2	SMR2	R/W	H'00	H'FF88
	Bit rate register 2	BRR2	R/W	H'FF	H'FF89
	Serial control register 2	SCR2	R/W	H'00	H'FF8A
	Transmit data register 2	TDR2	R/W	H'FF	H'FF8B
	Serial status register 2	SSR2	R/(W)[*2]	H'84	H'FF8C
	Receive data register 2	RDR2	R	H'00	H'FF8D
	Smart card mode register 2	SCMR2	R/W	H'F2	H'FF8E
All SCI channels	Module stop control register	MSTPCR	R/W	H'3FFF	H'FF3C

ADDRAH—A/D Data Register AH	**H'FF90**	**A/D Converter**
ADDRAL—A/D Data Register AL	**H'FF91**	**A/D Converter**
ADDRBH—A/D Data Register BH	**H'FF92**	**A/D Converter**
ADDRBL—A/D Data Register BL	**H'FF93**	**A/D Converter**
ADDRCH—A/D Data Register CH	**H'FF94**	**A/D Converter**
ADDRCL—A/D Data Register CL	**H'FF95**	**A/D Converter**
ADDRDH—A/D Data Register DH	**H'FF96**	**A/D Converter**
ADDRDL—A/D Data Register DL	**H'FF97**	**A/D Converter**

Bit	:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	—	—	—	—	—	—
Initial value	:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read/Write	:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Stores the results of A/D conversion

Analog Input Channel				A/D Data Register
Channel Set 0 (CH3 = 1)		Channel Set 1 (CH3 = 0)		
Group 0	Group 1	Group 0	Group 1	
AN0	AN4	Setting prohibited	AN12	ADDRA
AN1	AN5	Setting prohibited	AN13	ADDRB
AN2	AN6	Setting prohibited	AN14	ADDRC
AN3	AN7	Setting prohibited	AN15	ADDRD

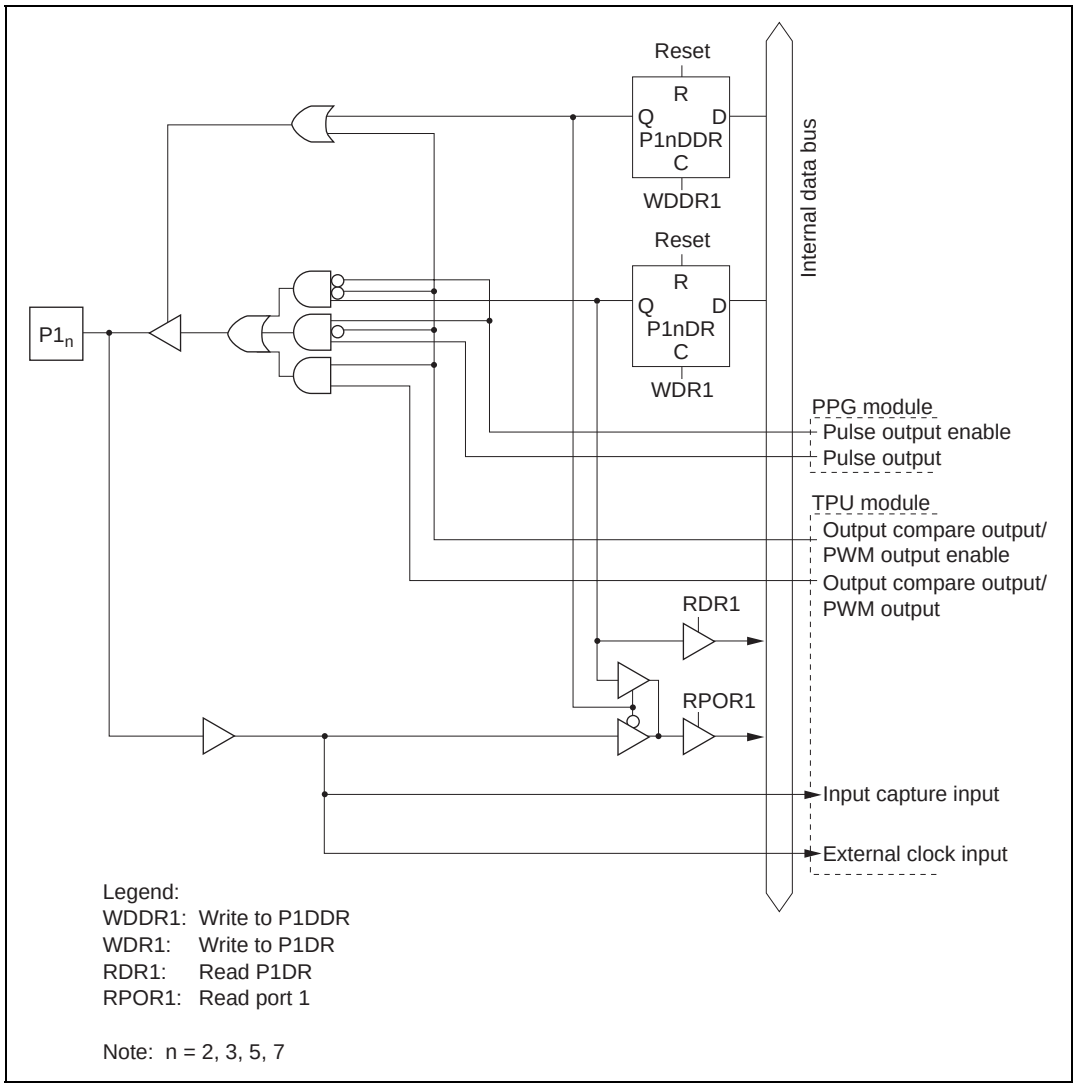


Figure C.1 (b) Port 1 Block Diagram (Pins $P1_2$, $P1_3$, $P1_5$, and $P1_7$)