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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | ST10 |
| Core Size | 16-Bit |
| Speed | 50MHz |
| Connectivity | EBI/EMI, SSP, UART/USART |
| Peripherals | POR, PWM, WDT |
| Number of I/O | 77 |
| Program Memory Size | - |
| Program Memory Type | ROMless |
| EEPROM Size | - |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-TQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/st10r272lt1-tr |

# Table of Contents

| Symbol | Pin Number (TQFP) | Input (I) Output (O) | Kind[1)] | Function |
|---|---|---|---|---|
| ALE | 36 | O | 5T | Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes. |
| $\overline{EA}$ | 37 | I | 5T | External Access Enable pin. Low level at this pin during and after reset forces the ST10R272L to begin instruction execution out of external memory. A high level forces execution out of the internal ROM. The ST10R272L must have this pin tied to '0'. |
| PORT0:<br>P0L.0– P0L.7,<br>P0H.0 - P0H.7 | <br>41 - 48<br>51 - 58 | I/O | 5T | PORT0 has two 8-bit bidirectional I/O ports P0L and P0H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state.<br>For external bus configuration, PORT0 acts as address (A) and address/data (AD) bus in multiplexed bus modes and as the data (D) bus in demultiplexed bus modes.<br>**Demultiplexed bus modes**<br>Data Path Width: 8-bit 16-bit<br>P0L.0 – P0L.7: D0 – D7 D0 - D7<br>P0H.0 – P0H.7: I/O D8 - D15<br>**Multiplexed bus modes**<br>Data Path Width: 8-bit 16-bit<br>P0L.0 – P0L.7: AD0 – AD7 AD0 - AD7<br>P0H.0 – P0H.7: A8 – A15 AD8 – AD15 |
| PORT1:<br>P1L.0– P1L.7,<br>P1H.0 - P1H.7 | <br>59- 66<br>67, 68 71-76 | I/O | 5T | PORT1 has two 8-bit bidirectional I/O ports P1L and P1H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. PORT1 acts as a 16-bit address bus (A) in demultiplexed bus modes and also after switching from a demultiplexed bus mode to a multiplexed bus mode. |

**Table 1 Pin definitions**

The Parallel Data Move shifts a table of operands in parallel with a computation on those operands. Its specific use is for signal processing algorithms like filter computation. The following figure gives an example of Parallel Data Move with CoMACM instruction.

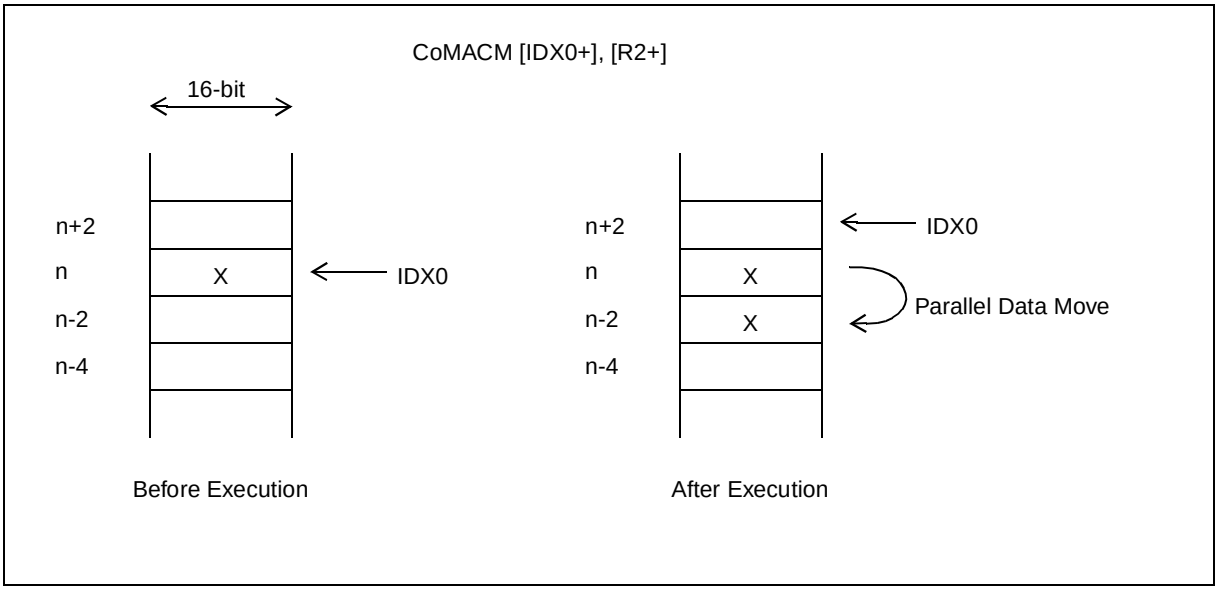


**Figure 6 Example of parallel data move**

## 16 x 16 signed/unsigned parallel multiplier

The multiplier executes 16 x 16-bit parallel signed/unsigned fractional and integer multiplies. The multiplier has two 16-bit input ports, and a 32-bit product output port. The input ports can accept data from the MA-bus and from the MB-bus. The output is sign-extended and then feeds a scaler that shifts the multiplier output according to the shift mode bit MP specified in the co-processor Control Word (MCW). The product can be shifted one bit left to compensate for the extra sign bit gained in multiplying two 16-bit signed (2's complement) fractional numbers if bit MP is set.

## 40-bit signed arithmetic unit

The arithmetic unit over 32 bits wide to allow intermediate overflow in a series of multiply/ accumulate operations. The extension flag E, contained in the most significant byte of MSW, is set when the Accumulator has overflowed beyond the 32-bit boundary, that is, when there are significant (non-sign) bits in the top eight (signed arithmetic) bits of the Accumulator.

The 40-bit arithmetic unit has two 40-bit input ports A and B. The A-input port accepts data from 4 possible sources: 00,0000,0000h, 00,0000,8000h (round), the sign-extended product, or the sign-extended data conveyed by the 32-bit bus resulting from the concatenation of MA- and MB-buses. Product and Concatenation can be shifted left by one according to MP for the multiplier or to the instruction for the concatenation. The B-input port is fed either by the 40-bit shifted/not shifted and inverted/not inverted accumulator or by 00,0000,0000h. A-input and B-

input ports can receive 00,0000,0000h to allow direct transfers from the B-source and A-source, respectively, to the Accumulator (case of Multiplication, Shift.). The output of the arithmetic unit goes to the Accumulator.

It is also possible to saturate the Accumulator on a 32-bit value, automatically after every accumulation. Automatic saturation is enabled by setting the saturation bit MS in the MCW register. When the Accumulator is in the saturation mode and an 32-bit overflow occurs, the accumulator is loaded with either the most positive or the most negative value representable in a 32-bit value, depending on the direction of the overflow. The value of the Accumulator upon saturation is 00,7fff,ffffh (positive) or ff,8000,0000h (negative) in signed arithmetic. Automatic saturation sets the SL flag MSW. This flag is a sticky flag which means it stays set until it is explicitly reset by the user.

40-bit overflow of the Accumulator sets the SV flag in MSW. This flag is also a sticky flag.

## 40-bit accumulator register

The 40-bit Accumulator consists of three SFR registers MAH, MAL and MAE. MAH and MAL are 16-bit wide. MAE is 8-bit wide and is contained within the least significant byte of MSW. Most co-processor operations specify the 40-bit Accumulator register as source and/or destination operand.

## Data limiter

Saturation arithmetic is also provided to selectively limit overflow, when reading the accumulator by means of a CoSTORE <destination> MAS instruction. Limiting is performed on the MAC Accumulator. If the contents of the Accumulator can be represented in the destination operand size without overflow, the data limiter is disabled and the operand is not modified. If the contents of the accumulator cannot be represented without overflow in the destination operand size, the limiter will substitute a ‘limited’ data as explained in the following table.

| Register | E bit | N bit | Output of the Limiter |
|---|---|---|---|
| x | 0 | x | unchanged |
| MAS | 1 | 0 | 7fffh |
| MAS | 1 | 1 | 8000h |

**Table 4 Data Limit Values**

*Note* *In this case, the accumulator and the status register are not affected. MAS readable from a CoSTORE instruction.*

## 6.2 Hardware Traps

Exceptions or error conditions that arise during run-time are called Hardware Traps. Hardware traps cause immediate non-maskable system reaction similar to a standard interrupt service (branching to a dedicated vector table location). The occurrence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except when another higher prioritized trap service is in progress, a hardware trap will interrupt any actual program execution. In turn, hardware trap services can not normally be interrupted by standard or PEC interrupts. The following table shows all of the possible exceptions or error conditions that can arise during run-time:

| Exception Condition | Trap Flag | Trap Vector | Vector Location | Trap Number | Trap Priority |
|---|---|---|---|---|---|
| Reset Functions: | | | | | |
| Hardware Reset | | RESET | 00'0000h | 00h | III |
| Software Reset | | RESET | 00'0000h | 00h | III |
| Watchdog Timer Overflow | | RESET | 00'0000h | 00h | III |
| Class A Hardware Traps: | | | | | |
| Non-Maskable Interrupt | NMI | NMITRAP | 00'0008h | 02h | II |
| Stack Overflow | STKOF | STOTRAP | 00'0010h | 04h | II |
| Stack Underflow | STKUF | STUTRAP | 00'0018h | 06h | II |
| Class B Hardware Traps: | | | | | |
| Undefined opcode | UNDOPC | BTRAP | 00'0028h | 0Ah | I |
| Protected instruction fault | PRTFLT | BTRAP | 00'0028h | 0Ah | I |
| Illegal word operand access | ILLOPA | BTRAP | 00'0028h | 0Ah | I |
| Illegal instruction access | ILLINA | BTRAP | 00'0028h | 0Ah | I |
| Illegal external bus access | ILLBUS | BTRAP | 00'0028h | 0Ah | I |
| MAC trap | MACTRP | BTRAP | 00'0028h | 0Ah | I |
| Reserved | | | [2Ch – 3Ch] | [0Bh – 0Fh] | |
| Software Traps | | | | | |
| TRAP Instruction | | | Any [00'0000h – 00'01FCh] steps of 4h | Any [00h – 7Fh] | Current CPU Priority |

**Table 6 Exceptions or error conditions**

# 10 GENERAL PURPOSE TIMERS

The GPTs are flexible multifunctional timer/counters used for time-related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation or pulse multiplication. The GPT unit contains five 16-bit timers, organized in two separate modules, GPT1 and GPT2. Each timer in each module may operate independently in a number of different modes, or may be concatenated with another timer of the same module.

## 10.1 GPT1

Each of the three timers T2, T3, T4 of the GPT1 module can be configured individually for one of four basic modes of operation: **timer**, **gated timer**, **counter mode and incremental interface mode**. In timer mode, the input clock for a timer is derived from the CPU clock, divided by a programmable prescaler. In counter mode, the timer is clocked in reference to external events. Pulse width or duty cycle measurement is supported in gated timer mode where the operation of a timer is controlled by the ‘gate’ level on an external input pin. For these purposes, each timer has one associated port pin (TxIN) which serves as gate or clock input. Table 8 GPT1 timer input frequencies, resolution and periods lists the timer input frequencies, resolution and periods for each pre-scaler option at 50MHz CPU clock. This also applies to the Gated Timer Mode of T3 and to the auxiliary timers T2 and T4 in Timer and Gated Timer Mode

The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD).

In Incremental Interface Mode, the GPT1 timers (T2, T3, T4) can be directly connected to the incremental position sensor signals A and B by their respective inputs TxIN and TxEUD. Direction and count signals are internally derived from these two input signals so that the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has output toggle latches (TxOTL) which changes state on each timer over-flow/ underflow. The state of this latch may be output on port pins (TxOUT) e. g. for time out monitoring of external hardware components, or may be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as capture or reload registers, timers T2 and T4 are stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at their associated input pins (TxIN). Timer T3 is reloaded with the contents of T2 or T4 triggered either by an external signal or by a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be constantly generated without software intervention.

| Name | Physical Address | 8-Bit Address | Description | Reset Value |
|---|---|---|---|---|
| IDX1 b | FF0Ah | 85h | MAC Unit Address Pointer 1 | 0000h |
| MAH | FE5Eh | 2Fh | MAC Unit Accumulator - High Word | 0000h |
| MAL | FE5Ch | 2Eh | MAC Unit Accumulator - Low Word | 0000h |
| MCW | FFDCh | EEh | MAC Unit Control Word | 0000h |
| MDC b | FF0Eh | 87h | CPU Multiply Divide Control Register | 0000h |
| MDH | FE0Ch | 06h | CPU Multiply Divide Register – High Word | 0000h |
| MDL | FE0Eh | 07h | CPU Multiply Divide Register – Low Word | 0000h |
| MRW b | FFDAh | EDh | MAC Unit Repeat Word | 0000h |
| MSW b | FFDEh | EFh | MAC Unit Status Word | 0200h |
| ODP2 b | F1C2h E | E1h | Port 2 Open Drain Control Register | -0--h |
| ODP3 b | F1C6h E | E3h | Port 3 Open Drain Control Register | 0000h |
| ODP6 b | F1CEh E | E7h | Port 6 Open Drain Control Register | 00h |
| ODP7 b | F1D2h E | E9h | Port 7 Open Drain Control Register | -0h |
| ONES | FF1Eh | 8Fh | Constant Value 1’s Register (read only) | FFFFh |
| P0L b | FF00h | 80h | Port 0 Low Register (Lower half of PORT0) | 00h |
| P0H b | FF02h | 81h | Port 0 High Register (Upper half of PORT0) | 00h |
| P1L b | FF04h | 82h | Port 1 Low Register (Lower half of PORT1) | 00h |
| P1H b | FF06h | 83h | Port 1 High Register (Upper half of PORT1) | 00h |
| P2 b | FFC0h | E0h | Port 2 Register (4 bits) | -0--h |
| P3 b | FFC4h | E2h | Port 3 Register | 0000h |
| P4 b | FFC8h | E4h | Port 4 Register (8 bits) | 00h |
| P5 b | FFA2h | D1h | Port 5 Register (read only) | XXXXh |
| P6 b | FFCCh | E6h | Port 6 Register (8 bits) | 00h |
| P7 b | FFD0h | E8h | Port 7Register (4 bits) | -0h |
| PECC0 | FEC0h | 60h | PEC Channel 0 Control Register | 0000h |
| PECC1 | FEC2h | 61h | PEC Channel 1 Control Register | 0000h |

**Table 13 Special functional registers**

| Parameter | Symbol | Limit Values | | Unit | Test Condition |
|---|---|---|---|---|---|
| | | min. | max. | | |
| PORT0 configuration current[3] | $I_{P0H}$[4] | – | -4 | µA | $V_{IN} = V_{IHmin}$ |
| | $I_{P0L}$[5] | -50 | – | µA | $V_{IN} = V_{ILmax}$ |
| RPD pulldown current[2] | $I_{RPD}$[5] | 100 | 500 | µA | $V_{OUT} = V_{DD}$ |
| XTAL1 input current | $I_{IL}$ CC | – | ±20 | µA | $0\ V < V_{IN} < V_{DD}$ |
| Pin capacitance[6] (digital inputs/outputs) | $C_{IO}$ CC | – | 10 | pF | f = 1 MHz<br>$T_A$ = 25 °C |
| Power supply current | $I_{CC}$ | – | 15 + 2.5 * $f_{CPU}$ | mA | $f_{CPU}$ in [MHz] [7] |
| Idle mode supply current | $I_{ID}$ | – | 10 + 0.9 * $f_{CPU}$ | mA | $\overline{RSTIN} = V_{IH1}$<br>$f_{CPU}$ in [MHz] [7] |
| Power-down mode supply current | $I_{PD}$ [8] | – | 200 | µA | $V_{DD}$ = 3.6 V [9] |

**Table 14 DC characteristics**

1) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the resulting voltage comes from the external circuitry.
2) This specification is only valid during reset, or interruptible power-down mode, after reception of an external interrupt signal that will wake up the CPU.
3) This specification is only valid during reset, hold or adapt-mode. Port 6 pins are only affected if they are used for $\overline{CS}$ output and the open drain function is not enabled.
4) The maximum current may be drawn while the signal line remains inactive.
5) The minimum current must be drawn in order to drive the signal line active.
6) Not 100% tested, guaranteed by design characterization.
7) Supply current is a function of operating frequency as illustrated in Figure 10 on page 44. This parameter is tested at $V_{DD}$max and 50 MHz CPU clock with all outputs disconnected and all inputs at $V_{IL}$ or $V_{IH}$ with an infinite execution of NOP instruction fetched from external memory (16-bit demux bus mode, no waitstates, no memory tri-state waitstates, normal ALE).
8) Typical value at 25°C = 20 µA.
9) This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at $V_{DD}$ – 0.1 V to $V_{DD}$, $V_{REF}$ = 0 V, all outputs (including pins configured as outputs) disconnected.

### 16.3 AC Characteristics

## Test conditions

- Input pulse levels: ..... 0 to +3.0 V
- Input rise and fall times (10%-90%): ..... 2.5 ns
- Input timing reference levels: ..... +1.5 V
- Output timing reference levels: ..... +1.5 V
- Output load: ..... see Figure 12

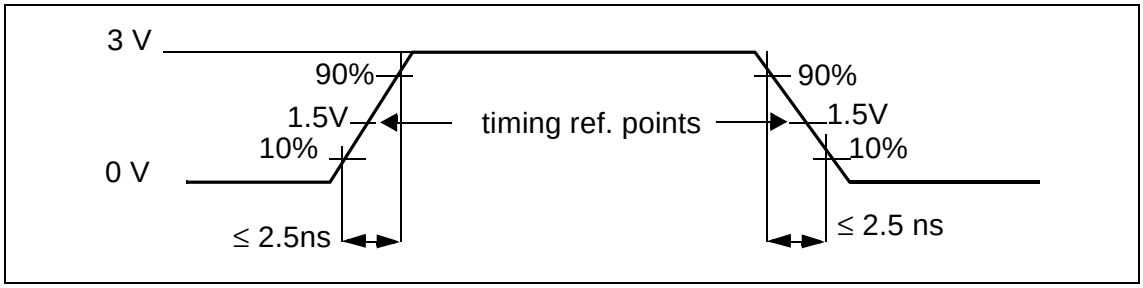


**Figure 11 Input waveforms**

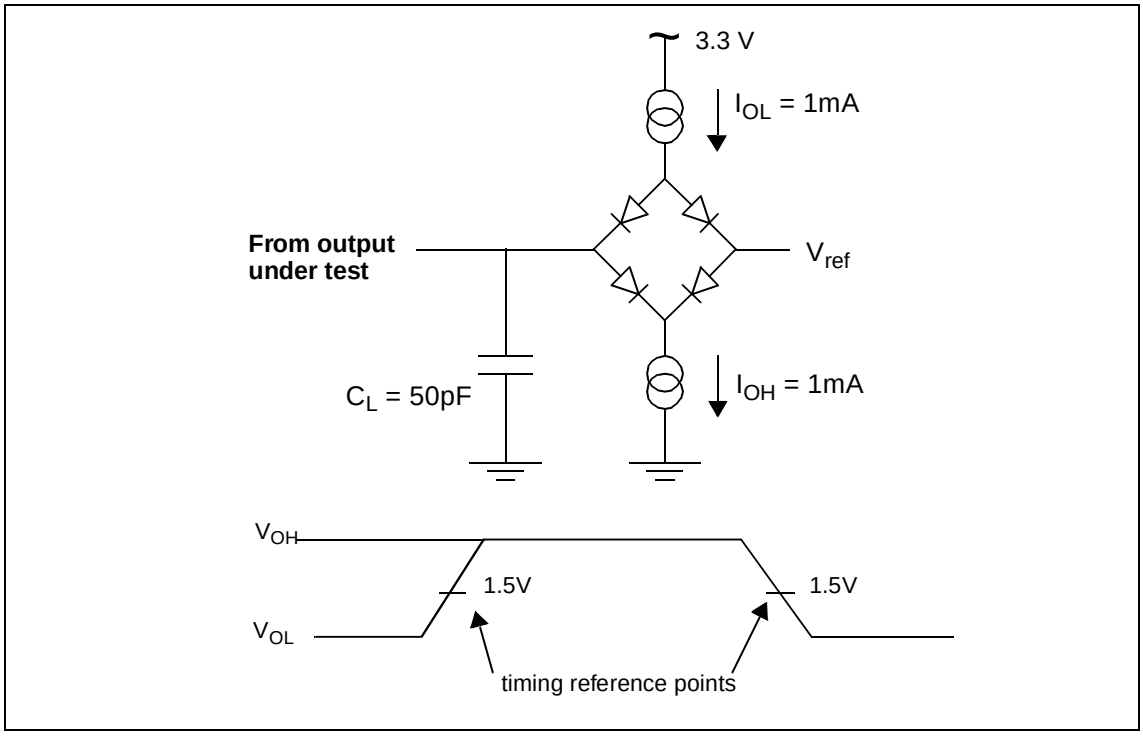


**Figure 12 Output load circuit waveform**

### 16.3.1 CPU Clock Generation Mechanisms

ST10R272L internal operation is controlled by the CPU clock $f_{CPU}$. Both edges of the CPU clock can trigger internal (e.g. pipeline) or external (e.g. bus cycles) operations. The external timing (AC Characteristics) specification therefore depends on the time between two consecutive edges of the CPU clock, called “TCL” (see figure below).

The CPU clock signal can be generated by different mechanisms. The duration of TCLs and their variation (and also the external timing) depends on the $f_{CPU}$ generation mechanism. This must be considered when calculating ST10R272L timing.

The CPU clock generation mechanism is set during reset by the logic levels on pins P0.15-13 (P0H.7-5).

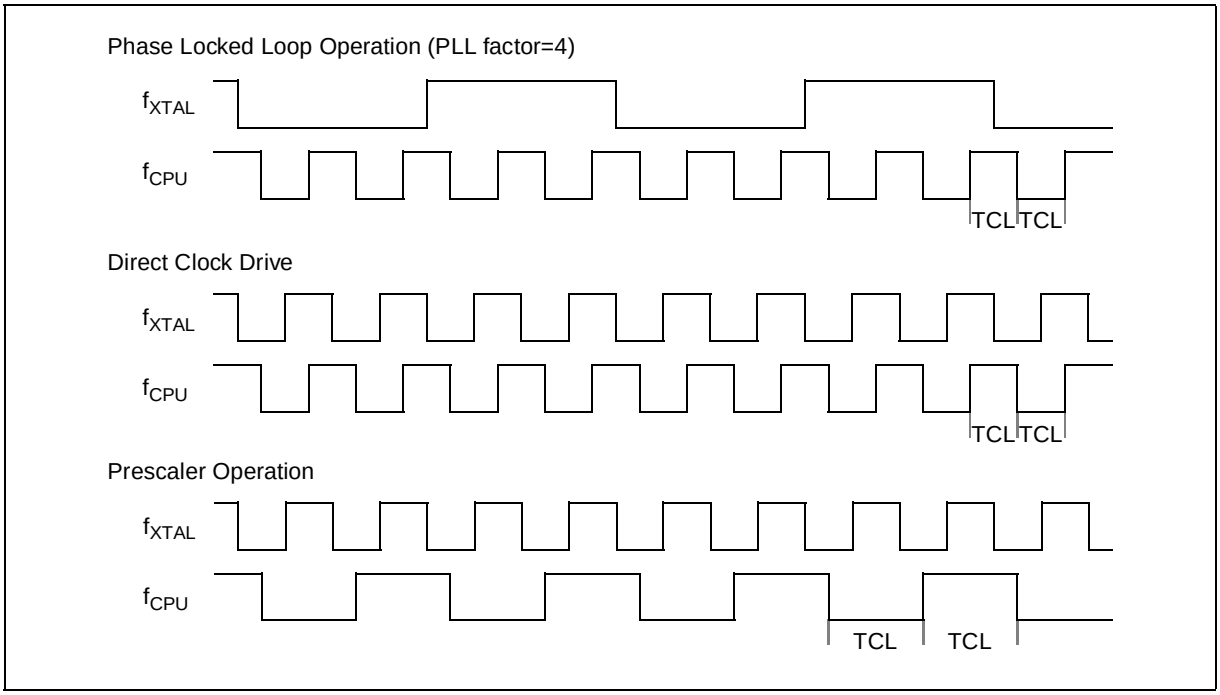


**Figure 14 CPU clock generation mechanisms**

| P0.15-13 (P0H.7-5) | | | CPU frequency $f_{CPU} = f_{XTAL} * F$ | External clock input range 10-50MHz | Notes |
|---|---|---|---|---|---|
| 1 | 1 | 1 | $F_{XTAL} * 4$ | 2.5 to 12.5 MHz | Default configuration |
| 1 | 1 | 0 | $F_{XTAL} * 3$ | 3.33 to 16.66 MHz | |
| 1 | 0 | 1 | $F_{XTAL} * 2$ | 5 to 25 MHz | |

**Table 15 CPU clock generation mechanisms**

| P0.15-13 (P0H.7-5) | | | CPU frequency $f_{CPU} = f_{XTAL} * F$ | External clock input range 10-50MHz | Notes |
|---|---|---|---|---|---|
| 1 | 0 | 0 | $F_{XTAL} * 5$ | 2 to 10 MHz | |
| 0 | 1 | 1 | $F_{XTAL} * 1$ | 1 to 50 MHz | Direct drive 1) |
| 0 | 1 | 0 | $F_{XTAL} * 1.5$ | 6.66 to 33.33 MHz | |
| 0 | 0 | 1 | $F_{XTAL} / 2$ | 2 to 100 MHz | CPU clock via 2:1 prescaler |
| 0 | 0 | 0 | $F_{XTAL} * 2.5$ | 4 to 20 MHz | |

**Table 15 CPU clock generation mechanisms**

1) The maximum depends on the duty cycle of the external clock signal. The maximum input frequency is 25 MHz when using an external crystal oscillator, but higher frequencies can be applied with an external clock source.

## Prescaler operation

Set when pins P0.15-13 (P0H.7-5) equal '001' during reset, the CPU clock is derived from the internal oscillator (input clock signal) by a 2:1 prescaler.
The frequency of $f_{CPU}$ is half the frequency of $f_{XTAL}$ and the high and low time of $f_{CPU}$ (i.e. the duration of an individual TCL) is defined by the period of the input clock $f_{XTAL}$.

The timings listed in the AC characteristics that refer to TCLs therefore can be calculated using the period of $f_{XTAL}$ for any TCL.

Note that if the bit OWDDIS in SYSCON register is cleared, the PLL runs on its free-running frequency and delivers the clock signal for the Oscillator Watchdog. If bit OWDDIS is set, then the PLL is switched off.

## Direct drive

When pins P0.15-13 (P0H.7-5) equal '011' during reset, the on-chip phase locked loop is disabled and the CPU clock is driven from the internal oscillator with the input clock signal. The frequency of $f_{CPU}$ directly follows the frequency of $f_{XTAL}$ so the high and low time of $f_{CPU}$ (i.e. the duration of an individual TCL) is defined by the duty cycle of the input clock $f_{XTAL}$.

The TCL timing below must be calculated using the minimum possible TCL which can be calculated by the formula: $TCL_{min} = 1/f_{XTAL} \times DC_{min} (DC = \text{duty cycle})$

For two consecutive TCLs the deviation caused by the duty cycle of $f_{XTAL}$ is compensated so the duration of 2TCL is always $1/f_{XTAL}$. Therefore, the minimum value $TCL_{min}$ has to be used only once for timings that require an odd number of TCLs (1,3,...). Timings that require an even number of TCLs (2,4,...) may use the formula: $2TCL = 1/f_{XTAL}$.

### 16.3.3 Multiplexed Bus

$V_{DD}$ = 3.3 V ± 0.3 V $V_{SS}$ = 0 V $T_A$ = -40 to +85 °C $C_L$ = 50 pF

ALE cycle time = 6 TCL + $2t_A$ + $t_C$ + $t_F$ (60 ns at 50-MHz CPU clock without waitstates)

| Parameter | Symbol | | Max. CPU Clock = 50 MHz | | Variable CPU Clock 1/2TCL = 1 to 50 MHz | | Unit |
|---|---|---|---|---|---|---|---|
| | | | min. | max. | min. | max. | |
| ALE high time | $t_5$ | CC | 7 + $t_A$ | – | TCL - 3 + $t_A$ | – | ns |
| Address (P1, P4), $\overline{BHE}$ setup to ALE | $t_6$ | CC | 3 + $t_A$ | – | TCL - 7 + $t_A$ | – | ns |
| Address (P0) setup to ALE | $t_{6m}$ | CC | 5 + $t_A$ | – | TCL - 5 + $t_A$ | – | ns |
| Address hold after ALE | $t_7$ | CC | 5 + $t_A$ | – | TCL - 5 + $t_A$ | – | ns |
| ALE falling edge to $\overline{RD}$, $\overline{WR}$ (with RW-delay) | $t_8$ | CC | 5 + $t_A$ | – | TCL - 5 + $t_A$ | – | ns |
| ALE falling edge to $\overline{RD}$, $\overline{WR}$ (no RW-delay) | $t_9$ | CC | -5 + $t_A$ | – | -5 + $t_A$ | – | ns |
| Address float after $\overline{RD}$, (with RW-delay)[1)] | $t_{10}$ | CC | – | 5[1] | – | 5[1] | ns |
| Address float after $\overline{RD}$, (no RW-delay)[1] | $t_{11}$ | CC | – | 15[1] | – | TCL + 5[1] | ns |
| $\overline{RD}$, $\overline{WR}$ low time (with RW-delay) | $t_{12}$ | CC | 13 + $t_C$ | – | 2TCL - 7+ $t_C$ | – | ns |
| $\overline{RD}$, $\overline{WR}$ low time (no RW-delay) | $t_{13}$ | CC | 23 + $t_C$ | – | 3TCL - 7 + $t_C$ | – | ns |
| $\overline{RD}$ to valid data in (with RW-delay) | $t_{14}$ | SR | – | 5 + $t_C$ | – | 2TCL - 15 + $t_C$ | ns |
| $\overline{RD}$ to valid data in (no RW-delay) | $t_{15}$ | SR | – | 15 + $t_C$ | – | 3TCL - 15 + $t_C$ | ns |
| ALE low to valid data in | $t_{16}$ | SR | – | 15 + $t_A$ + $t_C$ | – | 3TCL - 15 + $t_A$ + $t_C$ | ns |
| Address to valid data in | $t_{17}$ | SR | – | 20 + $2t_A$ + $t_C$ | – | 4TCL - 20 + $2t_A$ + $t_C$ | ns |

**Table 17 Multiplexed bus**

| Parameter | Symbol | | Max. CPU Clock = 50 MHz | | Variable CPU Clock 1/2TCL = 1 to 50 MHz | | Unit |
|---|---|---|---|---|---|---|---|
| | | | min. | max. | min. | max. | |
| $\overline{RdCS}$ to Valid Data In (with RW delay) | $t_{46}$ | SR | – | 3 + $t_C$ | – | 2TCL - 17 + $t_C$ | ns |
| $\overline{RdCS}$ to Valid Data In (no RW delay) | $t_{47}$ | SR | – | 13 + $t_C$ | – | 3TCL - 17 + $t_C$ | ns |
| $\overline{RdCS}$, $\overline{WrCS}$ Low Time (with RW delay) | $t_{48}$ | CC | 13 + $t_C$ | – | 2TCL - 7+ $t_C$ | – | ns |
| $\overline{RdCS}$, $\overline{WrCS}$ Low Time (no RW delay) | $t_{49}$ | CC | 23 + $t_C$ | – | 3TCL - 7+ $t_C$ | – | ns |
| Data valid to $\overline{WrCS}$ | $t_{50}$ | CC | 10 + $t_C$ | – | 2TCL - 10 + $t_C$ | – | ns |
| Data hold after $\overline{RdCS}$ | $t_{51}$ | SR | 0 | – | 0 | – | ns |
| Data float after $\overline{RdCS}$[1 2] | $t_{52}$ | SR | – | 13 + $t_F$[2] | – | 2TCL - 7 + $t_F$[2] | ns |
| Address hold after $\overline{RdCS}$, $\overline{WrCS}$ | $t_{54}$ | CC | 10 + $t_F$ | – | 2TCL - 10 + $t_F$ | – | ns |
| Data hold after $\overline{WrCS}$ | $t_{56}$ | CC | 10 + $t_F$ | – | 2TCL - 10 + $t_F$ | – | ns |

**Table 17 Multiplexed bus**

1) Output loading is specified using Figure 13 (CL = 5 pF).

2) This delay assumes that the following bus cycle is a multiplexed bus cycle. If next bus cycle is demultiplexed, refer to demuxultiplexed equivalent AC timing.

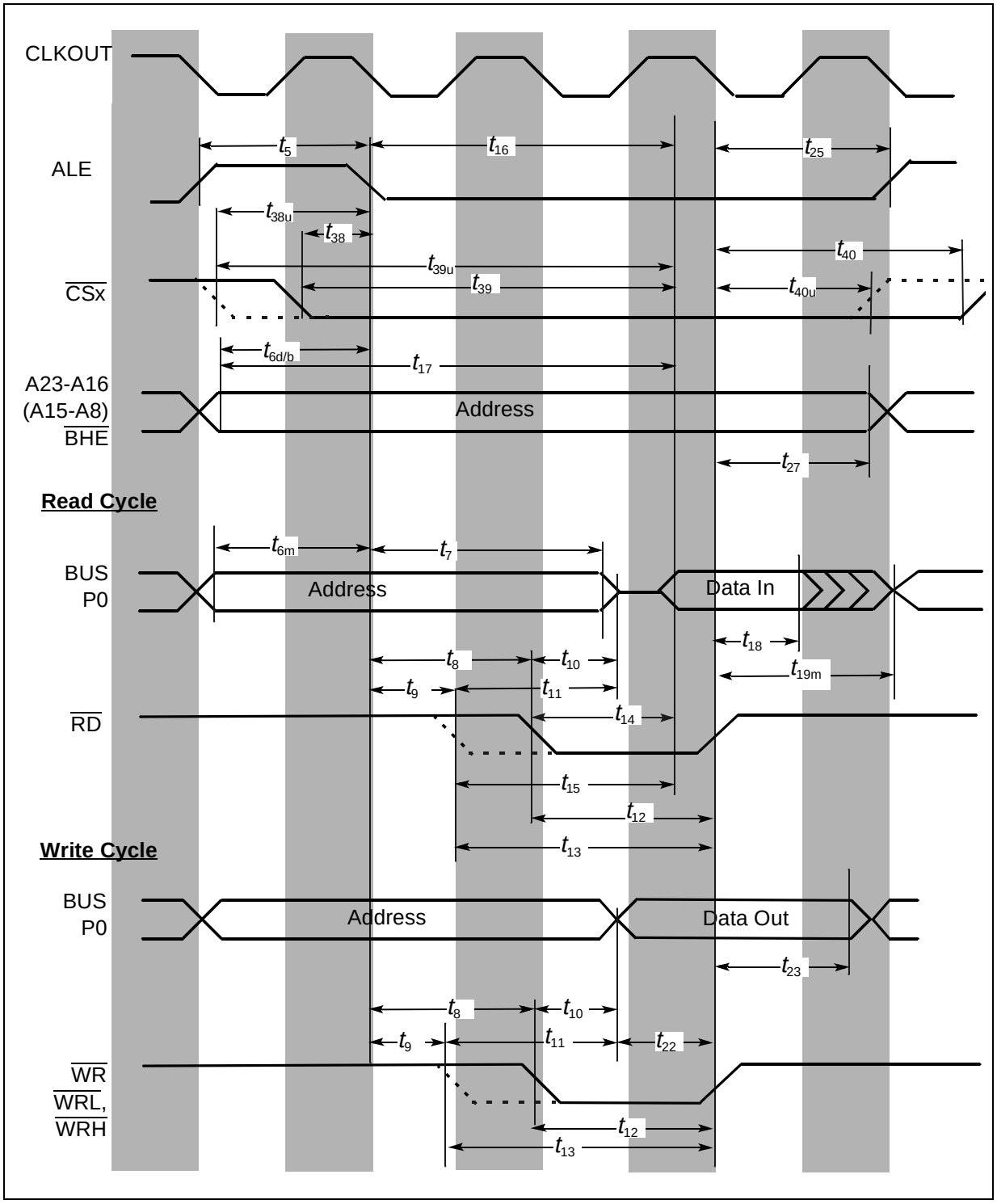


**Figure 17 External memory cycle:**
**multiplexed bus, with/without read/write delay, extended ALE**

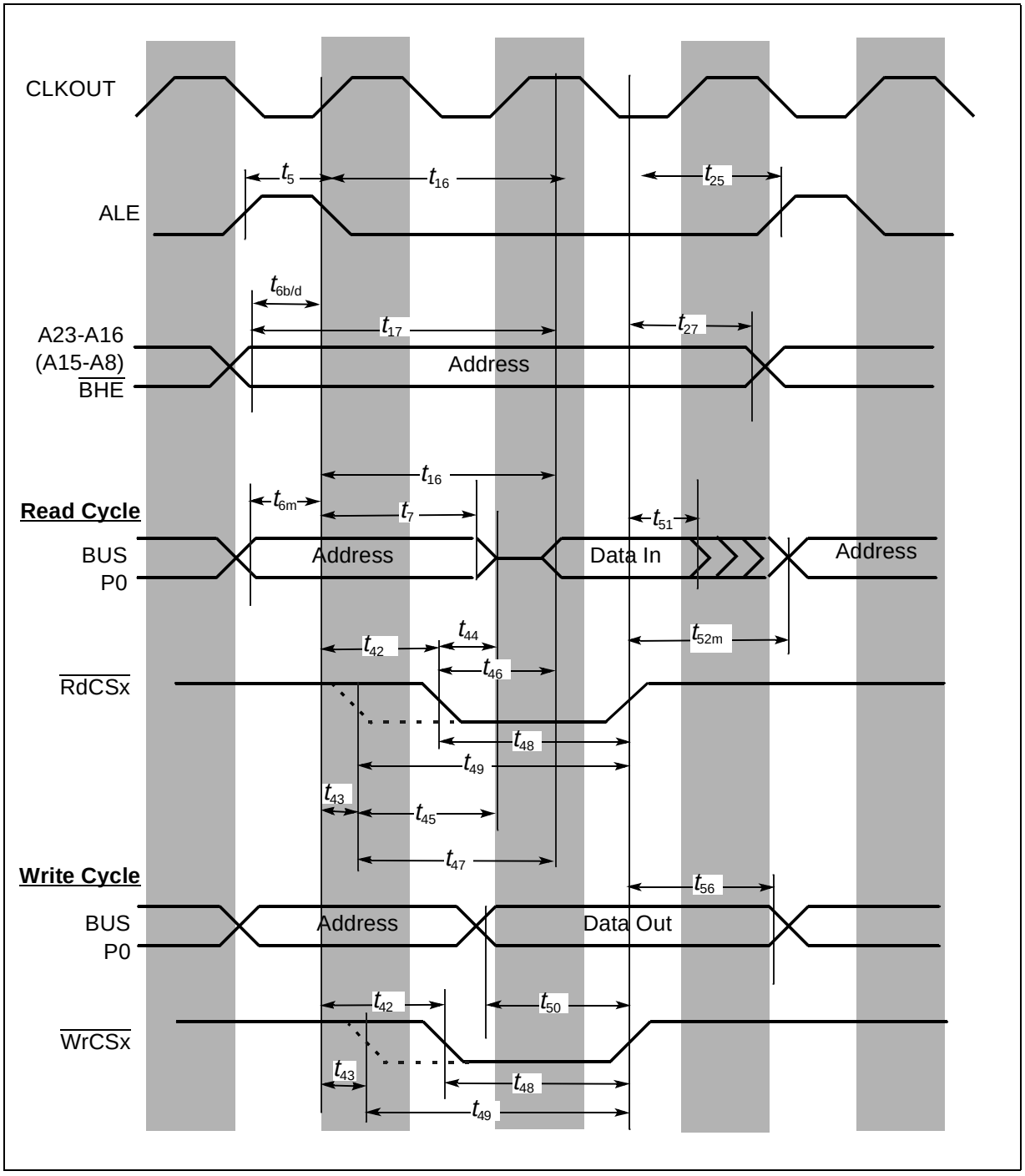


**Figure 18 External memory cycle:**
**multiplexed bus, with/without read/write delay, normal ALE, read/write chip select**

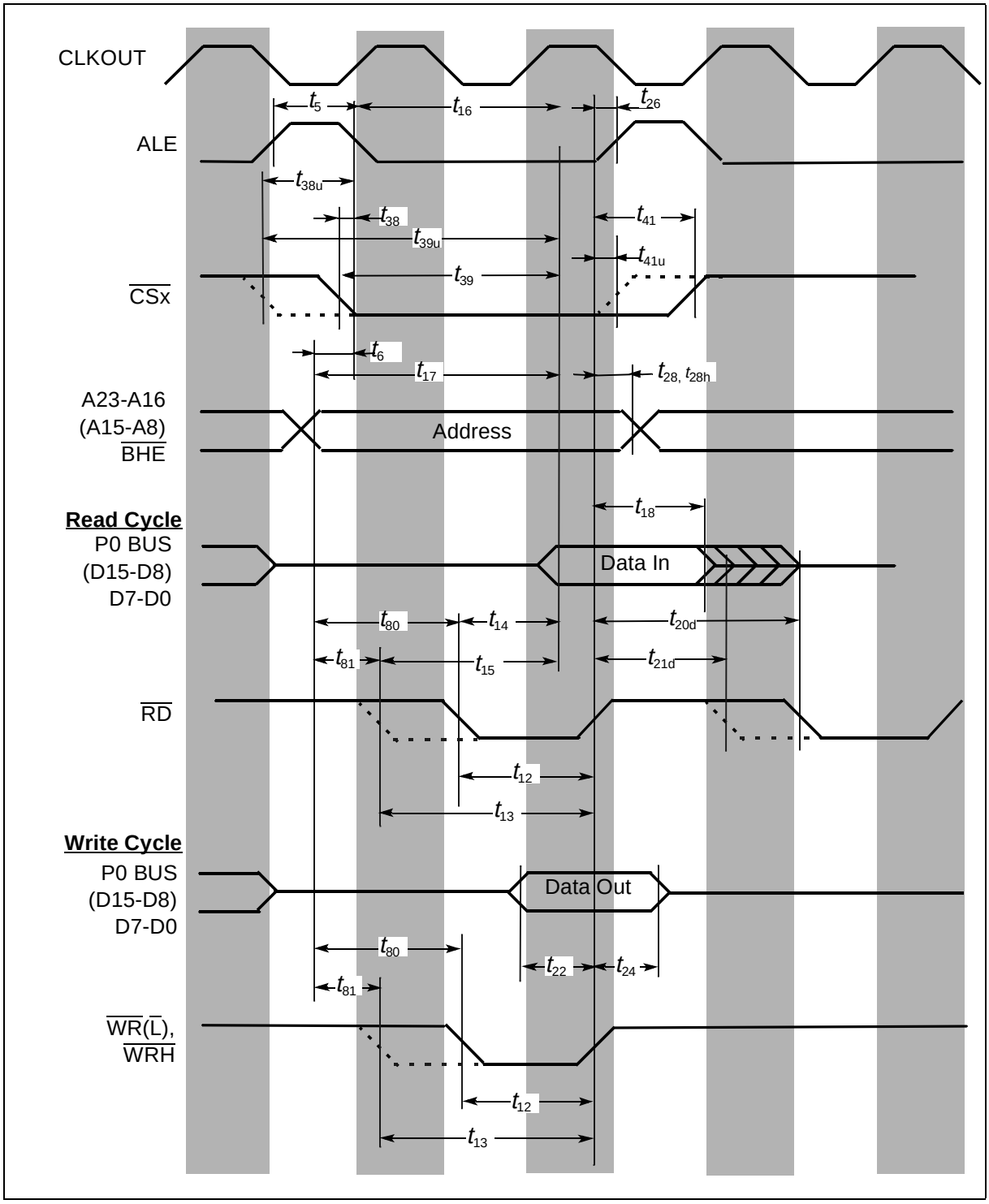


**Figure 20 External memory cycle:**
**demultiplexed bus, with/without read/write delay, normal ALE**

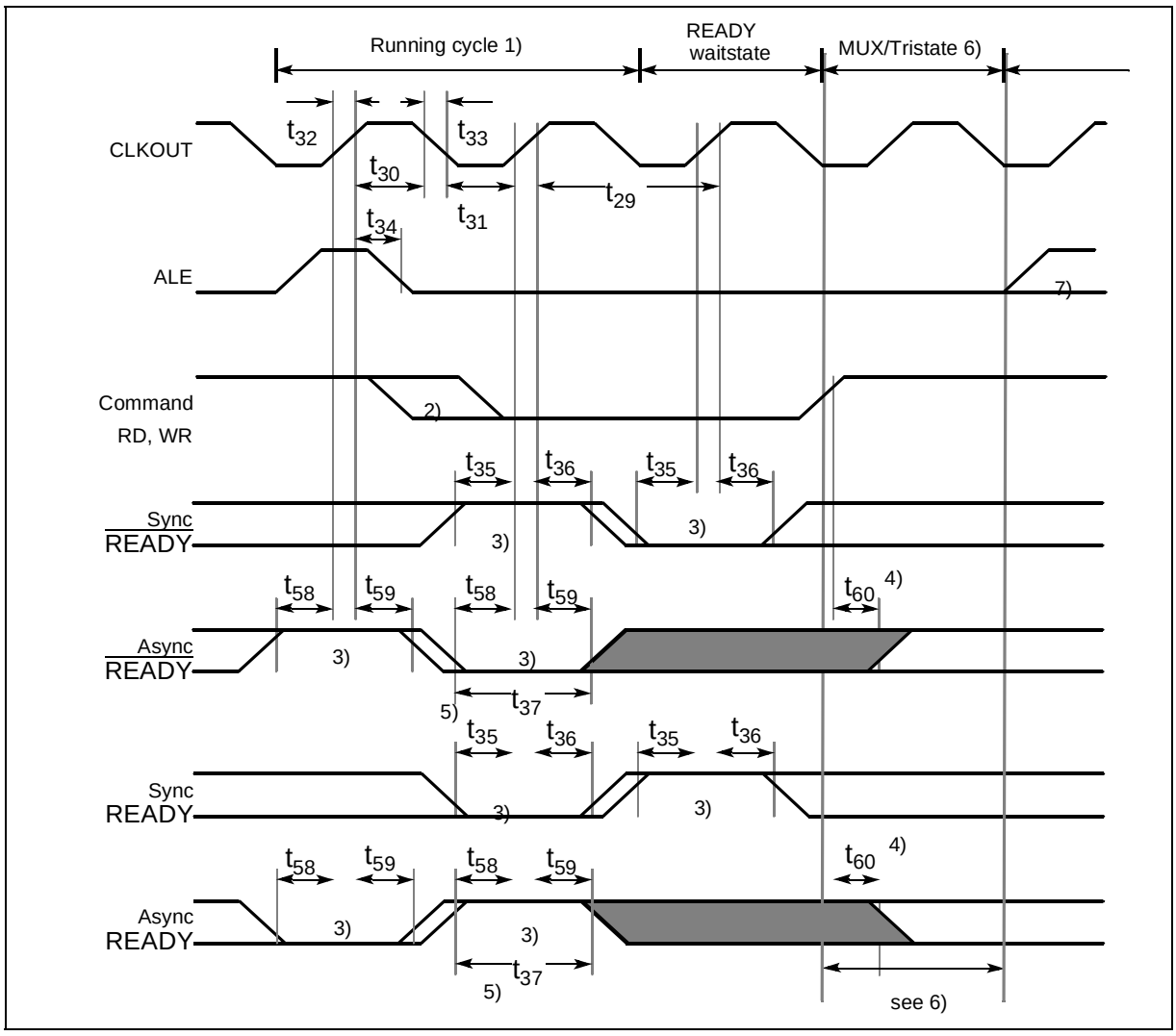


**Figure 24 CLKOUT and $\overline{\text{READY}}$/READY**

1 Cycle as programmed, including MCTC waitstates (Example shows 0 MCTC WS).

2 The leading edge of the respective command depends on RW-delay.

3 $\overline{\text{READY}}$ (or READY) sampled HIGH (resp. LOW) at this sampling point generates a READY controlled waitstate, $\overline{\text{READY}}$ (resp. READY) sampled LOW (resp. HIGH) at this sampling point terminates the currently running bus cycle.

4 $\overline{\text{READY}}$ (resp. READY) may be deactivated in response to the trailing (rising) edge of the corresponding command ($\overline{\text{RD}}$ or $\overline{\text{WR}}$).

5 If the Asynchronous $\overline{\text{READY}}$ (or READY) signal does not fulfill the indicated setup and hold times with respect to CLKOUT (e.g. because CLKOUT is not enabled), it must fulfill t 37 in order to be safely synchronized. This is guaranteed, if READY is removed in response to the command (see Note 4)).

### 16.3.6 External Bus Arbitration

$V_{DD}$ = 3.3 V ± 0.3 V $V_{SS}$ = 0 V $T_A$ = -40 to +85 °C $C_L$ = 50 pF

| Parameter | Symbol | | Max. CPU Clock = 50 MHz | | Variable CPU Clock 1/2TCL = 1 to 50 MHz | | Unit |
|---|---|---|---|---|---|---|---|
| | | | min. | max. | min. | max. | |
| $\overline{HOLD}$ input setup time to CLKOUT | $t_{61}$ | SR | 15 | – | 15 | – | ns |
| CLKOUT to $\overline{HLDA}$ high or $\overline{BREQ}$ low delay | $t_{62}$ | CC | – | 10 | – | 10 | ns |
| CLKOUT to $\overline{HLDA}$ low or $\overline{BREQ}$ high delay | $t_{63}$ | CC | – | 10 | – | 10 | ns |
| $\overline{CSx}$ release | $t_{64}$ | CC | – | 15 | – | 15 | ns |
| $\overline{CSx}$ drive | $t_{65}$ | CC | -3 | 15 | -3 | 15 | ns |
| Other signals release | $t_{66}$ | CC | – | 15 | – | 15 | ns |
| Other signals drive | $t_{67}$ | CC | -3 | 15 | -3 | 15 | ns |

**Table 20 External bus arbitration**

### 16.3.7 External Hardware Reset

$V_{DD}$ = 3.3 V ± 0.3 V  $V_{SS}$ = 0 V  $T_A$ = -40 to +85 °C  $C_L$ = 50 pF

| Parameter | Symbol | | Max. CPU Clock = 50 MHz | | Variable CPU Clock 1/2TCL = 1 to 50 MHz | | Unit |
|---|---|---|---|---|---|---|---|
| | | | min. | max. | min. | max. | |
| Sync. $\overline{\text{RSTIN}}$ low time[1)] | $t_{70}$ | SR | 50 | – | 4 TCL + 10 | – | ns |
| $\overline{\text{RSTIN}}$ low to internal reset sequence start | $t_{71}$ | CC | 4 | 16 | 4 | 16 | TCL |
| internal reset sequence, ($\overline{\text{RSTIN}}$ internally pulled low) | $t_{72}$ | CC | 1024 | 1024 | 1024 | 1024 | TCL |
| $\overline{\text{RSTIN}}$ rising edge to internal reset condition end | $t_{73}$ | CC | 4 | 6 | 4 | 6 | TCL |
| PORT0 system start-up configuration setup to $\overline{\text{RSTIN}}$ rising edge [2)] | $t_{74}$ | SR | 100 | – | 100 | – | ns |
| PORT0 system start-up configuration hold after $\overline{\text{RSTIN}}$ rising edge | $t_{75}$ | SR | 1 | 6 | 1 | 6 | TCL |
| Bus signals drive from internal reset end | $t_{76}$ | CC | 0 | 20 | 0 | 20 | ns |
| $\overline{\text{RSTIN}}$ low to signals release | $t_{77}$ | CC | – | 50 | – | 50 | ns |
| ALE rising edge from internal reset condition end | $t_{78}$ | CC | 8 | 8 | 8 | 8 | TCL |
| Async. $\overline{\text{RSTIN}}$ low time[1] | $t_{79}$ | SR | 1500 | – | 1500 | – | ns |

**Table 21 External hardware reset**

1) On power-up reset, the $\overline{\text{RSTIN}}$ pin must be asserted until a stable clock signal is available (about 10...50 ms to allow the on-chip oscillator to stabilize) and until System Start-up Configuration is correct on PORT0 (about 50 µs for internal pullup devices to load 50 pF from $V_{IL}$min to $V_{IH}$min).

2) The value of bits 0 (EMU), 1 (ADAPT), 13 to 15 (Clock Configuration) are loaded during hardware reset as long as internal reset signal is active, and have an immediate effect on the system.

### 16.3.8 Synchronous Serial Port Timing

$V_{CC}$ = 3.3 V ± 0.3 V $V_{SS}$ = 0 V $T_A$ = -40 to +85 °C $C_L$ = 50 pF

| Parameter | Symbol | | Max. Baudrate = 25 MBd | | Variable Baudrate = 0.2 to 25 MBd | | Unit |
|---|---|---|---|---|---|---|---|
| | | | min. | max. | min. | max. | |
| SSP clock cycle time | $t_{200}$ | CC | 40 | 40 | 4 TCL | 512 TCL | ns |
| SSP clock high time | $t_{201}$ | CC | 13 | – | $t_{200}/2$ - 7 | – | ns |
| SSP clock low time | $t_{202}$ | CC | 13 | – | $t_{200}/2$ - 7 | – | ns |
| SSP clock rise time | $t_{203}$ | CC | – | 3 | – | 3 | ns |
| SSP clock fall time | $t_{204}$ | CC | – | 3 | – | 3 | ns |
| CE active before shift edge | $t_{205}$ | CC | 13 | – | $t_{200}/2$ - 7 | – | ns |
| CE inactive after latch edge | $t_{206}$ | CC | 33 | 47 | $t_{200}$ - 7 | $t_{200}$ + 7 | ns |
| Write data valid after shift edge | $t_{207}$ | CC | – | 7 | – | 7 | ns |
| Write data hold after shift edge | $t_{208}$ | CC | 0 | – | 0 | – | ns |
| Write data hold after latch edge | $t_{209}$ | CC | 15 | 25 | $t_{200}/2$ - 5 | $t_{200}/2$ + 5 | ns |
| Read data active after latch edge | $t_{210}$ | SR | 27 | – | $t_{200}/2$ + 7 | – | ns |
| Read data setup time before latch edge | $t_{211}$ | SR | 15 | – | 15 | – | ns |
| Read data hold time after latch edge | $t_{212}$ | SR | 0 | – | 0 | – | ns |

**Table 22 Synchronous serial port timing**