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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST10
Core Size	16-Bit
Speed	50MHz
Connectivity	EBI/EMI, SSP, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	77
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st10r272lt1

4 CENTRAL PROCESSING UNIT

The main core of the CPU contains a 4-stage instruction pipeline, a MAC multiply-accumulation unit, a separate multiply and divide unit, a bit-mask generator and a barrel shifter. Most instructions can be executed in one machine cycle requiring 40ns at 50MHz CPU clock.

The CPU includes an actual register context consisting of 16 wordwide GPRs physically located in the on-chip RAM area. A Context Pointer (CP) register determines the base address of the active register bank to be accessed by the CPU. The number of register banks is only restricted by the available internal RAM space. For easy parameter passing, one register bank may overlap others.

A system stack of up to 1024 bytes is provided as a storage for temporary data. The system stack is allocated in the on-chip RAM area, and it is accessed by the CPU via the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are compared against the stack pointer value during each stack access to detect stack overflow or underflow.

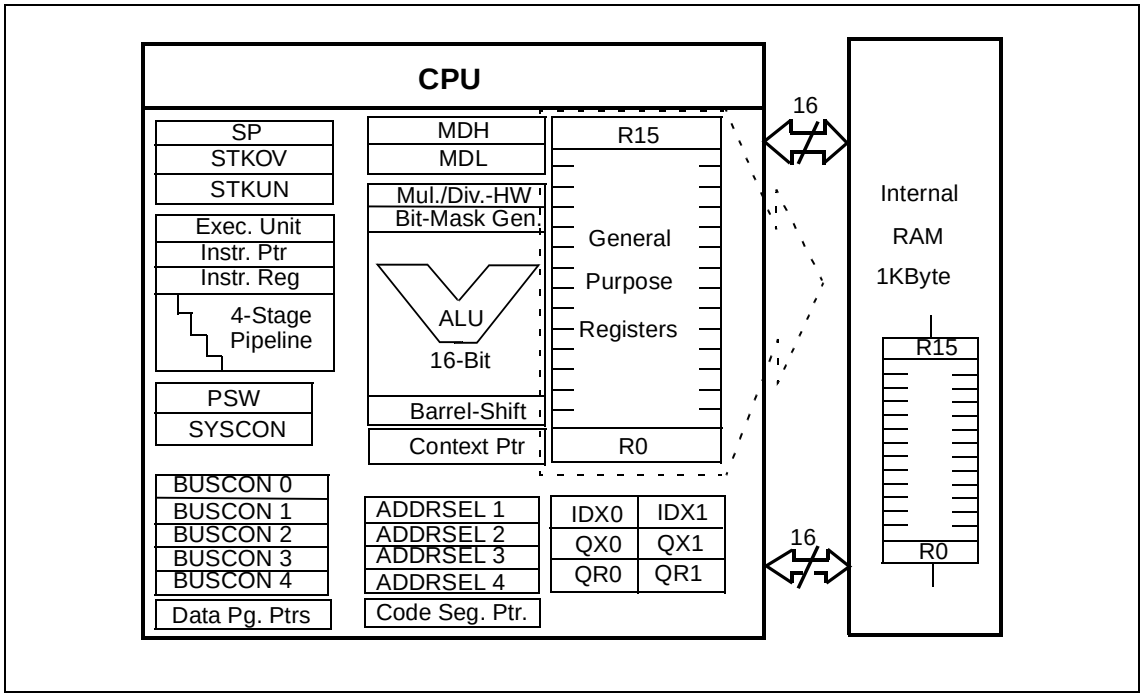

Figure 4 CPU block diagram

5 MULTIPLY-ACCUMULATE UNIT (MAC)

The MAC is a specialized co-processor added to the ST10R272L CPU core to improve the performance of signal processing algorithms. It includes:

- a multiply-accumulate unit
- an address generation unit, able to feed the mac unit with 2 operands per cycle
- a repeat unit, to execute a series of multiply-accumulate instructions

New addressing capabilities enable the CPU to supply the MAC with up to 2 operands per instruction cycle. MAC instructions: multiply, multiply-accumulate, 32-bit signed arithmetic operations and the CoMOV transfer instruction have been added to the standard instruction set. Full details are provided in the 'ST10 Family Programming Manual'.

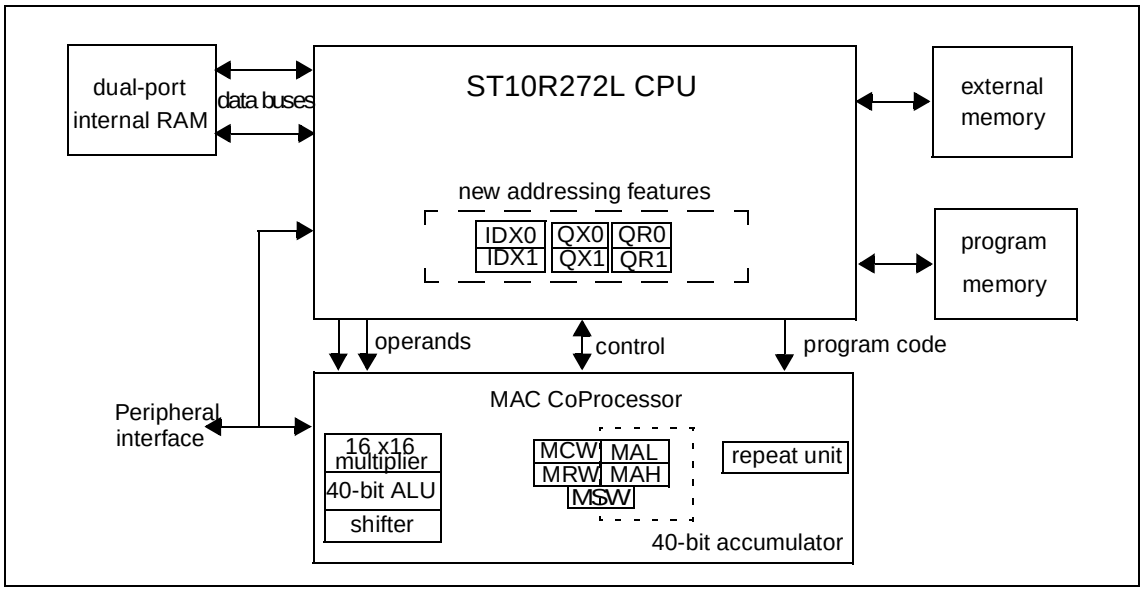

Figure 5 MAC architecture

input ports can receive 00,0000,0000h to allow direct transfers from the B-source and A-source, respectively, to the Accumulator (case of Multiplication, Shift.). The output of the arithmetic unit goes to the Accumulator.

It is also possible to saturate the Accumulator on a 32-bit value, automatically after every accumulation. Automatic saturation is enabled by setting the saturation bit MS in the MCW register. When the Accumulator is in the saturation mode and an 32-bit overflow occurs, the accumulator is loaded with either the most positive or the most negative value representable in a 32-bit value, depending on the direction of the overflow. The value of the Accumulator upon saturation is 00,7fff,ffffh (positive) or ff,8000,0000h (negative) in signed arithmetic. Automatic saturation sets the SL flag MSW. This flag is a sticky flag which means it stays set until it is explicitly reset by the user.

40-bit overflow of the Accumulator sets the SV flag in MSW. This flag is also a sticky flag.

40-bit accumulator register

The 40-bit Accumulator consists of three SFR registers MAH, MAL and MAE. MAH and MAL are 16-bit wide. MAE is 8-bit wide and is contained within the least significant byte of MSW. Most co-processor operations specify the 40-bit Accumulator register as source and/or destination operand.

Data limiter

Saturation arithmetic is also provided to selectively limit overflow, when reading the accumulator by means of a CoSTORE <destination> MAS instruction. Limiting is performed on the MAC Accumulator. If the contents of the Accumulator can be represented in the destination operand size without overflow, the data limiter is disabled and the operand is not modified. If the contents of the accumulator cannot be represented without overflow in the destination operand size, the limiter will substitute a ‘limited’ data as explained in the following table.

Register	E bit	N bit	Output of the Limiter
x	0	x	unchanged
MAS	1	0	7fffh
MAS	1	1	8000h

Table 4 Data Limit Values

Note *In this case, the accumulator and the status register are not affected. MAS readable from a CoSTORE instruction.*

Accumulator shifter

The Accumulator shifter is a parallel shifter with a 40-bit input and a 40-bit output. The source operand of the shifter is the Accumulator and the possible shifting operations are:

- No shift (Unmodified)
- Up to 8-bit Arithmetic Left Shift
- Up to 8-bit Arithmetic Right Shift

E, SV and SL bits from MSW are affected by Left shifts, therefore if the saturation mechanism is enabled (MS), the behavior is similar to the one of the arithmetic unit. The carry flag C is also affected by left shifts.

Repeat unit

The MAC includes a repeat unit allowing the repetition of some co-processor instructions up to 2^{13} (8192) times. The repeat count may be specified either by an immediate value (up to 31 times) or by the content of the Repeat Count (bits 12 to 0) in the MAC Repeat Word (MRW). If the Repeat Count equals “N” the instruction will be executed “N+1” times. At each iteration of a cumulative instruction the Repeat Count is tested for zero. If it is zero the instruction is terminated else the Repeat Count is decremented and the instruction is repeated. During such a repeat sequence, the Repeat Flag in MRW is set until the last execution of the repeated instruction.

The syntax of repeated instructions is shown in the following examples:

```
1         Repeat #24 times
          CoMAC[IDX0+],[R0+]       ; repeated 24 times
```

In example 1, the instruction is repeated according to a 5-bit immediate value. The Repeat Count in MRW is automatically loaded with this value minus one (MRW=23).

```
1         MOV MRW, #00FFh          ; load MRW
          NOP                      ; instruction latency
          Repeat MRW times
          CoMACM [IDX1-],[R2+]     ; repeated 256 times
```

In this example, the instruction is repeated according to the Repeat Count in MRW. Notice that due to the pipeline processing at least one instruction should be inserted between the write of MRW and the next repeated instruction.

Repeat sequences may be interrupted. When an interrupt occurs during a repeat sequence, the sequence is stopped and the interrupt routine is executed. The repeat sequence resumes at the end of the interrupt routine. During the interrupt, MR remains set, indicating that a repeated instruction has been interrupted and the Repeat Count holds the number (minus 1)

of repetition that remains to complete the sequence. If the Repeat Unit is used in the interrupt routine, MRW must be saved by the user and restored before the end of the interrupt routine.

Note The Repeat Count should be used with caution. In this case MR should be written as 0. In general MR should not be set by the user otherwise correct instruction processing can not be guaranteed.

MAC interrupt

The MAC can generate an interrupt according to the value of the status flags C (carry), SV (overflow), E (extension) or SL (limit) of the MSW. The MAC interrupt is globally enabled when the MIE flag in MCW is set. When it is enabled the flags C, SV, E or SL can triggered a MAC interrupt when they are set provided that the corresponding mask flag CM, VM, EM or LM in MCW is also set. A MAC interrupt request set the MIR flag in MSW, this flag must be reset by the user during the interrupt routine otherwise the interrupt processing restarts when returning from the interrupt routine.

The MAC interrupt is implemented as a Class B hardware trap (trap number Ah - trap priority I). The associated Trap Flag in the TFR register is MACTRP, bit #6 of the TFR (Remember that this flag must also be reset by the user in the case of an MAC interrupt request).

As the MAC status flags are updated (or eventually written by software) during the Execute stage of the pipeline, the response time of a MAC interrupt request is 3 instruction cycles (see Figure 3). It is the number of instruction cycles required between the time the request is sent and the time the first instruction located at the interrupt vector location enters the pipeline. Note that the IP value stacked after a MAC interrupt does not point to the instruction that triggers the interrupt.

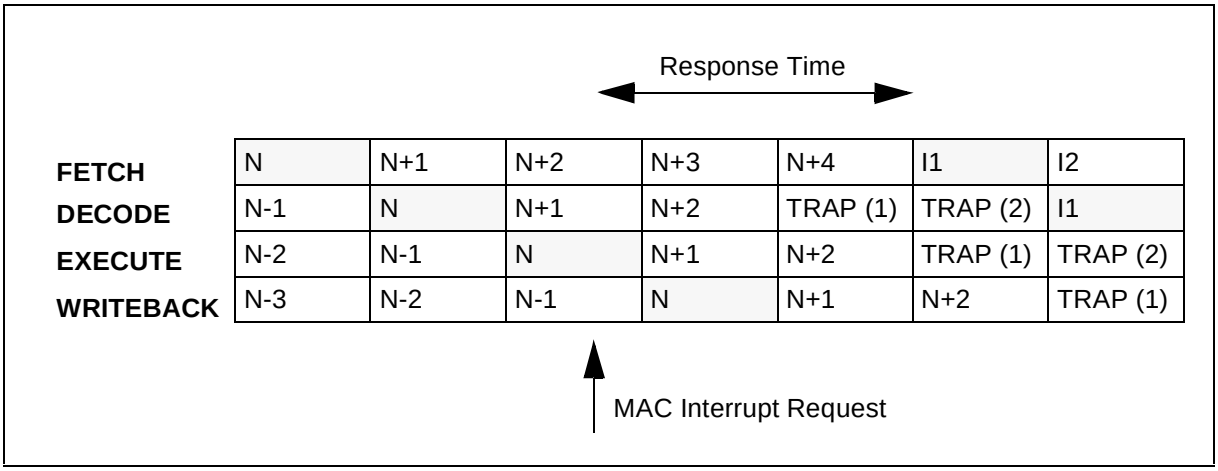

Figure 7 Pipeline diagram for MAC interrupt response time

6.1 Interrupt Sources

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
External Interrupt 0	CC8IR	CC8IE	CC8INT	60h	18h
External Interrupt 1	CC9IR	CC9IE	CC9INT	64h	19h
External Interrupt 2	CC10IR	CC10IE	CC10INT	68h	1Ah
External Interrupt 3	CC11IR	CC11IE	CC11INT	6Ch	1Bh
GPT1 Timer 2	T2IR	T2IE	T2INT	88h	22h
GPT1 Timer 3	T3IR	T3IE	T3INT	8Ch	23h
GPT1 Timer 4	T4IR	T4IE	T4INT	90h	24h
GPT2 Timer 5	T5IR	T5IE	T5INT	94h	25h
GPT2 Timer 6	T6IR	T6IE	T6INT	98h	26h
GPT2 CAPREL Register	CRIR	CRIE	CRINT	9Ch	27h
ASC0 Transmit	S0TIR	S0TIE	S0TINT	A8h	2Ah
ASC0 Transmit Buffer	S0TBIR	S0TBIE	S0TBINT	11Ch	47h
ASC0 Receive	S0RIR	S0RIE	S0RINT	ACh	2Bh
ASC0 Error	S0EIR	S0EIE	S0EINT	B0h	2Ch
PWM Channel 3	PWMIR	PWMIE	PWMINT	FCh	3Fh
SSP Interrupt	XP1IR	XP1IE	XP1INT	104h	41h
PLL Unlock	XP3IR	XP3IE	XP3INT	10Ch	43h

Table 5 List of possible interrupt sources, flags, vector and trap numbers

13 SYSTEM RESET

The following type of reset are implemented on the ST10R272L:

Asynchronous hardware reset: Asynchronous reset does not require a stabilized clock signal on XTAL1 as it is not internally resynchronized, it resets the microcontroller into its default reset state. Asynchronous reset is required on chip power-up and can be used during catastrophic situations. The rising edge of the RSTIN pin is internally resynchronized before exiting the reset condition, therefore, only the entry to hardware reset is asynchronous.

Synchronous hardware reset (warm reset): A warm synchronous hardware reset is triggered when the reset input signal $\overline{\text{RSTIN}}$ is latched low and Vpp pin is high. The I/Os are immediately (asynchronously) set in high impedance, $\overline{\text{RSTOUT}}$ is driven low. After $\overline{\text{RSTIN}}$ negation is detected, a short transition period elapses, during which pending internal hold states are cancelled and any current internal access cycles are completed, external bus cycles are aborted. Then, the internal reset sequence is active for 1024 TCL (512 CPU clock cycles). During this reset sequence, if bit BDRSTEN was previously set by software (bit 3 in SYSCON register), $\overline{\text{RSTIN}}$ pin is driven low and internal reset signal is asserted to reset the microcontroller in its default state. Note that after all reset sequence, bit BDRSTEN is cleared. After the reset sequence has been completed, the $\overline{\text{RSTIN}}$ input is sampled. When the reset input signal is active at that time the internal reset condition is prolonged until $\overline{\text{RSTIN}}$ becomes inactive.

Software reset: The reset sequence can be triggered at any time by the protected instruction SRST (software reset). This instruction can be executed deliberately within a program, e.g. to leave bootstrap loader mode, or on a hardware trap that reveals a system failure. As for a synchronous hardware reset, if bit BDRSTEN was previously set by software (bit 3 in SYSCON register), the reset sequence lasts 1024 TCL (512 CPU clock cycles), and drives the $\overline{\text{RSTIN}}$ pin low.

Watchdog timer reset: When the watchdog timer is not disabled during the initialization or serviced regularly during program execution it will overflow and trigger the reset sequence. Unlike hardware and software resets, the watchdog reset completes a running external bus cycle if this bus cycle does not use $\overline{\text{READY}}$, or if $\overline{\text{READY}}$ is sampled active (low) after the programmed waitstates. When $\overline{\text{READY}}$ is sampled inactive (high) after the programmed waitstates the running external bus cycle is aborted. Then the internal reset sequence is started. The watchdog reset cannot occur while the ST10R272L is in bootstrap loader mode.

Bidirectional reset: The bidirectional reset is activated by setting bit BDRSTEN (bit 3 in SYSCON register). This reset makes the watchdog timer reset and software reset externally visible. It is active for the duration of an internal reset sequences caused by a watchdog timer reset and software reset. Therefore, the bidirectional reset transforms an internal watchdog timer reset or software reset into an external hardware reset with a minimum duration of 1024 TCL.

Name	Physical Address	8-Bit Address	Description	Reset Value
IDX1 b	FF0Ah	85h	MAC Unit Address Pointer 1	0000h
MAH	FE5Eh	2Fh	MAC Unit Accumulator - High Word	0000h
MAL	FE5Ch	2Eh	MAC Unit Accumulator - Low Word	0000h
MCW	FFDCh	EEh	MAC Unit Control Word	0000h
MDC b	FF0Eh	87h	CPU Multiply Divide Control Register	0000h
MDH	FE0Ch	06h	CPU Multiply Divide Register – High Word	0000h
MDL	FE0Eh	07h	CPU Multiply Divide Register – Low Word	0000h
MRW b	FFDAh	EDh	MAC Unit Repeat Word	0000h
MSW b	FFDEh	EFh	MAC Unit Status Word	0200h
ODP2 b	F1C2h E	E1h	Port 2 Open Drain Control Register	-0--h
ODP3 b	F1C6h E	E3h	Port 3 Open Drain Control Register	0000h
ODP6 b	F1CEh E	E7h	Port 6 Open Drain Control Register	00h
ODP7 b	F1D2h E	E9h	Port 7 Open Drain Control Register	-0h
ONES	FF1Eh	8Fh	Constant Value 1’s Register (read only)	FFFFh
P0L b	FF00h	80h	Port 0 Low Register (Lower half of PORT0)	00h
P0H b	FF02h	81h	Port 0 High Register (Upper half of PORT0)	00h
P1L b	FF04h	82h	Port 1 Low Register (Lower half of PORT1)	00h
P1H b	FF06h	83h	Port 1 High Register (Upper half of PORT1)	00h
P2 b	FFC0h	E0h	Port 2 Register (4 bits)	-0--h
P3 b	FFC4h	E2h	Port 3 Register	0000h
P4 b	FFC8h	E4h	Port 4 Register (8 bits)	00h
P5 b	FFA2h	D1h	Port 5 Register (read only)	XXXXh
P6 b	FFCCh	E6h	Port 6 Register (8 bits)	00h
P7 b	FFD0h	E8h	Port 7Register (4 bits)	-0h
PECC0	FEC0h	60h	PEC Channel 0 Control Register	0000h
PECC1	FEC2h	61h	PEC Channel 1 Control Register	0000h

Table 13 Special functional registers

Name	Physical Address	8-Bit Address	Description	Reset Value
SP	FE12h	09h	CPU System Stack Pointer Register	FC00h
SSPCON0	EF00h X	---	SSP Control Register 0	0000h
SSPCON1	EF02h X	---	SSP Control Register 1	0000h
SSPRTB	EF04h X	---	SSP Receive/Transmit Buffer	XXXXh
SSPTBH	EF06h X	---	SSP Transmit Buffer High	XXXXh
STKOV	FE14h	0Ah	CPU Stack Overflow Pointer Register	FA00h
STKUN	FE16h	0Bh	CPU Stack Underflow Pointer Register	FC00h
SYSCON b	FF12h	89h	CPU System Configuration Register	0xx0h[1)]
T2	FE40h	20h	GPT1 Timer 2 Register	0000h
T2CON b	FF40h	A0h	GPT1 Timer 2 Control Register	0000h
T2IC b	FF60h	B0h	GPT1 Timer 2 Interrupt Control Register	0000h
T3	FE42h	21h	GPT1 Timer 3 Register	0000h
T3CON b	FF42h	A1h	GPT1 Timer 3 Control Register	0000h
T3IC b	FF62h	B1h	GPT1 Timer 3 Interrupt Control Register	0000h
T4	FE44h	22h	GPT1 Timer 4 Register	0000h
T4CON b	FF44h	A2h	GPT1 Timer 4 Control Register	0000h
T4IC b	FF64h	B2h	GPT1 Timer 4 Interrupt Control Register	0000h
T5	FE46h	23h	GPT2 Timer 5 Register	0000h
T5CON b	FF46h	A3h	GPT2 Timer 5 Control Register	0000h
T5IC b	FF66h	B3h	GPT2 Timer 5 Interrupt Control Register	0000h
T6	FE48h	24h	GPT2 Timer 6 Register	0000h
T6CON b	FF48h	A4h	GPT2 Timer 6 Control Register	0000h
T6IC b	FF68h	B4h	GPT2 Timer 6 Interrupt Control Register	0000h
TFR b	FFACh	D6h	Trap Flag Register	0000h
WDT	FEAEh	57h	Watchdog Timer Register (read only)	0000h
WDTCON	FFAEh	D7h	Watchdog Timer Control Register	000xh[2)]

Table 13 Special functional registers

Name	Physical Address	8-Bit Address	Description	Reset Value
XP1IC b	F18Eh E	C7h	SSP Interrupt Control Register	0000h
XP3IC b	F19Eh E	CFh	PLL unlock Interrupt Control Register	0000h
ZEROS b	FF1Ch	8Eh	Constant Value 0's Register (read only)	0000h

Table 13 Special functional registers

Note 1. The system configuration is selected during reset.

Note 2. Bit WDTR indicates a watchdog timer triggered reset.

Remarks on 5 volt tolerant (5T) and 5 volt fail-safe (5S) pins

The 5V tolerant input and output pins can sustain an absolute maximum external voltage of 5.5V.

However, signals on unterminated bus lines might have overshoot above 5.5V, presenting latchup and hot carrier risks. While these risks are under evaluation, observe the following security recommendations:

- Maximum peak voltage on 5V tolerant pin with respect to ground (V_{SS})= +6 V
- If the ringing of the external signal exceeds 6V, then clip the signal to the 5V supply.

Power supply failure condition

The power supply failure condition is a state where the chip is NOT supplied but is connected to active signal lines. There are several cases:

- 3.3V external lines on 3.3V (3T) pin on the non powered chip: .....NOT Acceptable
- 3.3V external lines on 5V tolerant (5T) pin on the non powered chip: ..... Acceptable

  The 5V tolerant buffer do not leak: external signals not altered. No reliability problem.
- 3.3V external lines on 5V fail-safe (5S) pin on the non powered chip: ..... Acceptable

  The 5V tolerant buffer do not leak: external signals not altered. No reliability problem.
- 5.5V external lines on 5V tolerant (5T) pin on the non powered chip: ..... Acceptable

  For VERY SHORT times only: the buffers do not leak (external signals not altered) but there is a fast degradation of the gate oxides in the buffers. The total maximum time under this stress condition is 2 days. This limits this configuration to short power-up/down sequences. For 10 year life time, the maximum duty factor is 1/1800 allowing e.g. a maximum stress duration of 48 seconds per day.
- 5.5V external lines on 5V fail-safe (5S) pin on the non powered chip: ..... Acceptable
- 6V transient signals on 5V tolerant (5T) pin on the non powered chip: ...NOT Acceptable
- 6V transient signals on 5V fail-safe (5S) pin on the non powered chip:..... Acceptable

16.3 AC Characteristics

Test conditions

- Input pulse levels: ..... 0 to +3.0 V
- Input rise and fall times (10%-90%): ..... 2.5 ns
- Input timing reference levels: ..... +1.5 V
- Output timing reference levels: ..... +1.5 V
- Output load: ..... see Figure 12

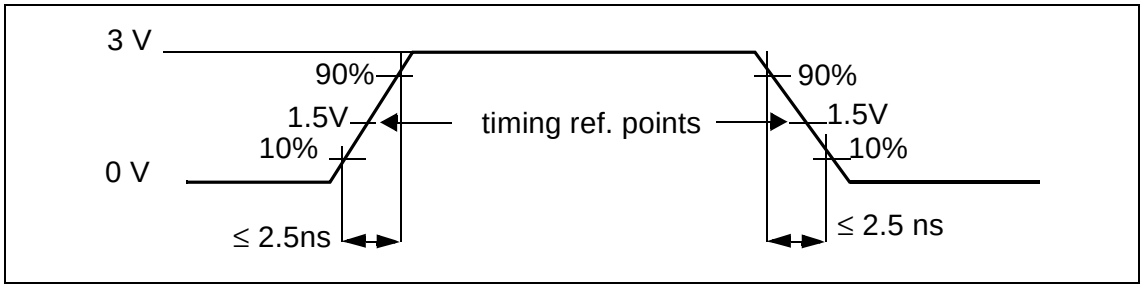

Figure 11 Input waveforms

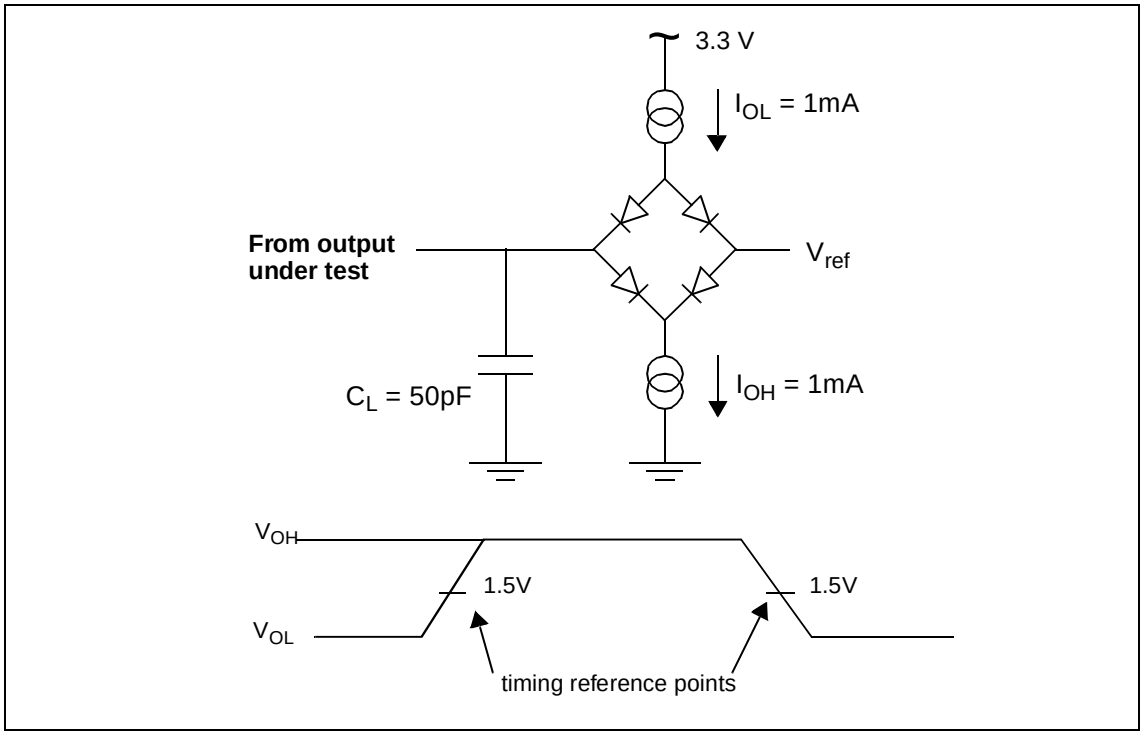

Figure 12 Output load circuit waveform

P0.15-13 (P0H.7-5)			CPU frequency $f_{CPU} = f_{XTAL} * F$	External clock input range 10-50MHz	Notes
1	0	0	$F_{XTAL} * 5$	2 to 10 MHz	
0	1	1	$F_{XTAL} * 1$	1 to 50 MHz	Direct drive 1)
0	1	0	$F_{XTAL} * 1.5$	6.66 to 33.33 MHz	
0	0	1	$F_{XTAL} / 2$	2 to 100 MHz	CPU clock via 2:1 prescaler
0	0	0	$F_{XTAL} * 2.5$	4 to 20 MHz	

Table 15 CPU clock generation mechanisms

1) The maximum depends on the duty cycle of the external clock signal. The maximum input frequency is 25 MHz when using an external crystal oscillator, but higher frequencies can be applied with an external clock source.

Prescaler operation

Set when pins P0.15-13 (P0H.7-5) equal '001' during reset, the CPU clock is derived from the internal oscillator (input clock signal) by a 2:1 prescaler.
The frequency of f_{CPU} is half the frequency of f_{XTAL} and the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the period of the input clock f_{XTAL}.

The timings listed in the AC characteristics that refer to TCLs therefore can be calculated using the period of f_{XTAL} for any TCL.

Note that if the bit OWDDIS in SYSCON register is cleared, the PLL runs on its free-running frequency and delivers the clock signal for the Oscillator Watchdog. If bit OWDDIS is set, then the PLL is switched off.

Direct drive

When pins P0.15-13 (P0H.7-5) equal '011' during reset, the on-chip phase locked loop is disabled and the CPU clock is driven from the internal oscillator with the input clock signal. The frequency of f_{CPU} directly follows the frequency of f_{XTAL} so the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the duty cycle of the input clock f_{XTAL}.

The TCL timing below must be calculated using the minimum possible TCL which can be calculated by the formula: $TCL_{min} = 1/f_{XTAL} \times DC_{min} (DC = \text{duty cycle})$

For two consecutive TCLs the deviation caused by the duty cycle of f_{XTAL} is compensated so the duration of 2TCL is always $1/f_{XTAL}$. Therefore, the minimum value TCL_{min} has to be used only once for timings that require an odd number of TCLs (1,3,...). Timings that require an even number of TCLs (2,4,...) may use the formula: $2TCL = 1/f_{XTAL}$.

16.3.3 Multiplexed Bus

V_{DD} = 3.3 V ± 0.3 V V_{SS} = 0 V T_A = -40 to +85 °C C_L = 50 pF

ALE cycle time = 6 TCL + $2t_A$ + t_C + t_F (60 ns at 50-MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 50 MHz		Variable CPU Clock 1/2TCL = 1 to 50 MHz		Unit
			min.	max.	min.	max.	
ALE high time	t_5	CC	7 + t_A	–	TCL - 3 + t_A	–	ns
Address (P1, P4), $\overline{BHE}$ setup to ALE	t_6	CC	3 + t_A	–	TCL - 7 + t_A	–	ns
Address (P0) setup to ALE	t_{6m}	CC	5 + t_A	–	TCL - 5 + t_A	–	ns
Address hold after ALE	t_7	CC	5 + t_A	–	TCL - 5 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_8	CC	5 + t_A	–	TCL - 5 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_9	CC	-5 + t_A	–	-5 + t_A	–	ns
Address float after $\overline{RD}$, (with RW-delay)[1)]	t_{10}	CC	–	5[1]	–	5[1]	ns
Address float after $\overline{RD}$, (no RW-delay)[1]	t_{11}	CC	–	15[1]	–	TCL + 5[1]	ns
$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	t_{12}	CC	13 + t_C	–	2TCL - 7+ t_C	–	ns
$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	t_{13}	CC	23 + t_C	–	3TCL - 7 + t_C	–	ns
$\overline{RD}$ to valid data in (with RW-delay)	t_{14}	SR	–	5 + t_C	–	2TCL - 15 + t_C	ns
$\overline{RD}$ to valid data in (no RW-delay)	t_{15}	SR	–	15 + t_C	–	3TCL - 15 + t_C	ns
ALE low to valid data in	t_{16}	SR	–	15 + t_A + t_C	–	3TCL - 15 + t_A + t_C	ns
Address to valid data in	t_{17}	SR	–	20 + $2t_A$ + t_C	–	4TCL - 20 + $2t_A$ + t_C	ns

Table 17 Multiplexed bus

Parameter	Symbol		Max CPU Clock 50MHz		Variable CPU Clock 1/2TCL = 1 to 50 MHz		Unit
			min.	max.	min.	max.	
Data hold after $\overline{WR}$	t_{24}	CC	5 + t_F	–	TCL - 5 + t_F	–	ns
ALE rising edge after $\overline{RD}$, $\overline{WR}$	t_{26}	CC	-5 + t_F	–	-5 + t_F	–	ns
Address hold after $\overline{RD}$, $\overline{WR}$	t_{28}	CC	0 (no t_F) -9+t_F ($t_{F>0}$)	–	0 (no t_F) -9 + t_F ($t_{F>0}$)	–	ns
Address hold after $\overline{WRH}$	t_{28h}	CC	-1 (no t_F) -8 +t_F ($t_{F>0}$)	–	-1 (no t_F) -8 + t_F ($t_{F>0}$)	–	ns
Latched $\overline{CS}$ setup to ALE	t_{38}	CC	-7 + t_A	3 + t_A	-7 + t_A	3 + t_A	ns
Unlatched $\overline{CS}$ setup to ALE	t_{38u}	CC	3 + t_A	–	TCL - 7 + t_A	–	ns
Latched $\overline{CS}$ low to Valid Data In	t_{39}	SR	–	13 + t_C + 2t_A	–	3TCL - 17 + t_C + 2t_A	ns
Unlatched $\overline{CS}$ low to Valid Data In	t_{39u}	SR	–	23 + t_C + 2t_A	–	4TCL - 17 + t_C + 2t_A	ns
Latched $\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$	t_{41}	CC	3 + t_F	–	TCL - 7 + t_F	–	ns
Unlatched $\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$	t_{41u}	CC	0 (no t_F) -7 +t_F ($t_{F>0}$)	–	0 (no t_F) -7 + t_F ($t_{F>0}$)	–	ns
Address setup to $\overline{RdCs}$, $\overline{WrCs}$ (with RW-delay)	t_{82}	CC	13 + 2t_A	–	2TCL - 7 + 2t_A	–	ns
Address setup to $\overline{RdCs}$, $\overline{WrCs}$ (no RW-delay)	t_{83}	CC	3 + 2t_A	–	TCL - 7 + 2t_A	–	ns
$\overline{RdCS}$ to Valid Data In (with RW-delay)	t_{46}	SR	–	3 + t_C	–	2TCL - 17 + t_C	ns
$\overline{RdCS}$ to Valid Data In (no RW-delay)	t_{47}	SR	–	13 + t_C	–	3TCL - 17 + t_C	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (with RW-delay)	t_{48}	CC	11 + t_C	–	2TCL - 9 + t_C	–	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (no RW-delay)	t_{49}	CC	21 + t_C	–	3TCL - 9 + t_C	–	ns
Data valid to $\overline{WrCS}$	t_{50}	CC	13 + t_C	–	2TCL - 7 + t_C	–	ns

Table 18 Demultiplexed bus

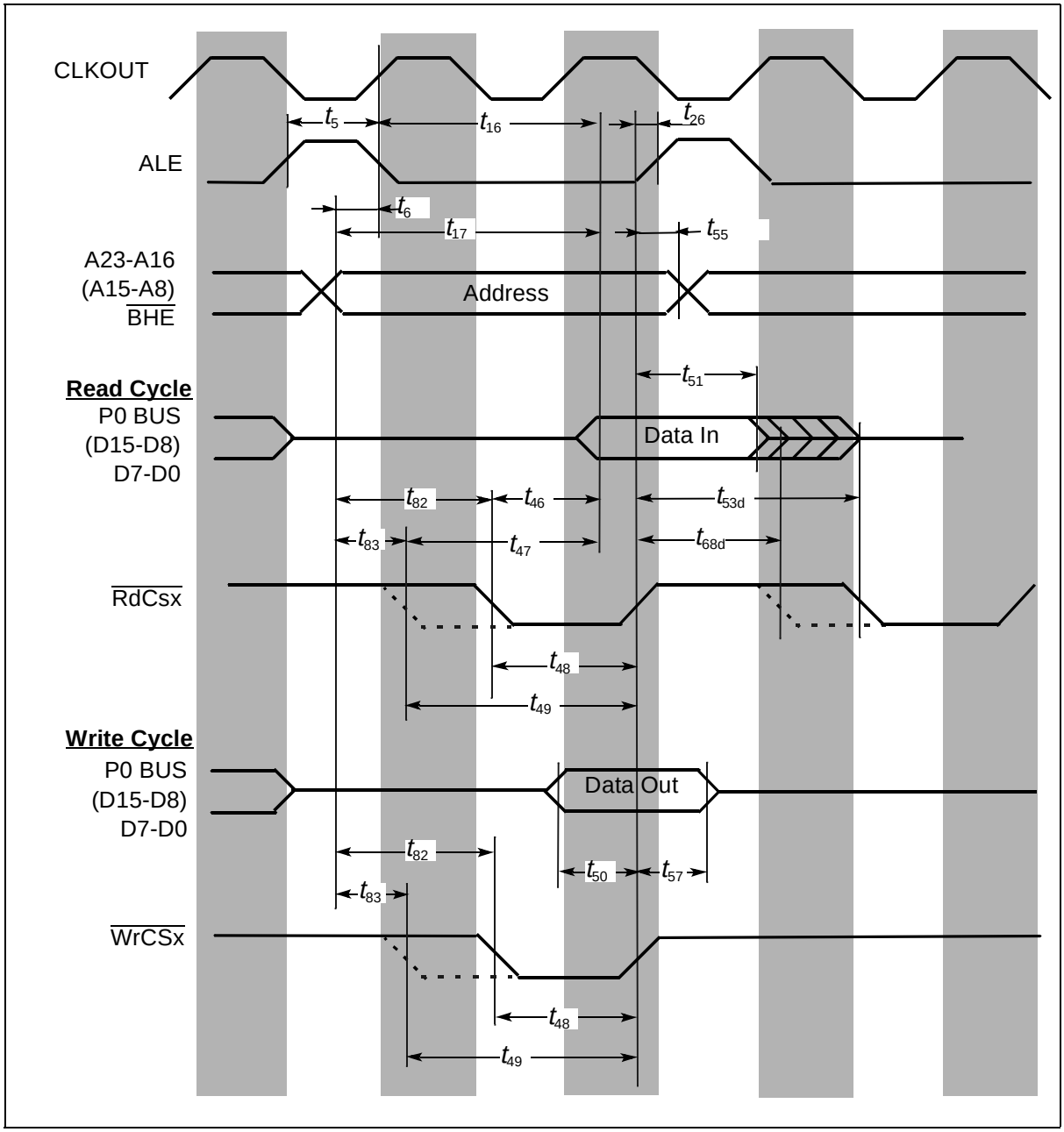

Figure 22 External memory cycle:
demultiplexed bus, with/without read/write delay, normal ALE, read/write chip select

6 Multiplexed bus modes have a MUX waitstate added after a bus cycle, and an additional MTTC waitstate may be inserted here. For a multiplexed bus with MTTC waitstate this delay is 2 CLKOUT cycles, for a demultiplexed bus without MTTC waitstate this delay is zero.

7 The next external bus cycle may start here.

16.3.6 External Bus Arbitration

V_{DD} = 3.3 V ± 0.3 V V_{SS} = 0 V T_A = -40 to +85 °C C_L = 50 pF

Parameter	Symbol		Max. CPU Clock = 50 MHz		Variable CPU Clock 1/2TCL = 1 to 50 MHz		Unit
			min.	max.	min.	max.	
$\overline{HOLD}$ input setup time to CLKOUT	t_{61}	SR	15	–	15	–	ns
CLKOUT to $\overline{HLDA}$ high or $\overline{BREQ}$ low delay	t_{62}	CC	–	10	–	10	ns
CLKOUT to $\overline{HLDA}$ low or $\overline{BREQ}$ high delay	t_{63}	CC	–	10	–	10	ns
$\overline{CSx}$ release	t_{64}	CC	–	15	–	15	ns
$\overline{CSx}$ drive	t_{65}	CC	-3	15	-3	15	ns
Other signals release	t_{66}	CC	–	15	–	15	ns
Other signals drive	t_{67}	CC	-3	15	-3	15	ns

Table 20 External bus arbitration

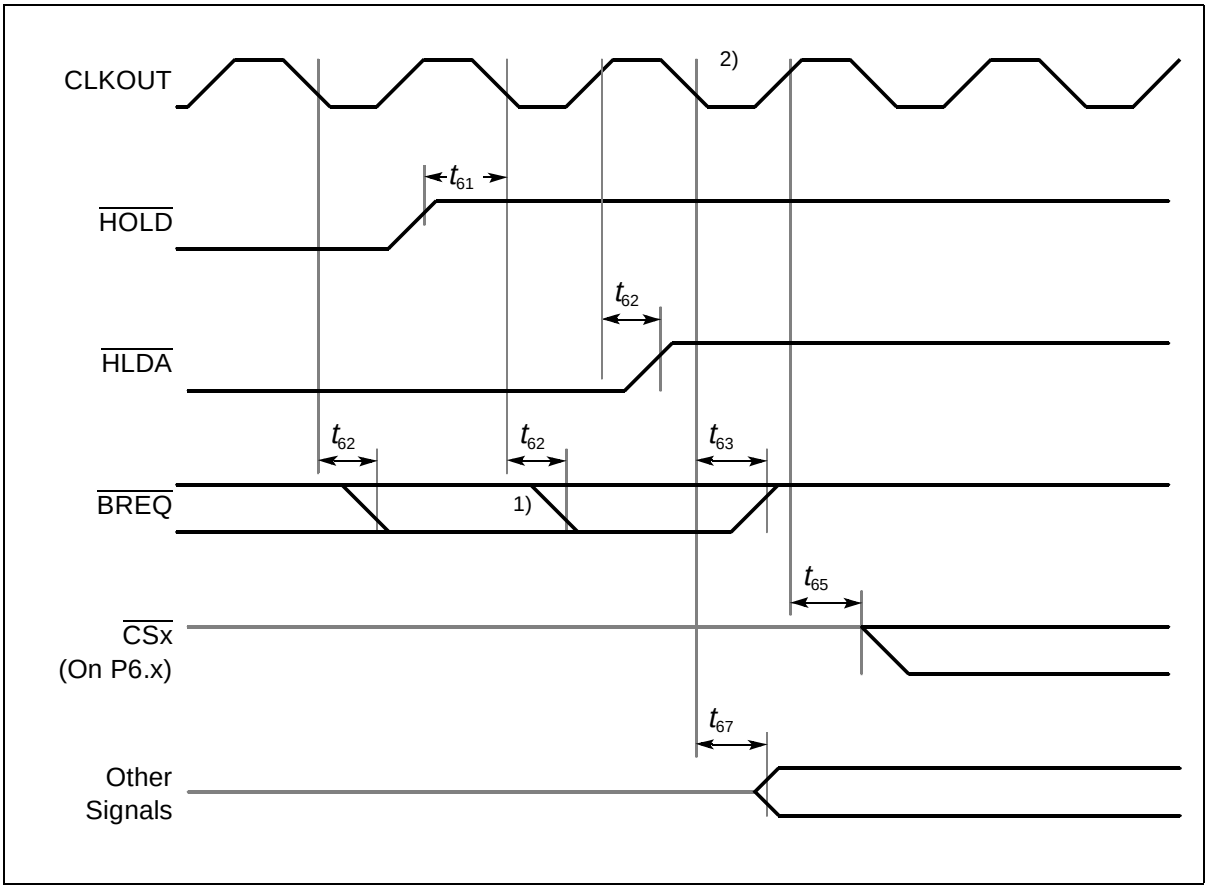

Figure 26 External bus arbitration, (regaining the bus)

1 This is the last chance for BREQ to trigger the regain-sequence indicated. Even if BREQ is activated earlier, the regain-sequence is initiated by HOLD going high. Please note that HOLD may also be de-activated without the ST10R272L requesting the bus.

2 The next ST10R272L driven bus cycle may start here.

.

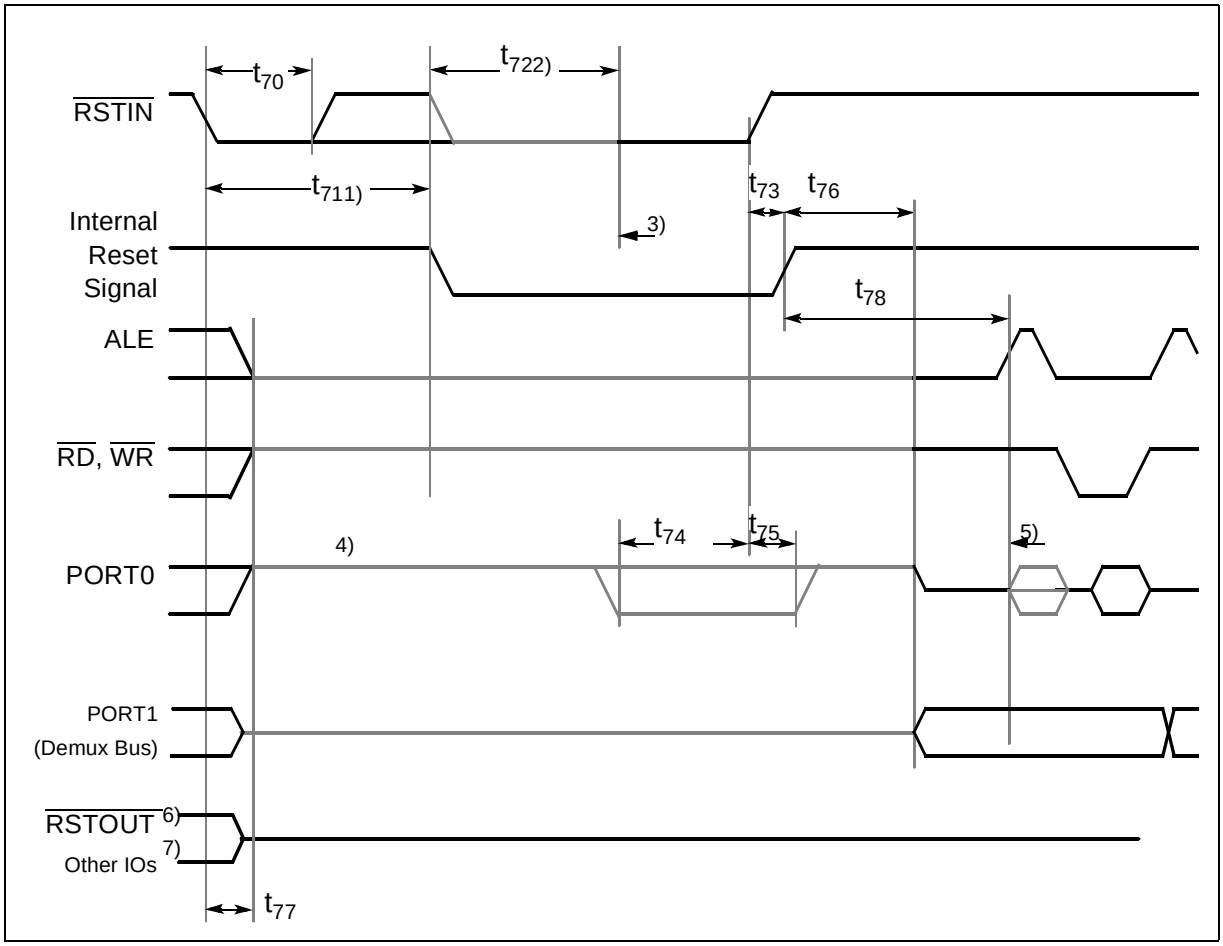

Figure 28 External synchronous hardware reset (warm reset): Vpp high

1 The pending internal hold states are cancelled and the current internal access cycle (if any) is completed.

2 $\overline{\text{RSTIN}}$ pulled low by internal device during internal reset sequence.

3 The reset condition may ends here if $\overline{\text{RSTIN}}$ pin is sampled high after t_{72}.

4 Internal pullup devices are active on the PORT0 lines. Their input level is high if the respective pin is left open, or is low if the respective pin is connected to an external pull-down device by resistive high (pullup) after t_{64}.

5 The ST10R272L starts execution here at address 00’0000h.

6 $\overline{\text{RSTOUT}}$ stays active until execution of the EINIT (End of Initialization) instruction.

7 Activation of the IO pins is controlled by software.