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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST10
Core Size	16-Bit
Speed	50MHz
Connectivity	EBI/EMI, SSP, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	77
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st10r272lt6

Symbol	Pin Number (TQFP)	Input (I) Output (O)	Kind[1)]	Function		
P5.10	98-100	I	5S	6-bit input-only port with Schmitt-Trigger characteristics. Port 5 pins also serve as timer inputs:		
–P5.15	1- 3	I	5S			
	98	I	5S	P5.10	T6EUD	GPT2 Timer T6 Ext.Up/Down Ctrl.Input
	99	I	5S	P5.11	T5EUD	GPT2 Timer T5 Ext.Up/Down Ctrl.Input
	100	I	5S	P5.12	T6IN	GPT2 Timer T6 Count Input
	1	I	5S	P5.13	T5IN	GPT2 Timer T5 Count Input
	2	I	5S	P5.14	T4EUD	GPT1 Timer T4 Ext.Up/Down Ctrl.Input
	3	I	5S	P5.15	T2EUD	GPT1 Timer T2 Ext.Up/Down Ctrl.Input
XTAL1	5	I	3T	XTAL1:	Input to the oscillator amplifier and internal clock generator	
XTAL2	6	O	3T	XTAL2:	Output of the oscillator amplifier circuit. To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Observe minimum and maximum high/low and rise/fall times specified in the AC Characteristics.	

Table 1 Pin definitions

Symbol	Pin Number (TQFP)	Input (I) Output (O)	Kind[1)]	Function		
P3.0 – P3.13	8-21	I/O	5T	A 15-bit (P3.14 is missing) bidirectional I/O port. Port 3 is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 3 outputs can be configured as push/ pull or open drain drivers. The following pins have alternate functions:		
P3.15	22	I/O	5T			
	9	O	5T	P3.1	T6OUT	GPT2 Timer T6 toggle latch output
	10	I	5T	P3.2	CAPIN	GPT2 Register CAPREL capture input
	11	O	5T	P3.3	T3OUT	GPT1 Timer T3 toggle latch output
	12	I	5T	P3.4	T3EUD	GPT1 Timer T3 ext.up/down ctrl.input
	13	I	5T	P3.5	T4IN	GPT1 Timer T4 input for count/gate/ reload/capture
	14	I	5T	P3.6	T3IN	GPT1 Timer T3 count/gate input
	15	I	5T	P3.7	T2IN	GPT1 Timer T2 input for count/gate/ reload/capture
	18	O	5T	P3.10	TxD0	ASC0 clock/data output (asyn./syn.)
	19	I/O	5T	P3.11	RxD0	ASC0 data input (asyn.) or I/O (syn.)
	20	O	5T	P3.12	$\overline{BHE}$	Ext. Memory High Byte Enable Signal
		O	5T		$\overline{WRH}$	Ext. Memory High Byte Write Strobe
	22	O	5T	P3.15	CLKOUT	System clock output (=CPU clock)

Table 1 Pin definitions

Symbol	Pin Number (TQFP)	Input (I) Output (O)	Kind[1)]	Function		
$\overline{\text{RSTIN}}$	79	I	5T	Reset Input with Schmitt-Trigger characteristics. Resets the device when a low level is applied for a specified duration while the oscillator is running. An internal pullup resistor enables power-on reset using only a capacitor connected to V_{SS}. With a bonding option, the $\overline{\text{RSTIN}}$ pin can also be pulled-down for 512 internal clock cycles for hardware, software or watchdog timer triggered resets		
$\overline{\text{RSTOUT}}$	80	O	5T	Internal Reset Indication Output. This pin is set to a low level when the part is executes hardware-, software- or watchdog timer reset. $\overline{\text{RSTOUT}}$ remains low until the EINIT (end of initialization) instruction is executed.		
$\overline{\text{NMI}}$	81	I	5S	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. If it is not used, $\overline{\text{NMI}}$ should be pulled high externally.		
P6.0-P6.7	82-89	I/O	5T	An 8-bit bidirectional I/O port. Port 6 is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 6 outputs can be configured as push/pull or open drain drivers. The following Port 6 pins have alternate functions:		
	82	O	5T	P6.0	$\overline{\text{CS0}}$	Chip Select 0 Output
	...	...	...	...	...	...
	86	O	5T	P6.4	$\overline{\text{CS4}}$	Chip Select 4 Output
	87	I	5T	P6.5	$\overline{\text{HOLD}}$	External Master Hold Request Input (Master mode: O, Slave mode: I)
	88	I/O	5T	P6.6	$\overline{\text{HLDA}}$	Hold Acknowledge Output
	89	O	5T	P6.7	$\overline{\text{BREQ}}$	Bus Request Output

Table 1 Pin definitions

5.1 MAC Features

Enhanced addressing capabilities

- Double indirect addressing mode with pointer post-modification.
- Parallel Data Move allows one operand move during Multiply-Accumulate instructions without penalty.
- CoSTORE instruction (for fast access to the MAC SFRs) and CoMOV (for fast memory to memory table transfer).

General

- Two-cycle execution for all MAC operations.
- 16 x 16 signed/unsigned parallel multiplier.
- 40-bit signed arithmetic unit with automatic saturation mode.
- 40-bit accumulator.
- 8-bit left/right shifter.
- Scaler (one-bit left shifter)
- Data limiter
- Full instruction set with multiply and multiply-accumulate, 32-bit signed arithmetic and compare instructions.
- Three 16-bit status and control registers: MSW: MAC Status Word, MCW: MAC Control Word, MRW: MAC Repeat Word.

Program control

- Repeat Unit allows some MAC co-processor instructions to be repeated up to 8192 times. Repeated instructions may be interrupted.
- MAC interrupt (Class B Trap) on MAC condition flags.

The following table shows the various combinations of pointer post-modification for each of these 2 new addressing modes. In this document the symbols "[$Rw_n\otimes$]" and "[$IDX_i\otimes$]" refer to these addressing modes.

Symbol	Mnemonic	Address Pointer Operation
"[$IDX_i\otimes$]" stands for	[IDX_i]	(IDX_i) ← (IDX_i) (no-op)
	[IDX_i+]	(IDX_i) ← (IDX_i) +2 (i=0,1)
	[IDX_i -]	(IDX_i) ← (IDX_i) -2 (i=0,1)
	[$IDX_i + QX_j$]	(IDX_i) ← (IDX_i) + (QX_j) (i, j =0,1)
	[IDX_i - QX_j]	(IDX_i) ← (IDX_i) - (QX_j) (i, j =0,1)
"[$Rw_n\otimes$]" stands for	[Rwn]	(Rwn) ← (Rwn) (no-op)
	[Rwn+]	(Rwn) ← (Rwn) +2 (n=0-15)
	[Rwn-]	(Rwn) ← (Rwn) -2 (k=0-15)
	[Rwn+QR_j]	(Rwn) ← (Rwn) + (QR_j) (n=0-15;j =0,1)
	[Rwn - QR_j]	(Rwn) ← (Rwn) - (QR_j) (n=0-15; j =0,1)

Table 2 Pointer post-modification combinations for IDXi and Rwn

For the CoMACM class of instruction, Parallel Data Move mechanism is implemented. This class of instruction is only available with double indirect addressing mode. Parallel Data Move allows the operand pointed by IDX_i to be moved to a new location in parallel with the MAC operation. The write-back address of Parallel Data Move is calculated depending on the post-modification of IDX_i. It is obtained by the reverse operation than the one used to calculate the new value of IDX_i. The following table shows these rules.

Instruction	Writeback Address
CoMACM [IDX_i+],...	<IDX_i-2>
CoMACM [IDX_i-],...	<IDX_i+2>
CoMACM [IDX_i+QX_j],...	<IDX_i-QX_j>
CoMACM [IDX_i-QX_j],...	<IDX_i+QX_j>

Table 3 Parallel data move addressing

Number representation & rounding

The MAC supports the two's-complement representation of binary numbers. In this format, the sign bit is the MSB of the binary word. This is set to zero for positive numbers and set to one for negative numbers. Unsigned numbers are supported only by multiply/multiply-accumulate instructions which specifies whether each operand is signed or unsigned.

In two's complement fractional format, the N-bit operand is represented using the 1.[N-1] format (1 signed bit, N-1 fractional bits). Such a format can represent numbers between -1 and $+1-2^{-[N-1]}$. This format is supported when MP of MCW is set.

The MAC implements 'two's complement rounding'. With this rounding type, one is added to the bit to the right of the rounding point (bit 15 of MAL), before truncation (MAL is cleared).

6 INTERRUPT AND TRAP FUNCTIONS

The architecture of the ST10R272L supports several mechanisms for fast and flexible response to the service requests that can be generated from various sources, internal or external to the microcontroller. Any of these interrupt requests can be programmed to be serviced, either by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In a standard interrupt service, program execution is suspended and a branch to the interrupt service routine is performed. For a PEC service, just one cycle is 'stolen' from the current CPU activity. A PEC service is a single, byte or word data transfer between any two memory locations, with an additional increment of either the PEC source or the destination pointer. An individual PEC transfer counter is decremented for each PEC service, except in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source-related vector location. PEC services are very well suited, for example, to the transmission or reception of blocks of data. The ST10R272L has 8 PEC channels, each of which offers fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield, exists for each of the possible interrupt sources. Via its related register, each source can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher priority service request. For standard interrupt processing, each of the possible interrupt sources has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs, feature programmable edge detection (rising edge, falling edge or both edges).

Software interrupts are supported by means of the 'TRAP' instruction in combination with an individual trap (interrupt) number.

of external memory space, the address space can be restricted to 1 MByte, 256 KByte or to 64 KByte.

9 PWM MODULE

A 1-channel Pulse Width Modulation (PWM) Module operates on channel 3. The pulse width modulation module can generate up to four PWM output signals using edge-aligned or centre-aligned PWM. In addition, the PWM module can generate PWM burst signals and single shot outputs. The table below shows the PWM frequencies for different resolutions. The level of the output signals is selectable and the PWM module can generate interrupt requests.

Mode 0 edge aligned	**Resolution**	**8-bit**	**10-bit**	**12-bit**	**14-bit**	**16-bit**
CPU clock/1	20ns	195.3 KHz	48.83KHz	12.21KHz	3.052KHz	762.9Hz
CPU clock/64	1.28ns	3.052KHz	762.9Hz	190.7Hz	47.68Hz	11.92Hz
Mode 1 center aligned	**Resolution**	**8-bit**	**10-bit**	**12-bit**	**14-bit**	**16-bit**
CPU clock/1	20ns	97.66KHz	24.41KHz	6.104KHz	1.525KHz	381.5Hz
CPU clock/64	1.28ns	1.525Hz	381.5 Hz	95.37Hz	23.84Hz	0Hz

Table 7 PWM unit frequencies and resolution at 50MHz CPU clock

10 GENERAL PURPOSE TIMERS

The GPTs are flexible multifunctional timer/counters used for time-related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation or pulse multiplication. The GPT unit contains five 16-bit timers, organized in two separate modules, GPT1 and GPT2. Each timer in each module may operate independently in a number of different modes, or may be concatenated with another timer of the same module.

10.1 GPT1

Each of the three timers T2, T3, T4 of the GPT1 module can be configured individually for one of four basic modes of operation: **timer**, **gated timer**, **counter mode and incremental interface mode**. In timer mode, the input clock for a timer is derived from the CPU clock, divided by a programmable prescaler. In counter mode, the timer is clocked in reference to external events. Pulse width or duty cycle measurement is supported in gated timer mode where the operation of a timer is controlled by the ‘gate’ level on an external input pin. For these purposes, each timer has one associated port pin (TxIN) which serves as gate or clock input. Table 8 GPT1 timer input frequencies, resolution and periods lists the timer input frequencies, resolution and periods for each pre-scaler option at 50MHz CPU clock. This also applies to the Gated Timer Mode of T3 and to the auxiliary timers T2 and T4 in Timer and Gated Timer Mode

The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD).

In Incremental Interface Mode, the GPT1 timers (T2, T3, T4) can be directly connected to the incremental position sensor signals A and B by their respective inputs TxIN and TxEUD. Direction and count signals are internally derived from these two input signals so that the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has output toggle latches (TxOTL) which changes state on each timer over-flow/ underflow. The state of this latch may be output on port pins (TxOUT) e. g. for time out monitoring of external hardware components, or may be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as capture or reload registers, timers T2 and T4 are stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at their associated input pins (TxIN). Timer T3 is reloaded with the contents of T2 or T4 triggered either by an external signal or by a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be constantly generated without software intervention.

F_{CPU}=50MHz	Timer input selection							
	000b	**001b**	**010b**	**011b**	**100b**	**101b**	**110b**	**111b**
Prescaler Factor	8	16	32	64	128	256	512	1024
Input Frequency	6.25 MHz	3.125 MHz	1.5625 MHz	781 KHz	391 KHz	195 KHz	97.5 KHz	48.83 KHz
Resolution	160ns	320ns	640ns	1.28 us	2.56 us	5.12 us	10.24 us	20.48 us
Period	10.49ms	20.97ms	41.94ms	83.88ms	168ms	336ms	672ms	1.342s

Table 8 GPT1 timer input frequencies, resolution and periods

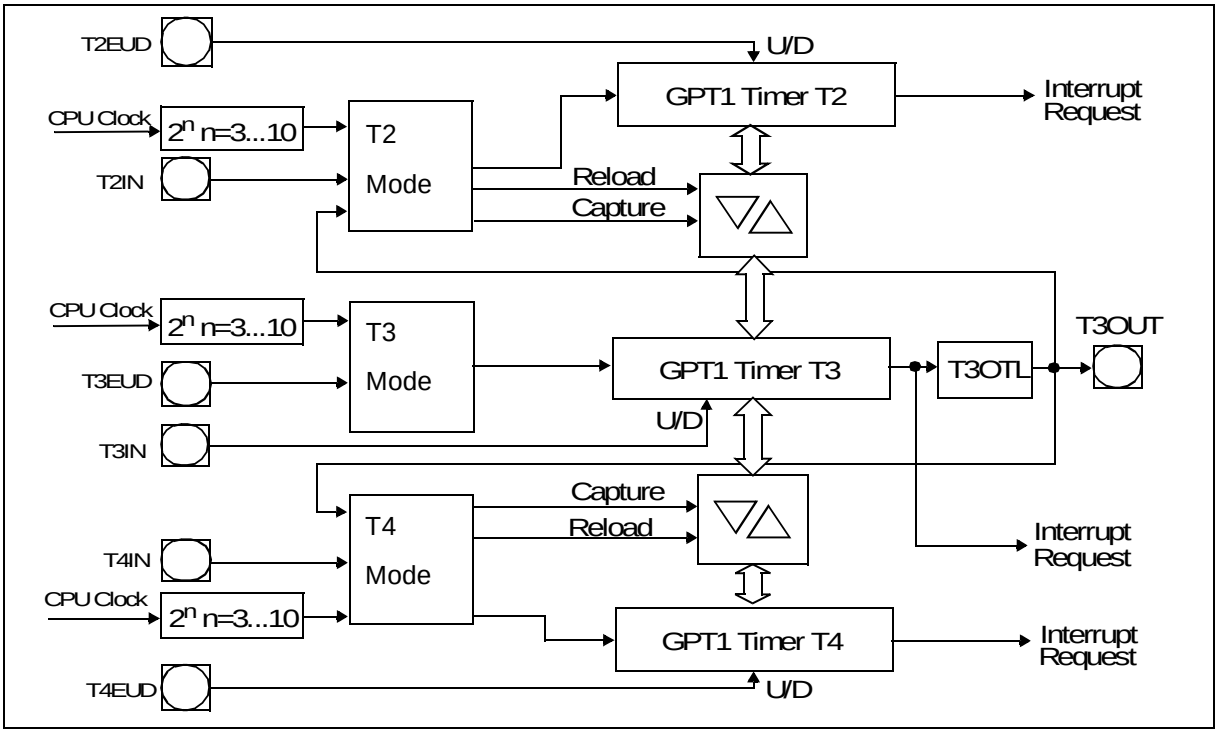

Figure 8 GPT1 block diagram

16 ELECTRICAL CHARACTERISTICS

16.1 Absolute Maximum Ratings

- Ambient temperature under bias (T_A): ..... -40 to +85 °C
- Storage temperature (T_{ST}): ..... – 65 to +150 °C
- Voltage on V_{DD} pins with respect to ground (V_{SS}): ..... – 0.5 to +4.0 V
- Voltage on any pin with respect to ground (V_{SS}): ..... –0.5 to V_{DD} +0.5 V
- Voltage on any 5V tolerant pin with respect to ground (V_{SS}): .....–0.5 to 5.5 V
- Voltage on any 5V fail-safe pin with respect to ground (V_{SS}): .....–0.5 to 5.5 V
- Input current on any pin during overload condition: ..... –10 to +10 mA
- Absolute sum of all input currents during overload condition: .....|100 mA|
- Power dissipation:.....1.0 W

Note *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions (V_{IN}>V_{DD} or V_{IN}<V_{SS}) the voltage on pins with respect to ground (V_{SS}) must not exceed the values defined by the Absolute Maximum Ratings.*

The parameters listed in this section represent both the ST10R272L controller characteristics and the system requirements. To aid parameters interpretation in design evaluation, the a symbol column is marked:

CC for **C**ontroller **C**haracteristics:	The ST10R272L logic provides signals with the respective timing characteristics.
SR for System Requirement:	The external system must provide signals with the respective timing characteristics to the ST10R272L.

16.3 AC Characteristics

Test conditions

- Input pulse levels: ..... 0 to +3.0 V
- Input rise and fall times (10%-90%): ..... 2.5 ns
- Input timing reference levels: ..... +1.5 V
- Output timing reference levels: ..... +1.5 V
- Output load: ..... see Figure 12

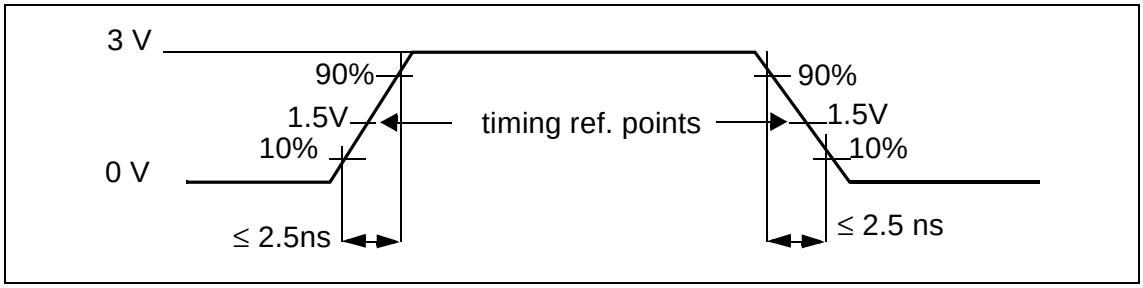

Figure 11 Input waveforms

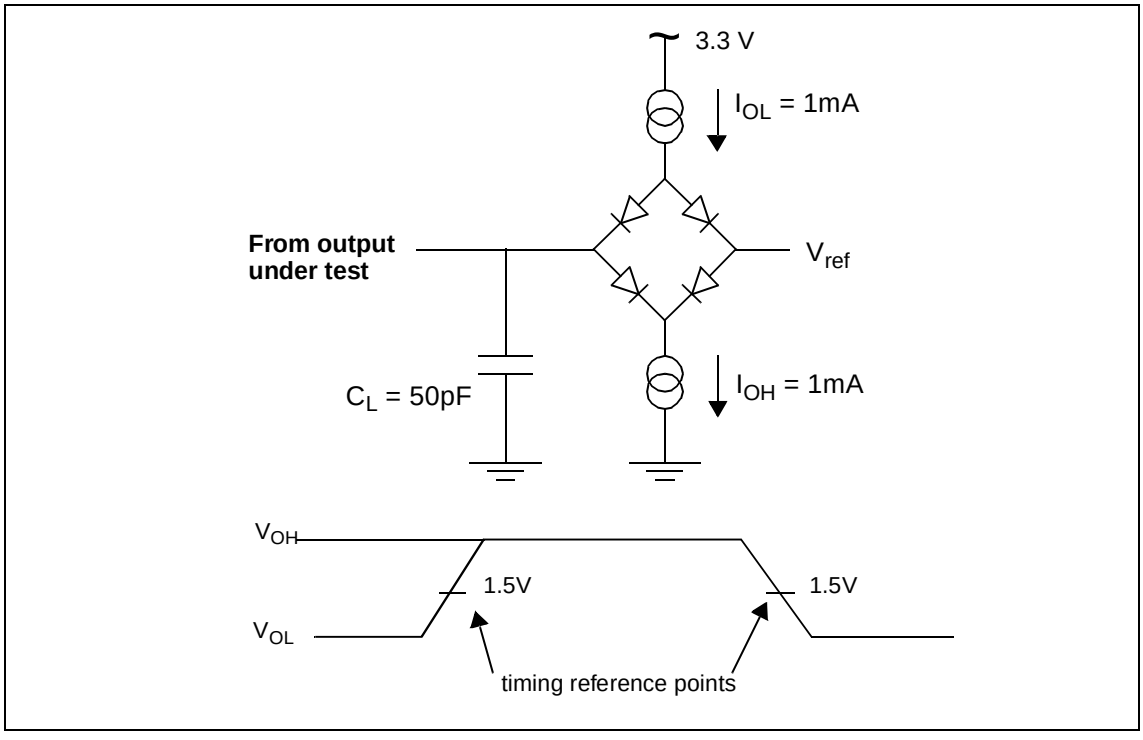

Figure 12 Output load circuit waveform

16.3.1 CPU Clock Generation Mechanisms

ST10R272L internal operation is controlled by the CPU clock f_{CPU}. Both edges of the CPU clock can trigger internal (e.g. pipeline) or external (e.g. bus cycles) operations. The external timing (AC Characteristics) specification therefore depends on the time between two consecutive edges of the CPU clock, called “TCL” (see figure below).

The CPU clock signal can be generated by different mechanisms. The duration of TCLs and their variation (and also the external timing) depends on the f_{CPU} generation mechanism. This must be considered when calculating ST10R272L timing.

The CPU clock generation mechanism is set during reset by the logic levels on pins P0.15-13 (P0H.7-5).

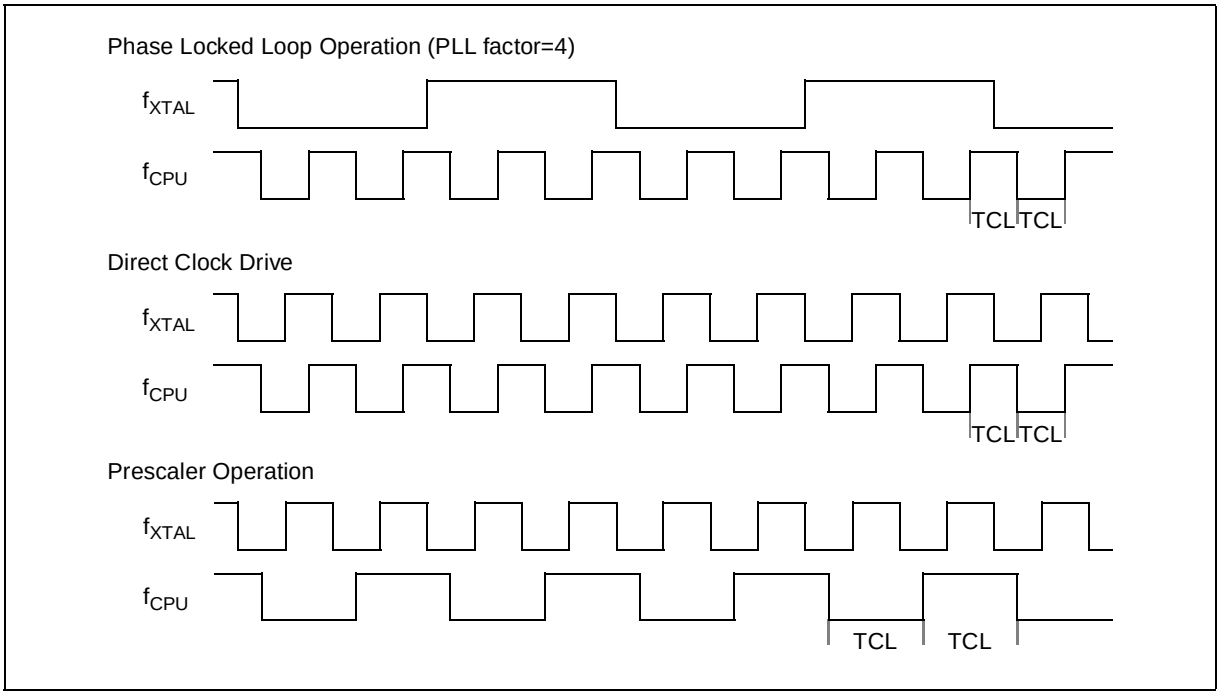

Figure 14 CPU clock generation mechanisms

P0.15-13 (P0H.7-5)			CPU frequency $f_{CPU} = f_{XTAL} * F$	External clock input range 10-50MHz	Notes
1	1	1	$F_{XTAL} * 4$	2.5 to 12.5 MHz	Default configuration
1	1	0	$F_{XTAL} * 3$	3.33 to 16.66 MHz	
1	0	1	$F_{XTAL} * 2$	5 to 25 MHz	

Table 15 CPU clock generation mechanisms

where ***N*** = number of consecutive TCLs and $1 \leq N \leq 40$. So for a period of 3 TCLs (i.e. $N = 3$):

$$D_3 = 4 - 3/15$$
$$= 3{,}8\%$$

and

$$3TCL_{min} = 3TCL_{NOM} \times (1 - 3{,}8/100)$$
$$= 3TCL_{NOM} \times 0{,}962 (36.07\text{nsec @fcpu=50MHz})$$

PLL jitter is an important factor for bus cycles using waitstates and for the operation of timers, serial interfaces, etc. For slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is negligible.

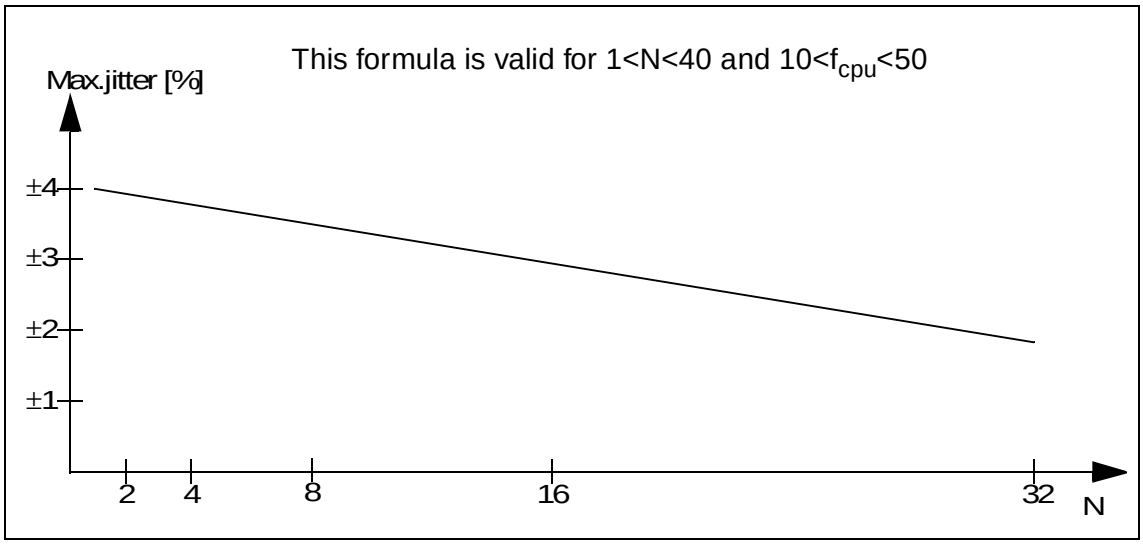

Figure 15 Approximated maximum PLL jitter

Parameter	Symbol		Max. CPU Clock = 50 MHz		Variable CPU Clock 1/2TCL = 1 to 50 MHz		Unit
			min.	max.	min.	max.	
Data hold after $\overline{RD}$ rising edge	t_{18}	SR	0	–	0	–	ns
Data float after $\overline{RD}$ rising edge [12)]	t_{19}	SR	–	15 + t_F[2]	–	2TCL - 5 + t_F[2]	ns
Data valid to $\overline{WR}$	t_{22}	CC	13 + t_C	–	2TCL - 7 + t_C	–	ns
Data hold after $\overline{WR}$	t_{23}	CC	13 + t_F	–	2TCL - 7+ t_F	–	ns
ALE rising edge after $\overline{RD}$, $\overline{WR}$	t_{25}	CC	10 + t_F	–	2TCL - 10 + t_F	–	ns
Address hold after $\overline{RD}$, $\overline{WR}$	t_{27}	CC	10 + t_F	–	2TCL - 10 + t_F	–	ns
Latched $\overline{CS}$ setup to ALE	t_{38}	CC	-7 + t_A	3 + t_A	-7 + t_A	3 + t_A	ns
Unlatched $\overline{CS}$ setup to ALE	t_{38u}	CC	3 + t_A	–	TCL - 7 + t_A	–	ns
Latched $\overline{CS}$ low to Valid Data In	t_{39}	SR	–	13 + t_C + 2t_A	–	3TCL - 17 + t_C + 2t_A	ns
Unlatched $\overline{CS}$ low to Valid Data In	t_{39u}	SR	–	23 + t_C + 2t_A	–	4TCL - 17 + t_C + 2t_A	ns
Latched $\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$	t_{40}	CC	20 + t_F	–	3TCL - 10 + t_F	–	ns
Unlatched $\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$	t_{40u}	CC	10 + t_F	–	2TCL - 10 + t_F	–	ns
ALE fall. edge to $\overline{RdCS}$, $\overline{WrCS}$ (with RW delay)	t_{42}	CC	7 + t_A	–	TCL - 3 + t_A	–	ns
ALE fall. edge to $\overline{RdCS}$, $\overline{WrCS}$ (no RW delay)	t_{43}	CC	-3 + t_A	–	-3 + t_A	–	ns
Address float after $\overline{RdCS}$ (with RW delay)[1]	t_{44}	CC	–	3[1]	–	3[1]	ns
Address float after $\overline{RdCS}$ (no RW delay)[1]	t_{45}	CC	–	13[1]	–	TCL + 3[1]	ns

Table 17 Multiplexed bus

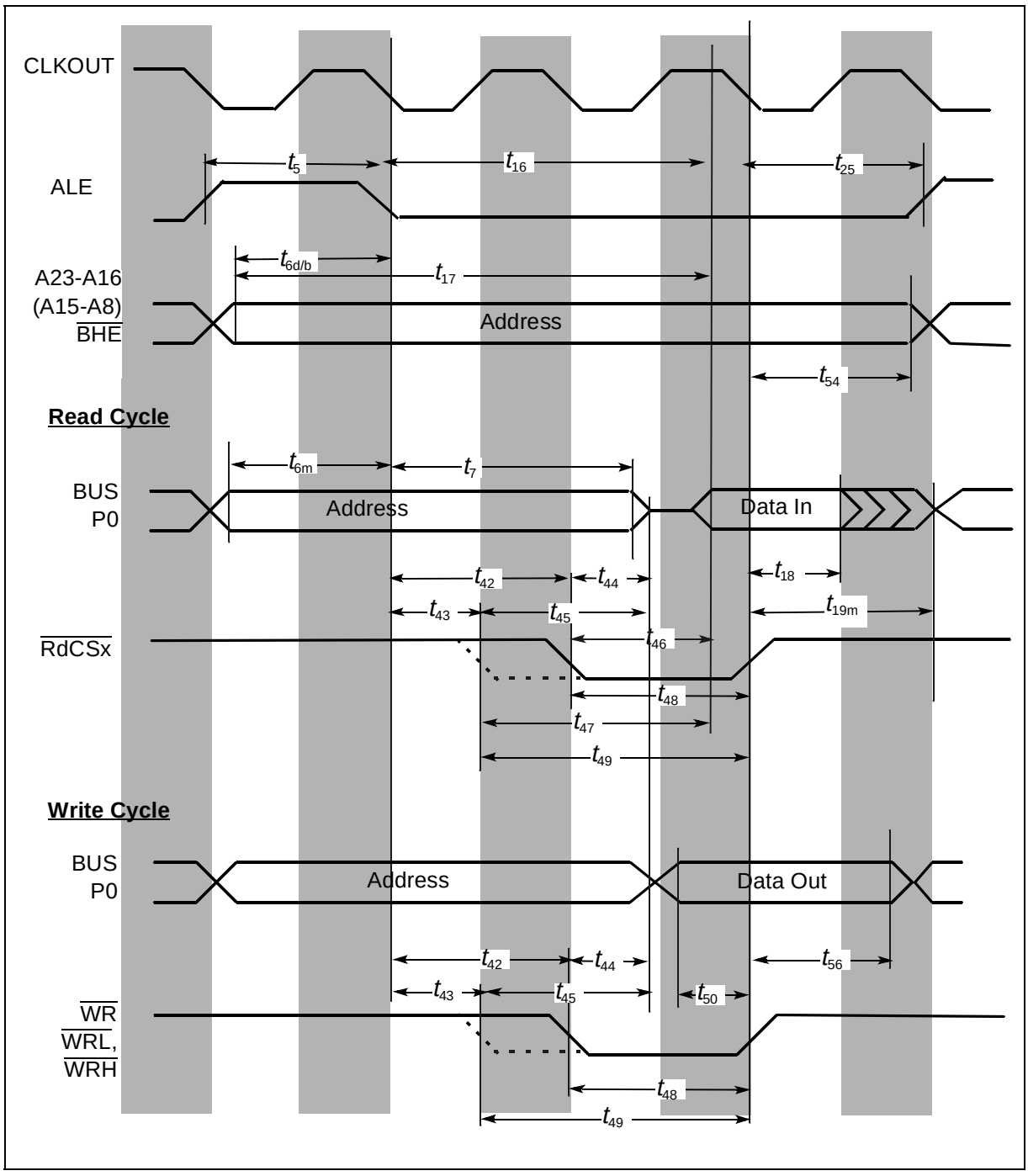

Figure 19 External memory cycle:
multiplexed bus, with/without read/write delay, extended ale, read/write chip select

16.3.4 Demultiplexed Bus

V_{DD} = 3.3 V ± 0.3 V V_{SS} = 0 V T_A = -40 to +85 °C C_L = 50 pF

ALE cycle time = 4 TCL + $2t_A$ + t_C + t_F (40 ns at 50 MHz CPU clock without waitstates)

Parameter	Symbol		Max CPU Clock 50MHz		Variable CPU Clock 1/2TCL = 1 to 50 MHz		Unit
			min.	max.	min.	max.	
ALE high time	t_5	CC	7 + t_A	–	TCL - 3 + t_A	–	ns
Address (P1, P4), $\overline{BHE}$ setup to ALE	t_6	CC	3 + t_A	–	TCL - 7 + t_A	–	ns
Address setup to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_{80}	CC	13 + $2t_A$	–	2TCL - 7 + $2t_A$	–	ns
Address setup to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_{81}	CC	3 + $2t_A$	–	TCL - 7 + $2t_A$	–	ns
$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	t_{12}	CC	13 + t_C	–	2TCL - 7 + t_C	–	ns
$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	t_{13}	CC	23 + t_C	–	3TCL - 7 + t_C	–	ns
$\overline{RD}$ to valid data in (with RW-delay)	t_{14}	SR	–	5 + t_C	–	2TCL - 15 + t_C	ns
$\overline{RD}$ to valid data in (no RW-delay)	t_{15}	SR	–	15 + t_C	–	3TCL - 15 + t_C	ns
ALE low to valid data in	t_{16}	SR	–	15 + t_A + t_C	–	3TCL - 15 + t_A + t_C	ns
Address to valid data in	t_{17}	SR	–	20 + $2t_A$ + t_C	–	4TCL - 20 + $2t_A$ + t_C	ns
Data hold after $\overline{RD}$ rising edge	t_{18}	SR	0	–	0	–	ns
Data float after $\overline{RD}$ rising edge (with RW-delay)[1) 2)]	t_{20}	SR	–	15 + t_F + $2t_A$[2]	–	2TCL - 5 + t_F + $2t_A$[2]	ns
Data float after $\overline{RD}$ rising edge (no RW-delay)[1 2]	t_{21}	SR	–	5 + t_F + $2t_A$[2]	–	TCL - 5 + t_F + $2t_A$[2]	ns
Data valid to $\overline{WR}$	t_{22}	CC	13 + t_C	–	2TCL - 7 + t_C	–	ns

Table 18 Demultiplexed bus

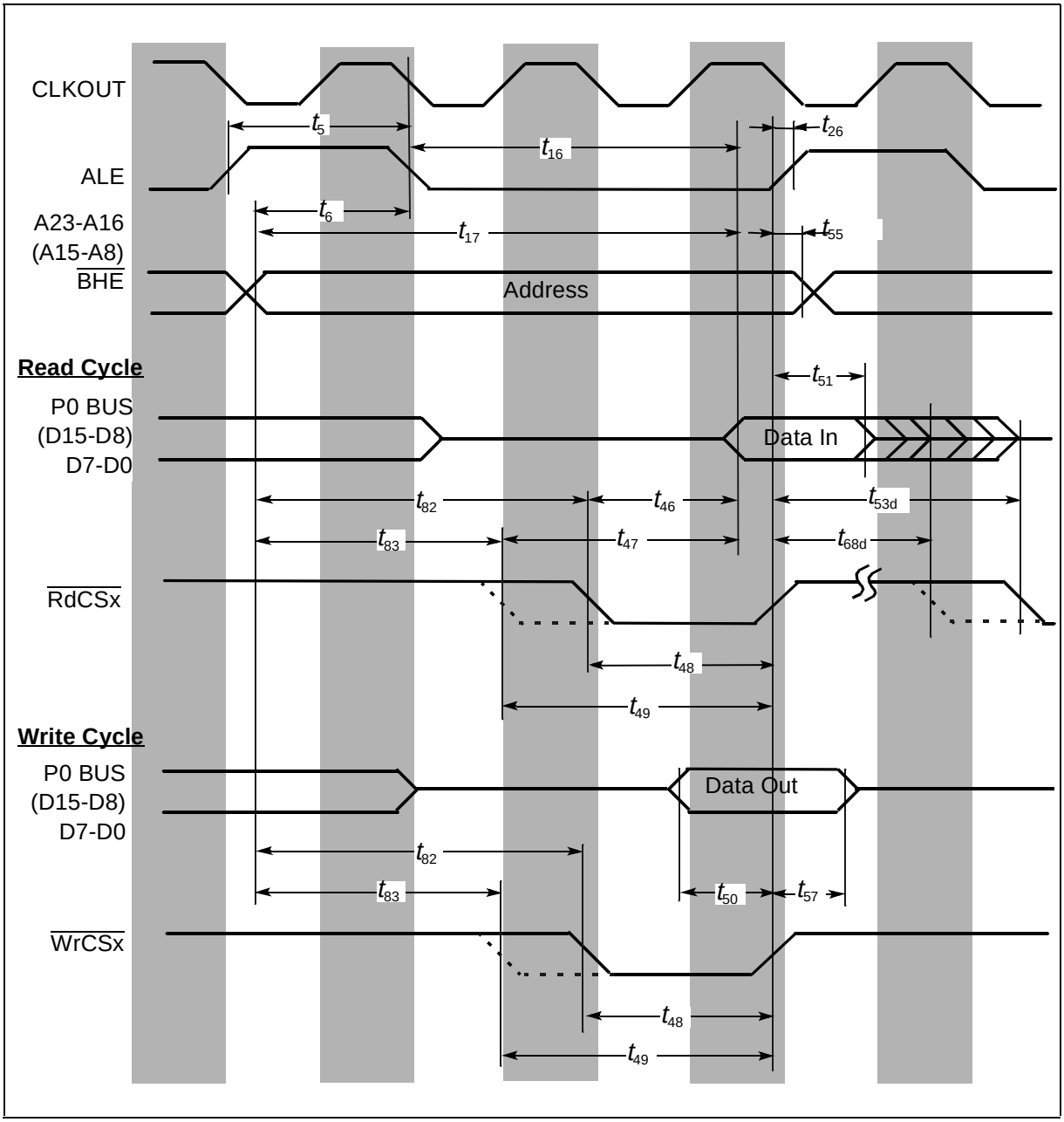

Figure 23 External memory cycle:
demultiplexed bus, no read/write delay, extended ALE, read/write chip select

6 Multiplexed bus modes have a MUX waitstate added after a bus cycle, and an additional MTTC waitstate may be inserted here. For a multiplexed bus with MTTC waitstate this delay is 2 CLKOUT cycles, for a demultiplexed bus without MTTC waitstate this delay is zero.

7 The next external bus cycle may start here.

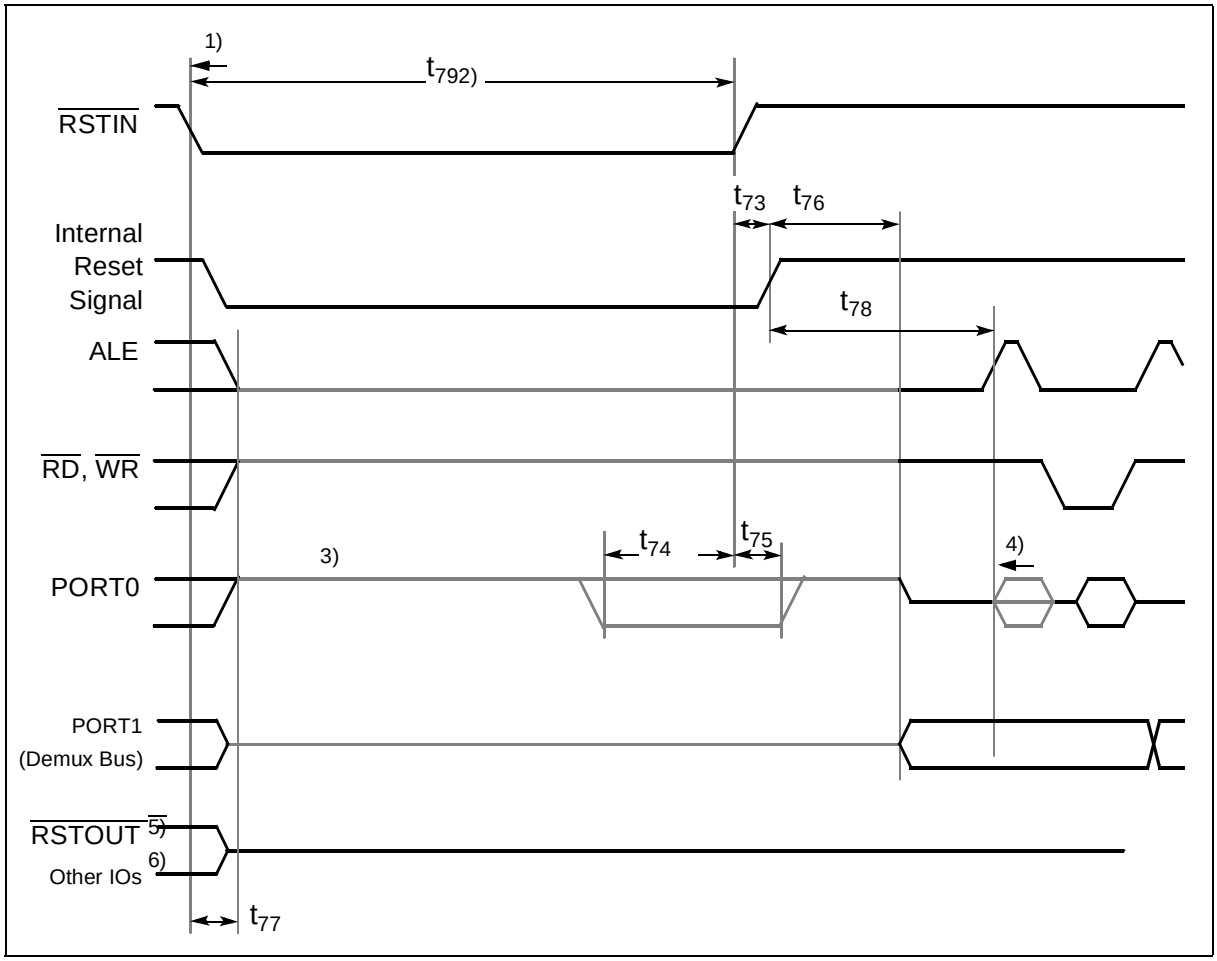

Figure 27 External asynchronous hardware reset (power-up reset): Vpp low

1 The ST10R272L is reset in its default state asynchronously with $\overline{\text{RSTIN}}$. The internal RAM content may be altered if an internal write access is in progress.

2 On power-up, $\overline{\text{RSTIN}}$ must be asserted t_{79} after a stabilized CPU clock signal is available.

3 Internal pullup devices are active on the PORT0 lines, so - input level is high if the respective pin is left open - or is low if the respective pin is connected to an external pulldown device.

4 The ST10R272L starts execution here at address 00’0000h.

5 $\overline{\text{RSTOUT}}$ stays active until execution of the EINIT (end of initialization) instruction.

6 Activation of the IO pins is controlled by software

16.3.8 Synchronous Serial Port Timing

V_{CC} = 3.3 V ± 0.3 V V_{SS} = 0 V T_A = -40 to +85 °C C_L = 50 pF

Parameter	Symbol		Max. Baudrate = 25 MBd		Variable Baudrate = 0.2 to 25 MBd		Unit
			min.	max.	min.	max.	
SSP clock cycle time	t_{200}	CC	40	40	4 TCL	512 TCL	ns
SSP clock high time	t_{201}	CC	13	–	$t_{200}/2$ - 7	–	ns
SSP clock low time	t_{202}	CC	13	–	$t_{200}/2$ - 7	–	ns
SSP clock rise time	t_{203}	CC	–	3	–	3	ns
SSP clock fall time	t_{204}	CC	–	3	–	3	ns
CE active before shift edge	t_{205}	CC	13	–	$t_{200}/2$ - 7	–	ns
CE inactive after latch edge	t_{206}	CC	33	47	t_{200} - 7	t_{200} + 7	ns
Write data valid after shift edge	t_{207}	CC	–	7	–	7	ns
Write data hold after shift edge	t_{208}	CC	0	–	0	–	ns
Write data hold after latch edge	t_{209}	CC	15	25	$t_{200}/2$ - 5	$t_{200}/2$ + 5	ns
Read data active after latch edge	t_{210}	SR	27	–	$t_{200}/2$ + 7	–	ns
Read data setup time before latch edge	t_{211}	SR	15	–	15	–	ns
Read data hold time after latch edge	t_{212}	SR	0	–	0	–	ns

Table 22 Synchronous serial port timing