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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	40MHz
Connectivity	SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	48
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-VQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/t89c51rd2-rdtil

Description

T89C51RD2 is high performance CMOS Flash version of the 80C51 CMOS single chip 8-bit microcontroller. It contains a 64 Kbytes Flash memory block for program and for data.

The 64 Kbytes Flash memory can be programmed either in parallel mode or in serial mode with the ISP capability or with software. The programming voltage is internally generated from the standard V_{CC} pin.

The T89C51RD2 retains all features of the ATMEL 80C52 with 256 bytes of internal RAM, a 7-source 4-level interrupt controller and three timer/counters.

In addition, the T89C51RD2 has a Programmable Counter Array, an XRAM of 1024 bytes, an EEPROM of 2048 bytes, a Hardware Watchdog Timer, a more versatile serial channel that facilitates multiprocessor communication (EUART) and a speed improvement mechanism (X2 mode). Pinout is either the standard 40/44 pins of the C52 or an extended version with 6 ports in a 64/68 pins package.

The fully static design of the T89C51RD2 allows to reduce system power consumption by bringing the clock frequency down to any value, even DC, without loss of data.

The T89C51RD2 has 2 software-selectable modes of reduced activity for further reduction in power consumption. In the idle mode the CPU is frozen while the peripherals and the interrupt system are still operating. In the power-down mode the RAM is saved and all other functions are inoperative.

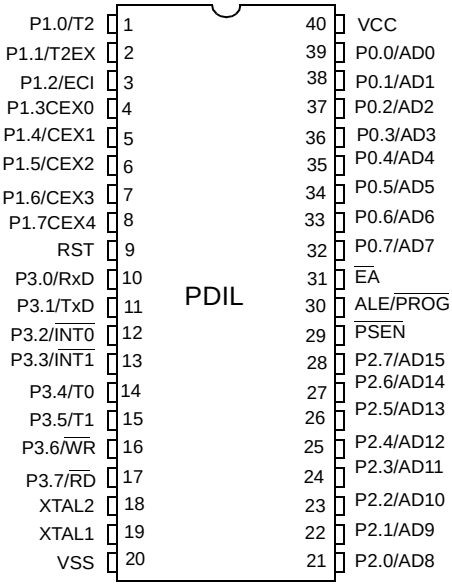
The added features of the T89C51RD2 makes it more powerful for applications that need pulse width modulation, high speed I/O and counting capabilities such as alarms, motor control, corded phones, smart card readers.

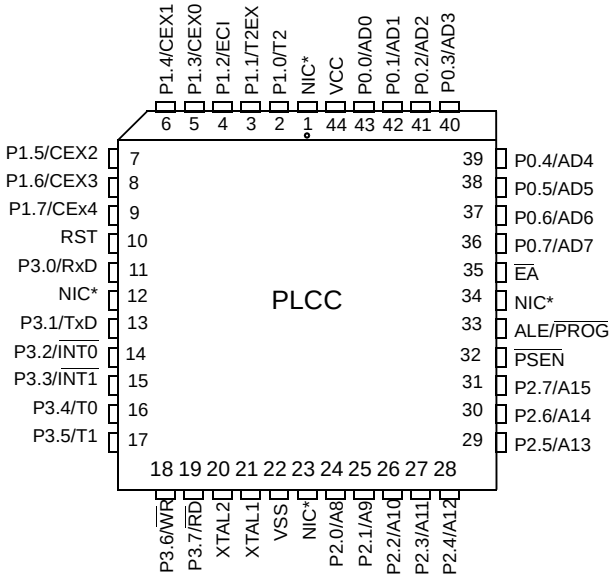
Table 1. Memory Size

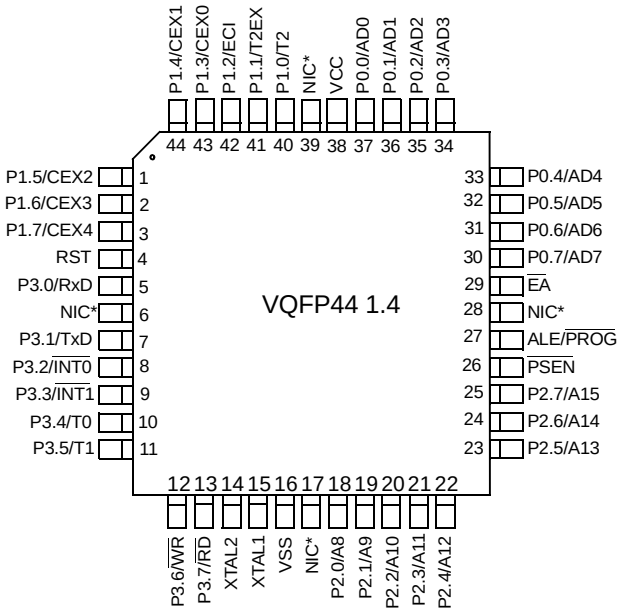
PDIL40 PLCC44 VQFP44 1.4	Flash (bytes)	EEPROM (bytes)	XRAM (bytes)	TOTAL RAM (bytes)	I/O
T89C51RD2	64K	2K	1024	1280	32

PLCC68 VQFP64 1.4	Flash (bytes)	EEPROM (bytes)	XRAM (bytes)	TOTAL RAM (bytes)	I/O
T89C51RD2	64K	2K	1024	1280	48

Pin Configuration







Note: NIC = No Internal Connection

SFR Mapping

The Special Function Registers (SFRs) of the T89C51RD2 fall into the following categories:

- C51 core registers: ACC, B, DPH, DPL, PSW, SP, AUXR1
- I/O port registers: P0, P1, P2, P3, P4, P5
- Timer registers: T2CON, T2MOD, TCON, TH0, TH1, TH2, TMOD, TL0, TL1, TL2, RCAP2L, RCAP2H
- Serial I/O port registers: SADDR, SADEN, SBUF, SCON
- Power and clock control registers: PCON
- Hardware Watchdog Timer register: WDTRST, WDTPRG
- Interrupt system registers: IE, IP, IPH
- Flash and EEPROM registers: FCON, EECON, EETIM
- Others: AUXR, AUXR1, CKCON

Enhanced Features

In comparison to the original 80C52, the T89C51RD2 implements some new features, which are:

- The X2 option
- The Dual Data Pointer
- The extended RAM
- The Programmable Counter Array (PCA)
- The Watchdog
- The 4 level interrupt priority system
- The power-off flag
- The ONCE mode
- The ALE disabling
- Some enhanced features are also located in the UART and the Timer 2

X2 Feature and Clock Generation

The T89C51RD2 core needs only 6 clock periods per machine cycle. This feature called "X2" provides the following advantages:

- Divide frequency crystals by 2 (cheaper crystals) while keeping same CPU power.
- Save power consumption while keeping same CPU power (oscillator power saving).
- Save power consumption by dividing dynamically operating frequency by 2 in operating and idle modes.
- Increase CPU power by 2 while keeping same crystal frequency.

In order to keep the original C51 compatibility, a divider by 2 is inserted between the XTAL1 signal and the main clock input of the core (phase generator). This divider may be disabled by software.

Description

The clock for the whole circuit and peripheral is first divided by two before being used by the CPU core and peripherals. This allows any cyclic ratio to be accepted on XTAL1 input. In X2 mode, as this divider is bypassed, the signals on XTAL1 must have a cyclic ratio between 40 to 60%. Figure 1 shows the clock generation block diagram. X2 bit is validated on XTAL1÷2 rising edge to avoid glitches when switching from X2 to STD mode. Figure 2 shows the mode switching waveforms.

Figure 1. Clock Generation Diagram

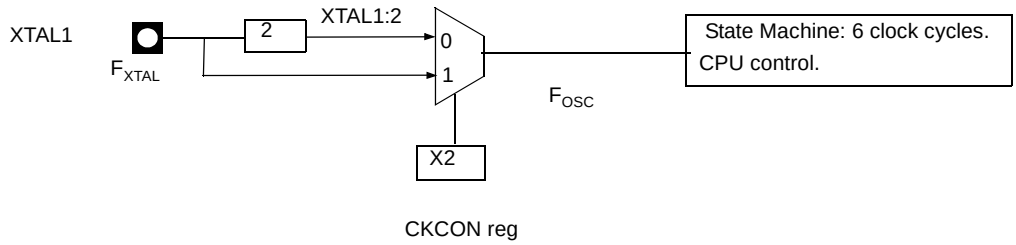
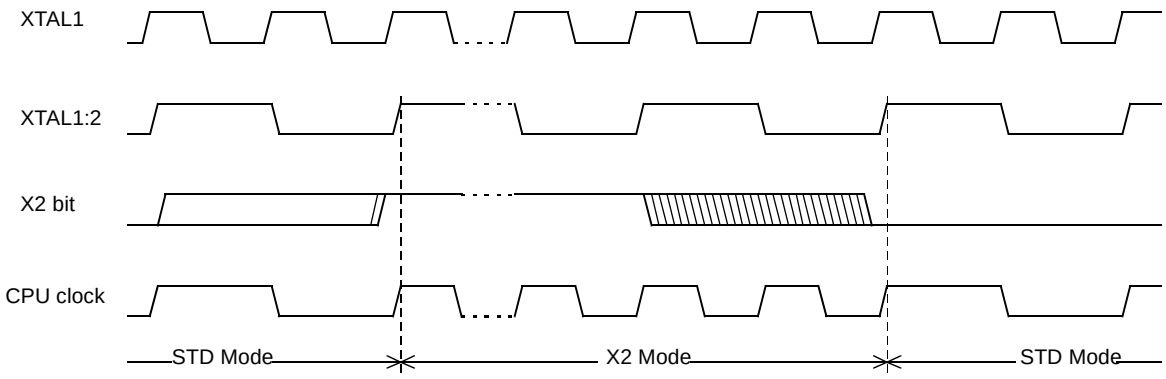


Figure 2. Mode Switching Waveforms



The X2 bit in the CKCON register (Table 4) allows to switch from 12 clock periods per instruction to 6 clock periods and vice versa. At reset, the standard speed is activated (STD mode). Setting this bit activates the X2 feature (X2 mode).

The T0X2, T1X2, T2X2, SiX2, PcaX2 and WdX2 bits in the CKCON register (Table 4) allow to switch from standard peripheral speed (12 clock periods per peripheral clock cycle) to fast peripheral speed (6 clock periods per peripheral clock cycle). These bits are active only in X2 mode.

More information about the X2 mode can be found in the application note ANM072 "How to take advantage of the X2 features in TS80C51 microcontroller".

Table 4. CKCON Register
CKCON - Clock Control Register (8Fh)

7	6	5	4	3	2	1	0
-	WdX2	PcaX2	SiX2	T2X2	T1X2	T0X2	X2

Bit Number	Bit Mnemonic	Description
7	-	**Reserved**
6	WdX2	**Watchdog clock** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect) Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
5	PcaX2	**Programmable Counter Array clock** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect) Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
4	SiX2	**Enhanced UART clock (Mode 0 and 2)** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect) Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
3	T2X2	**Timer2 clock** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect) Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.

Figure 6. Clock-Out Mode C/$\overline{T2}$ = 0

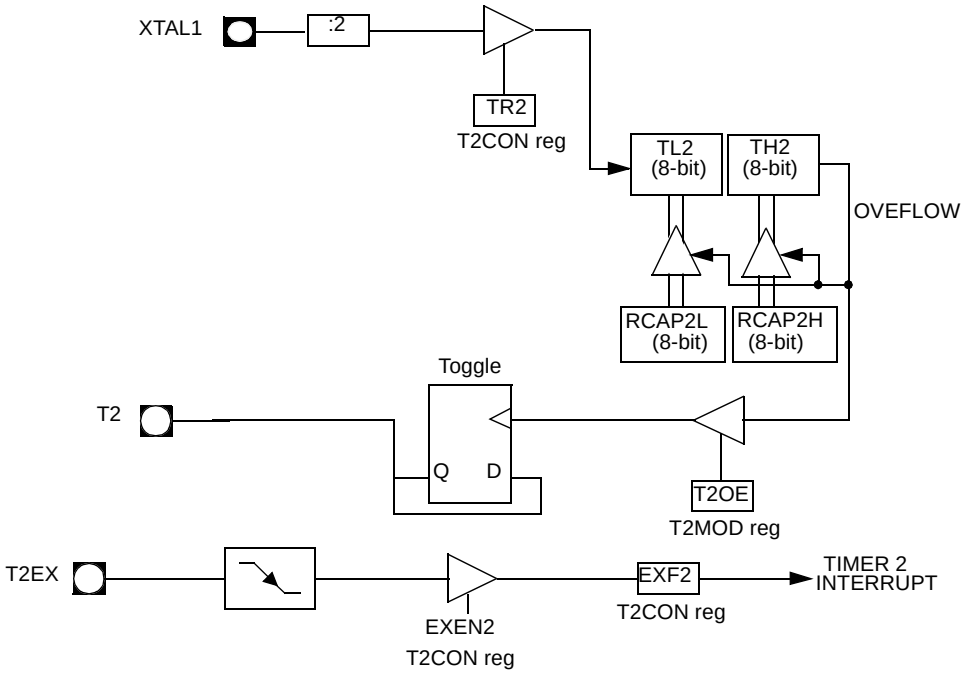


Figure 7. PCA Timer/Counter

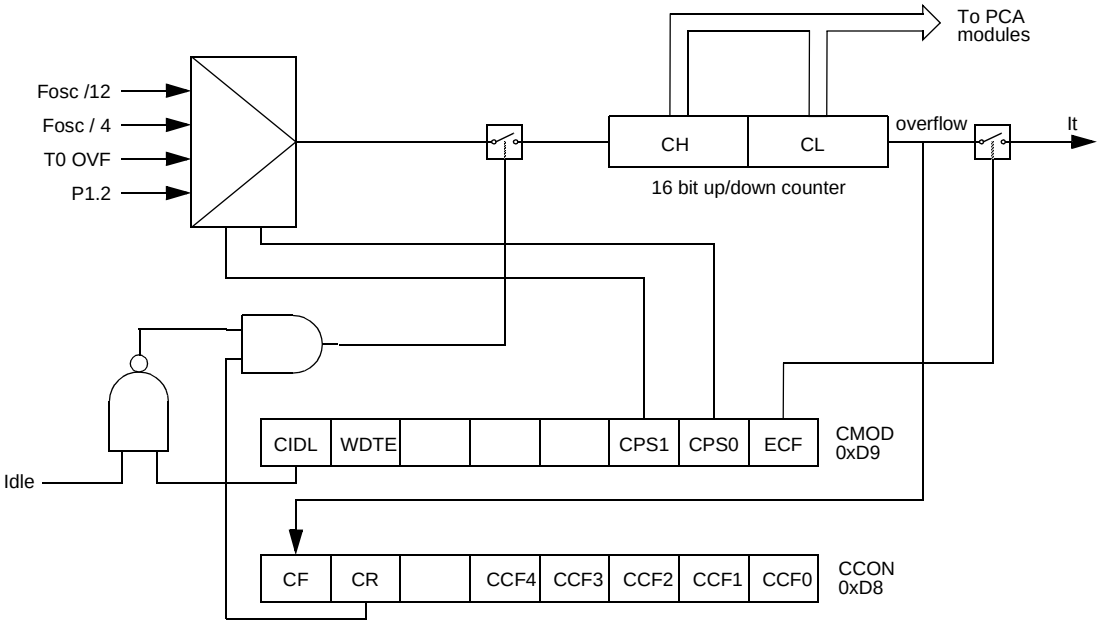


Table 10. CMOD: PCA Counter Mode Register

CMOD Address 0D9H	CIDL	WDTE	-	-	-	CPS1	CPS0	ECF
Reset value	0	0	X	X	X	0	0	0

Symbol	Function		
CIDL	Counter Idle control: CIDL = 0 programs the PCA Counter to continue functioning during idle Mode. CIDL = 1 programs it to be gated off during idle.		
WDTE	Watchdog Timer Enable: WDTE = 0 disables Watchdog Timer function on PCA Module 4. WDTE = 1 enables it.		
-	Not implemented, reserved for future use. (1)		
CPS1	PCA Count Pulse Select bit 1.		
CPS0	PCA Count Pulse Select bit 0.		
	CPS1	CPS0	Selected PCA input. (2)
	0	0	Internal clock f_{osc}/12 (Or f_{osc}/6 in X2 Mode).
	0	1	Internal clock f_{osc}/4 (Or f_{osc}/2 in X2 Mode).
	1	0	Timer 0 Overflow
	1	1	External clock at ECI/P1.2 pin (max rate = f_{osc}/ 8)
ECF	PCA Enable Counter Overflow interrupt: ECF = 1 enables CF bit in CCON to generate an interrupt. ECF = 0 disables that function of CF.		

1. User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.
2. f_{osc} = oscillator frequency

- The last bit in the register ECOM (CCAPMn.6) when set enables the comparator function.

Table 13 shows the CCAPMn settings for the various PCA functions.

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Table 12. CCAPMn: PCA Modules Compare/Capture Control Registers

CCAPMn Address n = 0 - 4	CCAPM0=0DAH CCAPM1=0DBH CCAPM2=0DCH CCAPM3=0DDH CCAPM4=0DEH							
	-	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMm	ECCFn
Reset value	X	0	0	0	0	0	0	0

Symbol	Function
-	Not implemented, reserved for future use. (1)
ECOMn	Enable Comparator. ECOMn = 1 enables the comparator function.
CAPPn	Capture Positive, CAPPn = 1 enables positive edge capture.
CAPNn	Capture Negative, CAPNn = 1 enables negative edge capture.
MATn	Match. When MATn = 1, a match of the PCA counter with this module's compare/capture register causes the CCFn bit in CCON to be set, flagging an interrupt.
TOGn	Toggle. When TOGn = 1, a match of the PCA counter with this module's compare/capture register causes the CEXn pin to toggle.
PWMn	Pulse Width Modulation Mode. PWMn = 1 enables the CEXn pin to be used as a pulse width modulated output.
ECCFn	Enable CCF interrupt. Enables compare/capture flag CCFn in the CCON register to generate an interrupt.

1. User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

Table 13. PCA Module Modes (CCAPMn Registers)

ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMm	ECCFn	Module Function
0	0	0	0	0	0	0	No Operation
X	1	0	0	0	0	X	16-bit capture by a positive-edge trigger on CEXn
X	0	1	0	0	0	X	16-bit capture by a negative trigger on CEXn
X	1	1	0	0	0	X	16-bit capture by a transition on CEXn
1	0	0	1	0	0	X	16-bit Software Timer / Compare mode.
1	0	0	1	1	0	X	16-bit High Speed Output
1	0	0	0	0	1	0	8-bit PWM

The SADEN byte is selected so that each slave may be addressed separately.
For slave A, bit 0 (the LSB) is a don't-care bit; for slaves B and C, bit 0 is a 1. To communicate with slave A only, the master must send an address where bit 0 is clear (e.g. 1111 0000b).
For slave A, bit 1 is a 1; for slaves B and C, bit 1 is a don't care bit. To communicate with slaves B and C, but not slave A, the master must send an address with bits 0 and 1 both set (e.g. 1111 0011b).
To communicate with slaves A, B and C, the master must send an address with bit 0 set, bit 1 clear, and bit 2 clear (e.g. 1111 0001b).

Broadcast Address

A broadcast address is formed from the logical OR of the SADDR and SADEN registers with zeros defined as don't-care bits, e.g.:

```
SADDR 0101 0110b
SADEN 1111 1100b
Broadcast =SADDR OR SADEN1111 111Xb
```

The use of don't-care bits provides flexibility in defining the broadcast address, however in most applications, a broadcast address is FFh. The following is an example of using broadcast addresses:

```
Slave A:SADDR1111 0001b
    SADEN1111 1010b
    Broadcast1111 1X11b,

Slave B:SADDR1111 0011b
    SADEN1111 1001b
    Broadcast1111 1X11B,

Slave C:SADDR=1111 0010b
    SADEN1111 1101b
    Broadcast1111 1111b
```

For slaves A and B, bit 2 is a don't care bit; for slave C, bit 2 is set. To communicate with all of the slaves, the master must send an address FFh. To communicate with slaves A and B, but not slave C, the master can send and address FBh.

Reset Addresses

On reset, the SADDR and SADEN registers are initialized to 00h, i.e. the given and broadcast addresses are XXXX XXXXb (all don't-care bits). This ensures that the serial port will reply to any address, and so, that it is backwards compatible with the 80C51 microcontrollers that do not support automatic address recognition.

Table 18. SADEN - Slave Address Mask Register (B9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b
Not bit addressable

Table 24. IP Register

IP - Interrupt Priority Register (B8h)

7	6	5	4	3	2	1	0
-	PPC	PT2	PS	PT1	PX1	PT0	PX0

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	PPC	**PCA interrupt priority bit** Refer to PPCH for priority level.
5	PT2	**Timer 2 overflow interrupt Priority bit** Refer to PT2H for priority level.
4	PS	**Serial port Priority bit** Refer to PSH for priority level.
3	PT1	**Timer 1 overflow interrupt Priority bit** Refer to PT1H for priority level.
2	PX1	**External interrupt 1 Priority bit** Refer to PX1H for priority level.
1	PT0	**Timer 0 overflow interrupt Priority bit** Refer to PT0H for priority level.
0	PX0	**External interrupt 0 Priority bit** Refer to PX0H for priority level.

Reset Value = X000 0000b

Bit addressable

Table 26. Minimum Reset Capacitor Value for a 50 kΩ Pull-down Resistor(1)

Oscillator Start-Up Time	VDD Rise Time		
	1 ms	10 ms	100 ms
5 ms	820 nF	1.2 µF	12 µF
20 ms	2.7 µF	3.9 µF	12 µF

Note: These values assume V_{DD} starts from 0V to the nominal value. If the time between 2 on/off sequences is too fast, the power-supply de-coupling capacitors may not be fully discharged, leading to a bad reset sequence.

Warm Reset

To achieve a valid reset, the reset signal must be maintained for at least 2 machine cycles (24 oscillator clock periods) while the oscillator is running. The number of clock periods is mode independent (X2 or X1).

Watchdog Reset

As detailed in Section “Watchdog Timer”, the WDT generates a 96-clock period pulse on the RST pin. In order to properly propagate this pulse to the rest of the application in case of external capacitor or power-supply supervisor circuit, a 1 kΩ resistor must be added as shown Figure 18.

Figure 18. Reset Circuitry for WDT Reset-out Usage

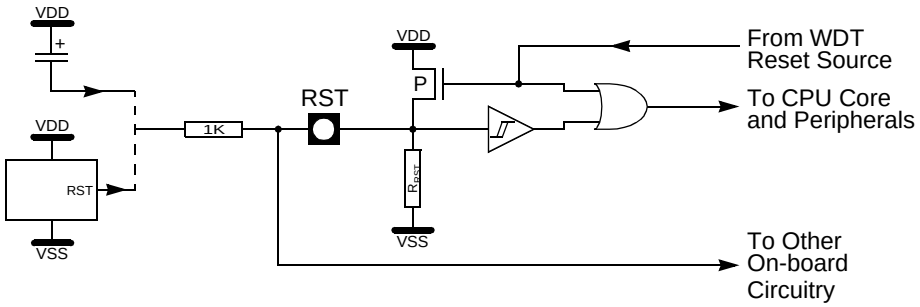


Table 33. EETIM Register

EETIM (S:*0D3*h)
EEPROM timing Control Register

7	6	5	4	3	2	1	0
EETIM							

Bit Number	Bit Mnemonic	Description
7-0	EETIM	Write Timer Register The write timer register value is required to adapt the write time to the oscillator frequency Value = 5 * Fxtal (MHz) in normal mode, 10 * Fxtal in X2 mode. Example : Fxtal = 33 MHZ, EETIM = 0A5h

Reset Value = 0000 0000b

Table 34. Program Lock bits

Program Lock Bits				Protection Description
Security level	LB0	LB1	LB2	
1	U	U	U	No program lock features enabled. MOVC instruction executed from external program memory returns non encrypted data.
2	P	U	U	MOVC instruction executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further parallel programming of the Flash is disabled.ISP and software programming with API are still allowed.
3	X	P	U	Same as 2, also verify through parallel programming interface is disabled.
4	X	X	P	Same as 3, also external execution is disabled.

Note: U: unprogrammed or "one" level.

Note: P: programmed or "zero" level.

Note: X:do not care

Note: WARNING: Security level 2 and 3 should only be programmed after Flash and code verification.

These security bits protect the code access through the parallel programming interface. They are set by default to level 4. The code access through the ISP is still possible and is controlled by the "software security bits" which are stored in the extra Flash memory accessed by the ISP firmware.

To load a new application with the parallel programmer, a chip erase must first be done. This will set the HSB in its inactive state and will erase the Flash memory, including the boot loader and the "Extra Flash Memory" (XAF). If needed, the 1K boot loader and the XAF content must be programmed in the Flash; the code is provided by ATMEL Wireless and Microcontrollers (see section 8.7.); the part reference can always be read using Flash parallel programming modes.

Default Values

The default value of the HSB provides parts ready to be programmed with ISP:

- SB: Cleared to secure the content of the HSB.
- BLJB: Cleared to force ISP operation.
- BLLB: Clear to protect the default boot loader.
- LB2-0: Security level four to protect the code from a parallel access with maximum security.

Software Registers

Several registers are used, in factory and by parallel programmers, to make copies of hardware registers contents. These values are used by ATMEL Wireless and Microcontrollers ISP (see section 8.7.).

These registers are in the "Extra Flash Memory" part of the Flash memory. This block is also called "XAF" or eXtra Array Flash. They are accessed in the following ways:

- Commands issued by the parallel memory programmer.
- Commands issued by the ISP software.

Calls of API issued by the application software.

They are several software registers described in Table 35

Set-up modes configuration

Control and program signals must be held at the levels indicated in the two following tables.

Mode Name	Mode	Rst	Psen	Ale _ _ |_|	EA	P2.6	P2.7	P3.6	P3.7	P0[7..0]
PELCK	Program or Erase Lock. Disable the Erasure or Programming access	1	0	_ _ |_|	1	1	0	1	0	xx
PEULCK	Program or Erase UnLock. Enable the Erasure or Programming access	1	0	Note 2	1	1	0	1	0	55-AA
PGMC	Write Code Data (byte) or write Page Always precedeed by PGML	1	0	_ _ |_| Internally timed	1	0	1	1	1	xx
PGML	Memory Page Load (up to 128 bytes)	1	0	Note 1	1	0	1	0	1	Din
PGMV	Read Code Data (byte)	1	0	1	1	0	_ _ |_|	1	1	Dout
VSB	Read Security Byte (=HSB)	1	0	1	1	0	_ _ |_|	0	1	Dout
PGMS	Write Security Byte (Note 3) (security byte = HSB)	1	0	10 ms	1	1	1	0	0	Din
CERR	Chip Erase User + XAF	1	0	100 ms	1	1	0	0	0	xx
PGXC	Write Byte or Page in Extra Memory (XAF) Always precedeed by PGXL	1	0	_ _ |_| Internally timed	1	1	1	0	1	xx
PGXL	Memory Page Load XAF (up to 128 bytes)	1	0	Note 1	1	1	1	0	1	Din
TMS	Read Signature bytes 30h (Manufacturer code) 31h (Device ID #1) 60h (Device ID #2) 61h (Device ID #3)	1	0	1	1	0	_ _ |_|	0	0	Dout = 58h D7h FCh FFh
RXAF	Read Extra Memory (XAF)	1	0	1	1	0	_ _ |_|	0	0	Dout

Table 44. DC Parameters for Standard Voltage [2]

Symbol	Parameter	Min	Typ[5]	Max	Unit	Test Conditions
$I_{CCProgFlash}$	Power Supply Current during Flash Write / Erase		0.3 Freq (MHz) + 10	0.4 Freq (MHz) + 12	mA	V_{CC} = 5.5 V[1]
$I_{CCProgEE}$	Power Supply Current during EEprom data Write / Erase		0.7 Freq (MHz) + 3	0.7 Freq (MHz) + 18	mA	V_{CC} = 5.5 V[1]
I_{CCIDLE}	Power Supply Current on idle mode			0.5 Freq (MHz) + 2 mA	mA	V_{CC} = 5.5 V[2]

Figure 35. I_{CC} Test Condition, Power-Down Mode

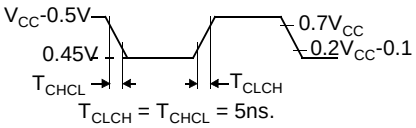
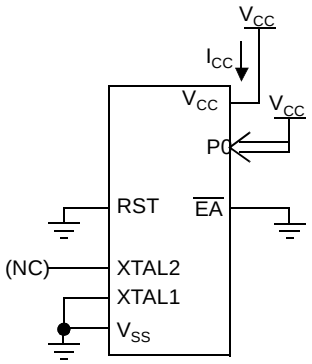


Figure 36. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes



All other pins are disconnected.

AC Parameters

Explanation of the AC Symbols

Each timing symbol has 5 characters. The first character is always a “T” (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

Example: T_{AVLL} = Time for Address Valid to ALE Low.
T_{LLPL} = Time for ALE Low to $\overline{PSEN}$ Low.

T_A = 0 to +70°C; V_{SS} = 0 V; V_{CC} = 5 V ± 10%; M range.
T_A = -40°C to +85°C; V_{SS} = 0 V; V_{CC} = 5 V ± 10%; M range.
T_A = 0 to +70°C; V_{SS} = 0 V; 2.7 V < V_{CC} < 3.3 V; L range.
T_A = -40°C to +85°C; V_{SS} = 0 V; 2.7 V < V_{CC} < 3.3 V; L range.

AC characteristics of -M parts at 3 volts are similar to -L parts

(Load Capacitance for port 0, ALE and PSEN = 100 pF; Load Capacitance for all other outputs = 80 pF.)

Table 44, Table 48 and Table 50 give the description of each AC symbols.

Table 46, Table 49 and Table 51 give for each range the AC parameter.

Table 47, Table 50 and Table 52 give the frequency derating formula of the AC parameter for each speed range description. To calculate each AC symbols. take the x value in the correponding column (-M or -L) and use this value in the formula.

Example: T_{LLIU} for -M and 20 MHz, Standard clock.
x = 35 ns
T = 50 ns
T_{CCIV} = 4T - x = 165 ns

Table 43. DC Parameters in Standard Voltage [1]

Symbol	Parameter	Min	Typ [5]	Max	Unit	Test Conditions
C_{IO}	Capacitance of I/O Buffer			10	pF	Fc = 1 MHz T_A = 25 C
I_{PD}	Power Down Current		120	150	A	V_{CC} = 3 V to 5.5 V[3]
I_{CCOP}	Power Supply Current on normal mode			0.7 Freq (MHz) + 3	mA	V_{CC} = 5.5 V[1]
$I_{CCProgFlash}$	Power Supply Current during Flash Write / Erase		0.3 Freq (MHz) + 10	0.4 Freq (MHz) + 12	mA	V_{CC} = 5.5 V[1]
$I_{CCProgEE}$	Power Supply Current during EEprom data Write / Erase		0.7 Freq (MHz) + 3	0.7 Freq (MHz) + 18	mA	V_{CC} = 5.5 V[1]
I_{CCIDLE}	Power Supply Current on idle mode			0.4 Freq (MHz) + 2	mA	V_{CC} = 5.5 V[2]

DC Parameters for Standard Voltage (2)

T_A = 0 C to +70 C; V_{SS} = 0 V; V_{CC} = 3 V to 5.5 V; F = 0 to 33 MHz.
T_A = -40 C to +85 C; V_{SS} = 0 V; V_{CC} = 3 V to 5.5 V; F = 0 to 33 MHz.

Table 44. DC Parameters for Standard Voltage [2]

Symbol	Parameter	Min	Typ[5]	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5		0.2 V_{CC} - 0.1	V	
V_{IH}	Input High Voltage except XTAL1, RST	0.2 V_{CC} + 0.9		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage, XTAL1, RST	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage, ports 1, 2, 3, 4 and 5 [6]			0.45	V	I_{OL} = 0.8 mA[4]
V_{OL1}	Output Low Voltage, port 0, ALE, $\overline{PSEN}$ [6]			0.45	V	I_{OL} = 1.6 mA[4]
V_{OH}	Output High Voltage, ports 1, 2, 3, 4 and 5	0.9 V_{CC}			V	I_{OH} = -10 A
V_{OH1}	Output High Voltage, port 0, ALE, $\overline{PSEN}$	0.9 V_{CC}			V	I_{OH} = -40 A
I_{IL}	Logical 0 Input Current ports 1, 2, 3, 4 and 5			-50	A	Vin = 0.45 V
I_{LI}	Input Leakage Current for P0 only			10	A	0.45 V < Vin < V_{CC}
I_{TL}	Logical 1 to 0 Transition Current, ports 1, 2, 3, 4 and 5			-650	A	Vin = 2.0 V
R_{RST}	RST Pulldown Resistor	50	90	200	k	
CIO	Capacitance of I/O Buffer			10	pF	Fc = 1 MHz T_A = 25 C
I_{PD}	Power Down Current		120	150	A	V_{CC} = 3 V to 5.5 V[3]
I_{CCOP}	Power Supply Current on normal mode			0.7 Freq (MHz) + 3 mA	mA	V_{CC} = 5.5 V[1]

Figure 35. I_{CC} Test Condition, Power-Down Mode

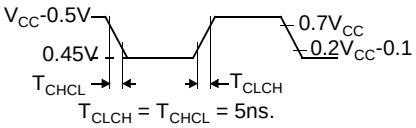
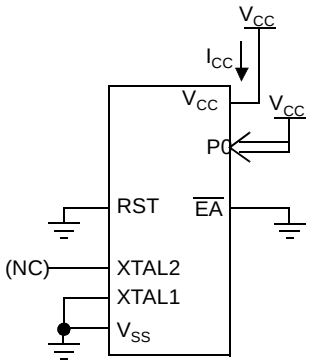


Figure 36. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes



All other pins are disconnected.

AC Parameters

Explanation of the AC Symbols

Each timing symbol has 5 characters. The first character is always a “T” (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

Example: T_{AVLL} = Time for Address Valid to ALE Low.
T_{LLPL} = Time for ALE Low to $\overline{PSEN}$ Low.

T_A = 0 to +70 C; V_{SS} = 0 V; V_{CC} = 5 V 10%; M range.
T_A = -40 C to +85 C; V_{SS} = 0 V; V_{CC} = 5 V 10%; M range.
T_A = 0 to +70 C; V_{SS} = 0 V; 2.7 V < V_{CC} < 3.3 V; L range.
T_A = -40 C to +85 C; V_{SS} = 0 V; 2.7 V < V_{CC} < 3.3 V; L range.

AC characteristics of -M parts at 3 volts are similar to -L parts

(Load Capacitance for port 0, ALE and PSEN = 100 pF; Load Capacitance for all other outputs = 80 pF.)

Table 44, Table 48 and Table 50 give the description of each AC symbols.

Table 46, Table 49 and Table 51 give for each range the AC parameter.

Table 47, Table 50 and Table 52 give the frequency derating formula of the AC parameter for each speed range description. To calculate each AC symbols. take the x value in the correponding column (-M or -L) and use this value in the formula.

Example: T_{LLIU} for -M and 20 MHz, Standard clock.
x = 35 ns
T = 50 ns
T_{CCIV} = 4T - x = 165 ns