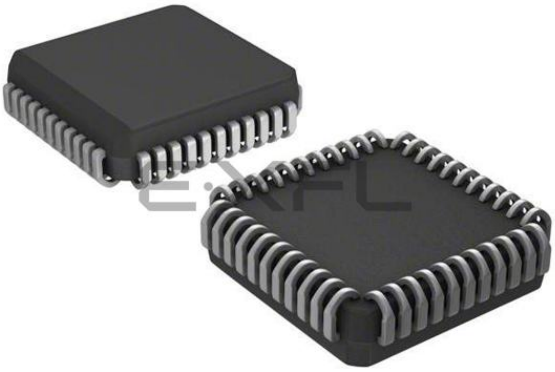

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	40MHz
Connectivity	SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.6x16.6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/t89c51rd2-slsim

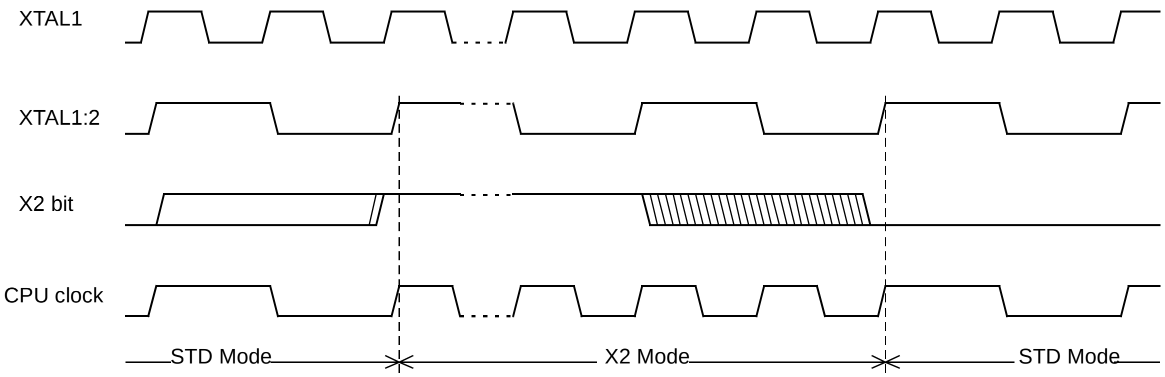
Table 3 below shows all SFRs with their address and their reset value.

Table 3. SFR Table

	Bit Addressable	Non Bit addressable							
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h		CH 0000 0000	CCAP0H XXXX XXXX	CCAP1H XXXX XXXX	CCAP2H XXXX XXXX	CCAP3H XXXX XXXX	CCAP4H XXXX XXXX		FFh
F0h	B 0000 0000								F7h
E8h	P5 1111 1111	CL 0000 0000	CCAP0L XXXX XXXX	CCAP1L XXXX XXXX	CCAP2L XXXX XXXX	CCAP3L XXXX XXXX	CCAP4L XXXX XXXX		EFh
E0h	ACC 0000 0000								E7h
D8h	CCON 00X0 0000	CMOD 00XX X000	CCAPM0 X000 0000	CCAPM1 X000 0000	CCAPM2 X000 0000	CCAPM3 X000 0000	CCAPM4 X000 0000		DFh
D0h	PSW 0000 0000	FCON XXXX 0000	EECON XXXX XX00	EETIM 0000 0000					D7h
C8h	T2CON 0000 0000	T2MOD XXXX XX00	RCAP2L 0000 0000	RCAP2H 0000 0000	TL2 0000 0000	TH2 0000 0000			CFh
C0h	P4 1111 1111							P5 1111 1111	C7h
B8h	IP X000 000	SADEN 0000 0000							BFh
B0h	P3 1111 1111							IPH X000 0000	B7h
A8h	IE 0000 0000	SADDR 0000 0000							AFh
A0h	P2 1111 1111		AUXR1 XXXX 00X0				WDTRST XXXX XXXX	WDTPRG XXXX X000	A7h
98h	SCON 0000 0000	SBUF XXXX XXXX							9Fh
90h	P1 1111 1111								97h
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR XX0X 1000	CKCON X000 0000	8Fh
80h	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000				PCON 00X1 0000	87h
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

▨ reserved

Figure 2. Mode Switching Waveforms



The X2 bit in the CKCON register (Table 4) allows to switch from 12 clock periods per instruction to 6 clock periods and vice versa. At reset, the standard speed is activated (STD mode). Setting this bit activates the X2 feature (X2 mode).

The T0X2, T1X2, T2X2, SiX2, PcaX2 and WdX2 bits in the CKCON register (Table 4) allow to switch from standard peripheral speed (12 clock periods per peripheral clock cycle) to fast peripheral speed (6 clock periods per peripheral clock cycle). These bits are active only in X2 mode.

More information about the X2 mode can be found in the application note ANM072 "How to take advantage of the X2 features in TS80C51 microcontroller".

Table 4. CKCON Register
CKCON - Clock Control Register (8Fh)

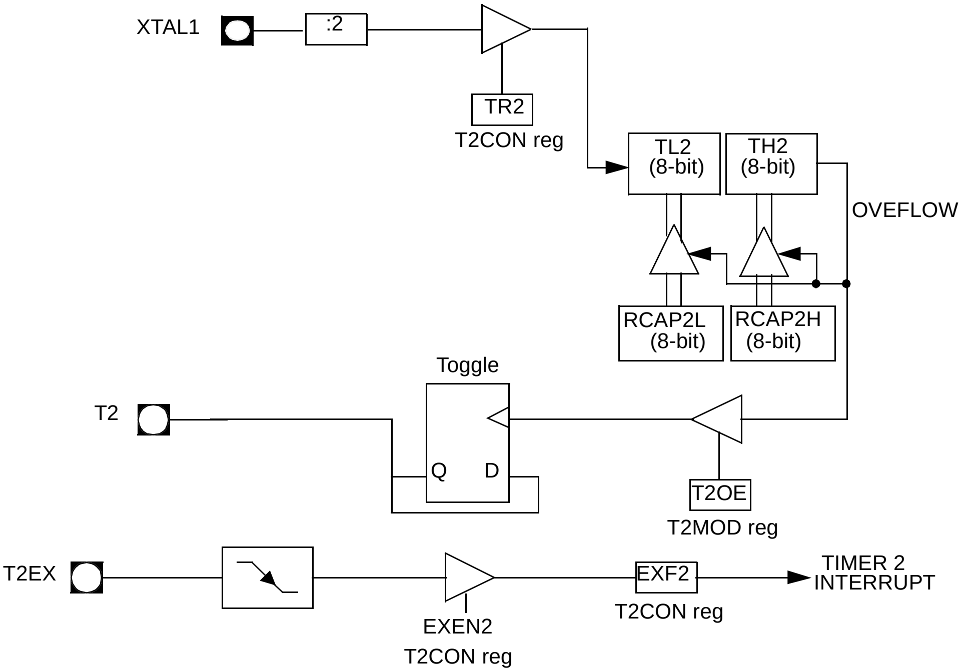
7	6	5	4	3	2	1	0
-	WdX2	PcaX2	SiX2	T2X2	T1X2	T0X2	X2

Bit Number	Bit Mnemonic	Description
7	-	**Reserved**
6	WdX2	**Watchdog clock** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect) Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
5	PcaX2	**Programmable Counter Array clock** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect) Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
4	SiX2	**Enhanced UART clock (Mode 0 and 2)** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect) Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
3	T2X2	**Timer2 clock** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect) Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.

Bit Number	Bit Mnemonic	Description
2	T1X2	**Timer1 clock** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect) Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle
1	T0X2	**Timer0 clock** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect) Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle
0	X2	**CPU clock** Clear to select 12 clock periods per machine cycle (STD mode) for CPU and all the peripherals. Set to select 6clock periods per machine cycle (X2 mode) and to enable the individual peripherals "X2" bits.

Reset Value = X000 0000b
Not bit addressable

Figure 6. Clock-Out Mode C/$\overline{\text{T2}}$ = 0



Programmable Counter Array PCA

The PCA provides more timing capabilities with less CPU intervention than the standard timer/counters. Its advantages include reduced software overhead and improved accuracy. The PCA consists of a dedicated timer/counter which serves as the time base for an array of five compare/ capture modules. Its clock input can be programmed to count any one of the following signals:

- Oscillator frequency ÷ 12 (÷ 6 in X2 mode)
- Oscillator frequency ÷ 4 (÷ 2 in X2 mode)
- Timer 0 overflow
- External input on ECI (P1.2)

Each compare/capture modules can be programmed in any one of the following modes:

- rising and/or falling edge capture,
- software timer,
- high-speed output, or
- pulse width modulator.

Module 4 can also be programmed as a watchdog timer (See Section "PCA Watchdog Timer", page 32).

When the compare/capture modules are programmed in the capture mode, software timer, or high speed output mode, an interrupt can be generated when the module executes its function. All five modules plus the PCA timer overflow share one interrupt vector.

The PCA timer/counter and compare/capture modules share Port 1 for external I/O. These pins are listed below. If one or several bits in the port are not used for the PCA, they can still be used for standard I/O.

PCA component	External I/O Pin
16-bit Counter	P1.2 / ECI
16-bit Module 0	P1.3 / CEX0
16-bit Module 1	P1.4 / CEX1
16-bit Module 2	P1.5 / CEX2
16-bit Module 3	P1.6 / CEX3
16-bit Module 4	P1.7 / CEX4

The PCA timer is a common time base for all five modules (See Figure 7). The timer count source is determined from the CPS1 and CPS0 bits in the **CMOD SFR** (See Table 10) and can be programmed to run at:

- 1/12 the oscillator frequency. (Or 1/6 in X2 Mode)
- 1/4 the oscillator frequency. (Or 1/2 in X2 Mode)
- The Timer 0 overflow
- The input on the ECI pin (P1.2)

- The last bit in the register ECOM (CCAPMn.6) when set enables the comparator function.

Table 13 shows the CCAPMn settings for the various PCA functions.

.

Table 12. CCAPMn: PCA Modules Compare/Capture Control Registers

CCAPMn Address n = 0 - 4	CCAPM0=0DAH
	CCAPM1=0DBH
	CCAPM2=0DCH
	CCAPM3=0DDH
	CCAPM4=0DEH

	-	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMm	ECCFn
Reset value	X	0	0	0	0	0	0	0

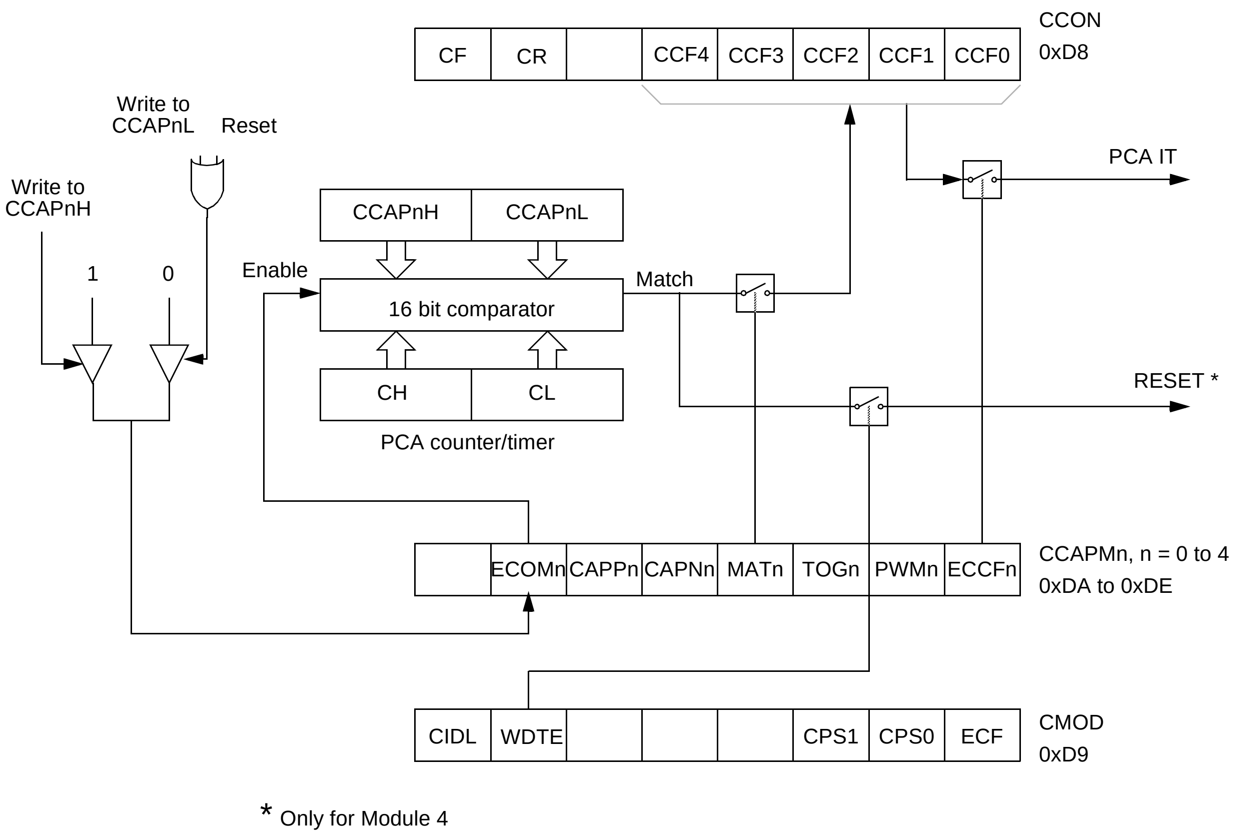
Symbol	Function
-	Not implemented, reserved for future use. (1)
ECOMn	Enable Comparator. ECOMn = 1 enables the comparator function.
CAPPn	Capture Positive, CAPPn = 1 enables positive edge capture.
CAPNn	Capture Negative, CAPNn = 1 enables negative edge capture.
MATn	Match. When MATn = 1, a match of the PCA counter with this module's compare/capture register causes the CCFn bit in CCON to be set, flagging an interrupt.
TOGn	Toggle. When TOGn = 1, a match of the PCA counter with this module's compare/capture register causes the CEXn pin to toggle.
PWMn	Pulse Width Modulation Mode. PWMn = 1 enables the CEXn pin to be used as a pulse width modulated output.
ECCFn	Enable CCF interrupt. Enables compare/capture flag CCFn in the CCON register to generate an interrupt.

1. User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

Table 13. PCA Module Modes (CCAPMn Registers)

ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMm	ECCFn	Module Function
0	0	0	0	0	0	0	No Operation
X	1	0	0	0	0	X	16-bit capture by a positive-edge trigger on CEXn
X	0	1	0	0	0	X	16-bit capture by a negative trigger on CEXn
X	1	1	0	0	0	X	16-bit capture by a transition on CEXn
1	0	0	1	0	0	X	16-bit Software Timer / Compare mode.
1	0	0	1	1	0	X	16-bit High Speed Output
1	0	0	0	0	1	0	8-bit PWM

Figure 10. PCA Compare Mode and PCA Watchdog Timer



Before enabling ECOM bit, CCAPnL and CCAPnH should be set with a non zero value, otherwise an unwanted match could happen. Writing to CCAPnH will set the ECOM bit.

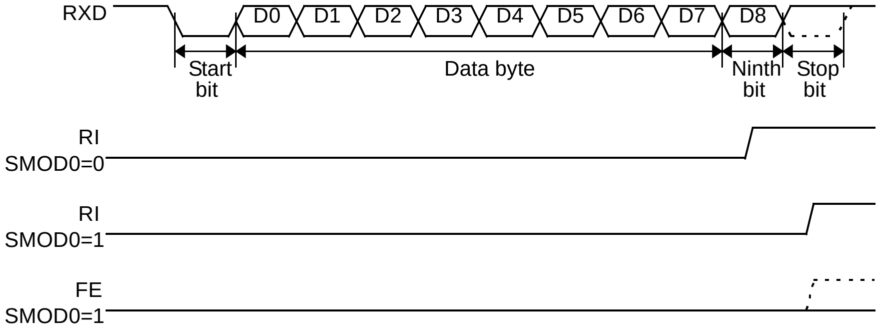
Once ECOM set, writing CCAPnL will clear ECOM so that an unwanted match doesn't occur while modifying the compare value. Writing to CCAPnH will set ECOM. For this reason, user software should write CCAPnL first, and then CCAPnH. Of course, the ECOM bit can still be controlled by accessing to CCAPMn register.

High Speed Output Mode

In this mode the CEX output (on port 1) associated with the PCA module will toggle each time a match occurs between the PCA counter and the module's capture registers. To activate this mode the TOG, MAT, and ECOM bits in the module's CCAPMn SFR must be set (See Figure 11).

A prior write must be done to CCAPnL and CCAPnH before writing the ECOMn bit.

Figure 15. UART Timings in Modes 2 and 3



Automatic Address Recognition

The automatic address recognition feature is enabled when the multiprocessor communication feature is enabled (SM2 bit in SCON register is set).

Implemented in hardware, automatic address recognition enhances the multiprocessor communication feature by allowing the serial port to examine the address of each incoming command frame. Only when the serial port recognizes its own address, the receiver sets RI bit in SCON register to generate an interrupt. This ensures that the CPU is not interrupted by command frames addressed to other devices.

If desired, you may enable the automatic address recognition feature in mode 1. In this configuration, the stop bit takes the place of the ninth data bit. Bit RI is set only when the received command frame address matches the device's address and is terminated by a valid stop bit.

To support automatic address recognition, a device is identified by a given address and a broadcast address.

Note: The multiprocessor communication and automatic address recognition features cannot be enabled in mode 0 (i.e. setting SM2 bit in SCON register in mode 0 has no effect).

Given Address

Each device has an individual address that is specified in SADDR register; the SADEN register is a mask byte that contains don't-care bits (defined by zeros) to form the device's given address. The don't-care bits provide the flexibility to address one or more slaves at a time. The following example illustrates how a given address is formed.

To address a device by its individual address, the SADEN mask byte must be `1111 1111b`.

For example:

```
SADDR0101 0110b
SADEN1111 1100b
Given0101 01XXb
```

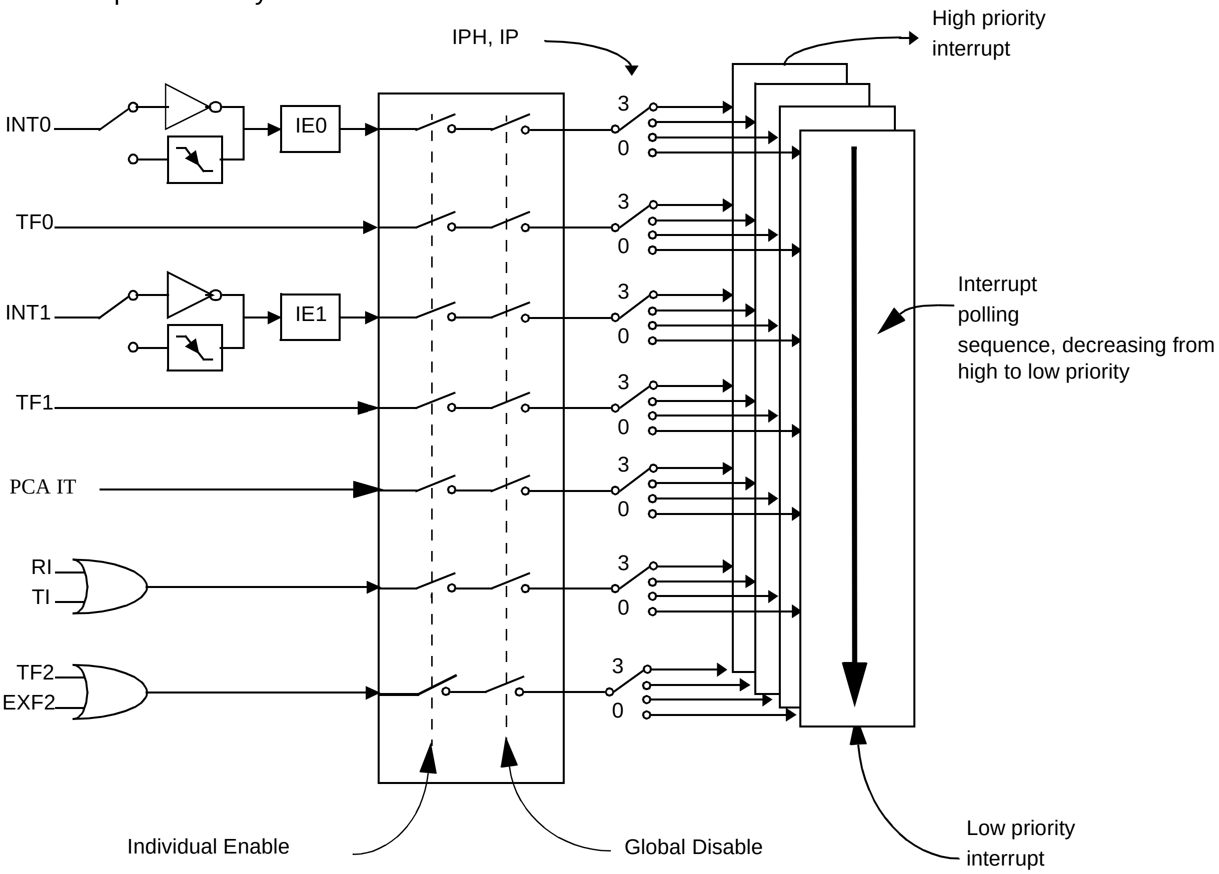
The following is an example of how to use given addresses to address different slaves:

```
Slave A:SADDR1111 0001b
    SADEN1111 1010b
    Given1111 0X0Xb


Slave B:SADDR1111 0011b
    SADEN1111 1001b
    Given1111 0XX1b


Slave C:SADDR1111 0010b
    SADEN1111 1101b
    Given1111 00X1b
```

Interrupt System

The T89C51RD2 has a total of 7 interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (timers 0, 1 and 2), the serial port interrupt and the PCA global interrupt. These interrupts are shown in Figure 16.

Figure 16. Interrupt Control System



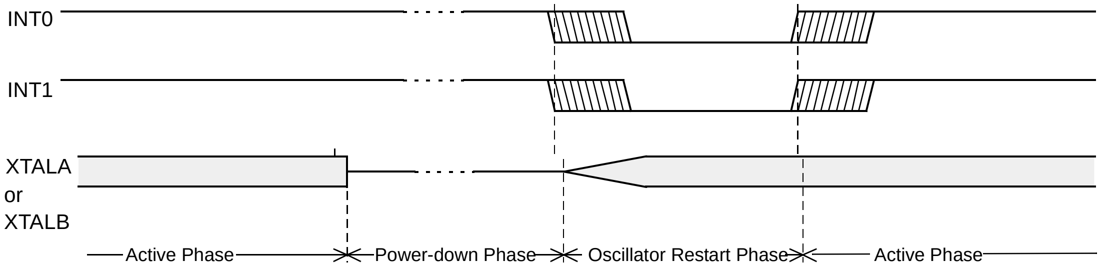
Each of the interrupt sources can be individually enabled or disabled by setting or clearing a bit in the Interrupt Enable register (See Table 23.). This register also contains a global disable bit, which must be cleared to disable all interrupts at once.

Each interrupt source can also be individually programmed to one out of four priority levels by setting or clearing a bit in the Interrupt Priority register (See Table 24.) and in the Interrupt Priority High register (See Table 22). shows the bit values and priority levels associated with each combination.

Table 22. Priority Level Bit Values

IPH.x	IP.x	Interrupt Level Priority
0	0	0 (Lowest)
0	1	1
1	0	2
1	1	3 (Highest)

Figure 19. Power-down Exit Waveform



Exit from Power-down by reset redefines all the SFRs, exit from Power-down by external interrupt does no affect the SFRs.

Exit from Power-down by either reset or external interrupt does not affect the internal RAM content.

Note: If idle mode is activated with Power-down mode (IDL and PD bits set), the exit sequence is unchanged, when execution is vectored to interrupt, PD and IDL bits are cleared and idle mode is not entered.

Table 27 shows the state of ports during idle and power-down modes.

Table 27. State of Ports

Mode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Port Data[(1)]	Port Data	Port Data	Port Data
Idle	External	1	1	Floating	Port Data	Address	Port Data
Power Down	Internal	0	0	Port Data[(1)]	Port Data	Port Data	Port Data
Power Down	External	0	0	Floating	Port Data	Port Data	Port Data

Port 0 can force a 0 level. A "one" will leave port floating.

Bit Number	Bit Mnemonic	Description
0	S0	WDT Time-out select bit 0
		S2 S1 S0Selected Time-out 0 0 0(2^{14} - 1) machine cycles, 16.3 ms @ 12 MHz 0 0 1(2^{15} - 1) machine cycles, 32.7 ms @ 12 MHz 0 1 0(2^{16} - 1) machine cycles, 65.5 ms @ 12 MHz 0 1 1(2^{17} - 1) machine cycles, 131 ms @ 12 MHz 1 0 0(2^{18} - 1) machine cycles, 262 ms @ 12 MHz 1 0 1(2^{19} - 1) machine cycles, 542 ms @ 12 MHz 1 1 0(2^{20} - 1) machine cycles, 1.05 s @ 12 MHz 1 1 1(2^{21} - 1) machine cycles, 2.09 s @ 12 MHz

Reset value XXXX X000

WDT During Power Down and Idle

In Power Down mode the oscillator stops, which means the WDT also stops. While in Power Down mode the user does not need to service the WDT. There are 2 methods of exiting Power Down mode: by a hardware reset or via a level activated external interrupt which is enabled prior to entering Power Down mode. When Power Down is exited with hardware reset, servicing the WDT should occur as it normally should whenever the T89C51RD2 is reset. Exiting Power Down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service routine.

To ensure that the WDT does not overflow within a few states of exiting of powerdown, it is best to reset the WDT just before entering powerdown.

In the Idle mode, the oscillator continues to run. To prevent the WDT from resetting the T89C51RD2 while in Idle mode, the user should always set up a timer that will periodically exit Idle, service the WDT, and re-enter Idle mode.

If the WDT is activated, the power consumption in stand-by mode will be above the specified value.

EEPROM Data Memory

General Description

The EEPROM memory block contains 2048 bytes and is organized in 32 pages (or rows) of 64 bytes. The necessary high programming voltage is generated on-chip using the standard Vcc pin of the microcontroller.

The EEPROM memory block is located at the addresses 0000h to 07FFh of the XRAM memory space and is selected by setting control bits in the EECON register.

A read in the EEPROM memory is done with a MOVX instruction.

A physical write in the EEPROM memory is done in two steps : write data in the column latches and transfer of all data latches in a EEPROM memory row (programming).

The number of data written in the page may vary from 1 to 64 (the page size). When programming, only the data written in the column latch are programmed. This provides the capability to program the whole memory by bytes, by page or by a number of bytes in a page.

Write Data in the Column Latches

Data is written by byte to the column latches as if it was in an external RAM memory. Out of the 16 address bits of the data pointer, the 10 MSB are used for page selection and 6 are used for byte selection. Between two EEPROM programming, all addresses in the column latches must remain in the same page, thus the 10MSB must be unchanged.

The following procedure is used to write in the colums latches :

- Map the program space (Set bit EEE of EECON register)
- Load DPTR with the address to write
- Load A register with the data to be written
- Execute a MOVX @DPTR, A
- If needed loop the three last instructions until the end of a 64bytes page

Programming

The EEPROM programming consists on the following actions :

- write one or more bytes in a page in the column latches. Normally, all bytes must belong to the same page; if this is not the case, the first page address is latched and the others are discarded.
- Set EETIM with the value corresponding to the XTAL frequency.
- Launch the programming by writing the control sequence (52h or 50h followed by A2h or A0h) to the EECON register (see Table 32).
- EEBUSY flag in EECON is then set by hardware to indicate that programming is in progress and that EEPROM segment is not available for read.
- The end of programming is signaled by a hardware clear of the EEBUSY flag.

Example : .....   ; DPTR = EEPROM data pointer, A = Data to write

```
Wait :     MOV     A,EECON
              ANL      A,#01h
              JNZ       Wait
   MOV     EETIM,#3Ch              ; 12MHz*5 = 3Ch
              MOV     EECON,#02h             ; EEE=1 EEPROM mapped
              MOVX  @DPTR,A                  ; Write data to EEPROM
              MOV     EECON,#50h or 52h  ; Write Sequence
              MOV     EECON,#A0h or A2h
              ....
```

Table 33. EETIM Register

EETIM (S:*0D3*h)
EEPROM timing Control Register

7	6	5	4	3	2	1	0
EETIM							

Bit Number	Bit Mnemonic	Description
7-0	EETIM	Write Timer Register The write timer register value is required to adapt the write time to the oscillator frequency Value = 5 * Fxtal (MHz) in normal mode, 10 * Fxtal in X2 mode. Example : Fxtal = 33 MHZ, EETIM = 0A5h

Reset Value = 0000 0000b

7	6	5	4	3	2	1	0
SB	BLJB	BLLB	-	-	LB2	LB1	LB0

Bit Number	Bit Mnemonic	Description
7	SB	**Safe Bit** This bit must be cleared to secure the content of the HSB. Only security level can be increased.
6	BLJB	Boot loader Jump Bit Set to force hardware boot address at 0000h. (unless previously force by hardware conditions as described in the chapter 9.6). Clear to force hardware boot address at FC03h (default).
5	BLLB	Boot loader Lock Bit Set to allow programming and writing of the boot loader segment. Clear to forbid software programming and writing of the boot loader segment (default). This protection protect only ISP or IAP access; protection through parallel access is done globally by the lock bits LB2-0.
4	-	Reserved Do not clear this bit.
3	-	Reserved Do not clear this bit.
2-0	LB2-0	User Memory Lock Bits See Table 29

Boot Loader Lock Bit (BLLB)

One bit of the HSB is used to secure by hardware the internal boot loader sector against software reprogramming.

When the BLLB is cleared, any attempt to write in the boot loader segment (Address FC00h to FFFFh) will have no effect. This protection applies for software writing only.

Boot Loader Jump Bit (BLJB)

One bit of the HSB, the BLJB bit, is used to force the boot address:

- When this bit is set the boot address is 0000h.
- When this bit is reset the boot address is FC03h. By default, this bit is cleared and the ISP is enabled.

Flash memory lock bits

The three lock bits provide different levels of protection for the on-chip code and data, when programmed according to Table 29.

Functional Description

Configuration and Manufacturer Information

The table below lists Configuration and Manufacturer byte information used by the bootloader. This information can be accessed through a set of API or ISP commands.

Mnemonic	Description	Default Value
BSB	Boot Status Byte	FFh
SBV	Software Boot Vector	FCh
SSB	Software Security Byte	FFh
Manufacturer Id		58h
Id1: Family code		D7h
Id2: Product Name		FCh
Id3: Product Revision		FFh

Software Security Bits (SSB)

The SSB protects any Flash access from ISP command.
The command "Program Software Security bit" can only write a higher priority level.

There are three levels of security:

- level 0: ***NO_SECURITY*** (FFh)

This is the default level.
From level 0, one can write level 1 or level 2.

- level 1: ***WRITE_SECURITY*** (10h)

For this level it is impossible to write in the Flash memory, BSB and SBV.
The Bootloader returns ’P’ on write access.
From level 1, one can write only level 2.

- level 2: ***RD_WR_SECURITY*** (00h

The level 2 forbids all read and write accesses to/from the Flash/EEPROM memory.
The Bootloader returns ’L’ on read or write access.
Only a full chip erase in parallel mode (using a programmer) or ISP command can reset the software security bits.
From level 2, one cannot read and write anything.

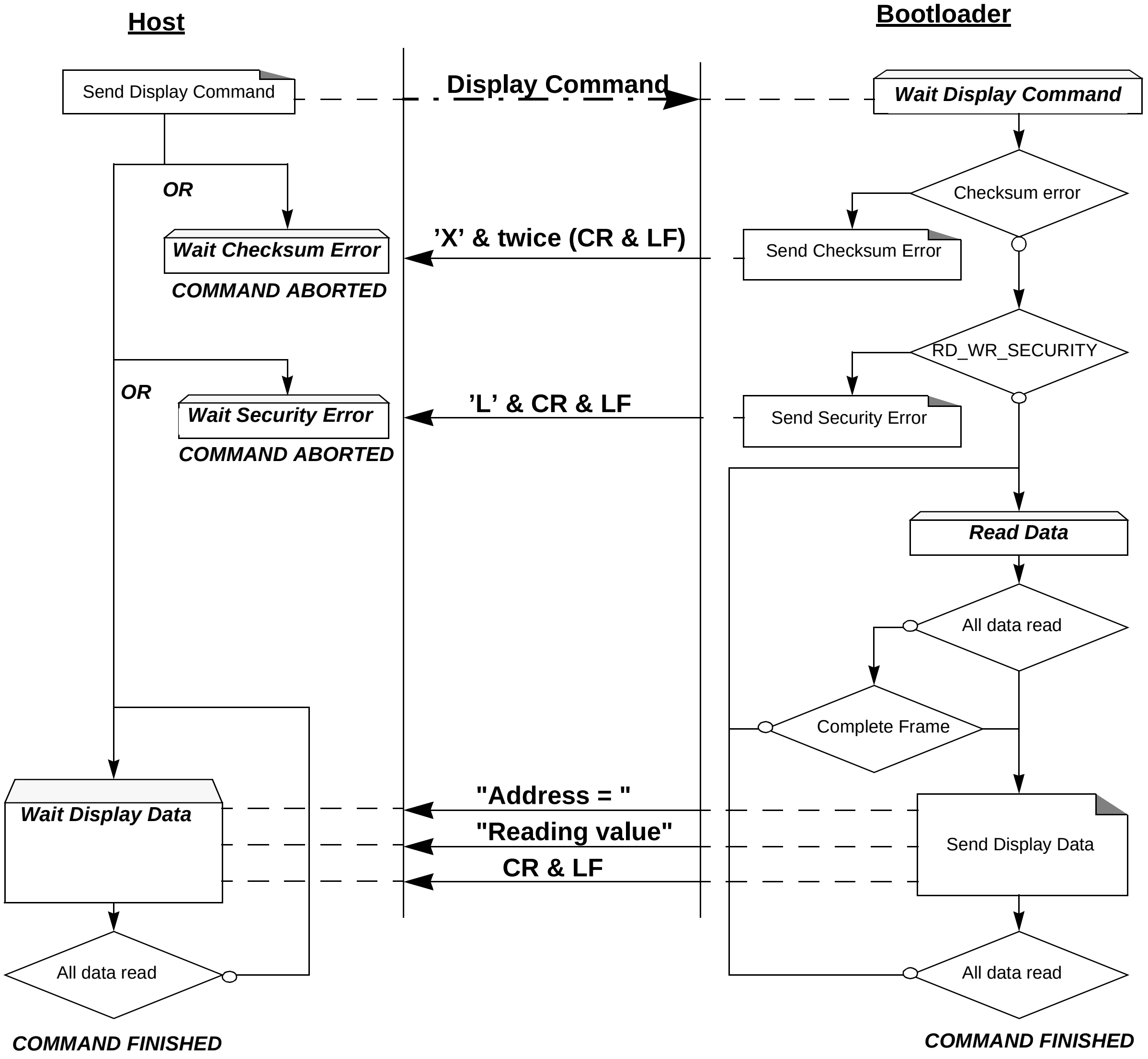
Table 38. Software Security Byte Behavior

	Level 0	Level 1	Level 2
Flash/EEPROM	Any access allowed	Read only access allowed	Any access not allowed
Fuse Bit	Any access allowed	Read only access allowed	Any access not allowed
BSB & SBV	Any access allowed	Read only access allowed	Any access not allowed
SSB	Any access allowed	Write level 2 allowed	Read only access allowed

Display Data

Description

Figure 29. Display Flow



Note: The maximum size of block is 400h. To read more than 400h Bytes, the Host must send a new command.

The API calls description and arguments are shown in Table 41.

Table 41. API Call Summary

Command	R1	A	DPTR0	DPTR1	Returned Value	Command Effect
READ MANUF ID	00h	XXh	0000h	XXh	ACC=Manufacturer ID	Read Manufacturer identifier
READ DEVICE ID1	00h	XXh	0001h	XXh	ACC= Device ID 1	Read Device identifier 1
READ DEVICE ID2	00h	XXh	0002h	XXh	ACC=Device ID 2	Read Device identifier 2
READ DEVICE ID3	00h	XXh	0003h	XXh	ACC=Device ID 3	Read Device identifier 3
PROGRAM DATA BYTE	02h	Byte value to program	Address of Byte to program		ACC = 0 : DONE	Program one Data Byte in user Flash
ERASE BOOT VECTOR	04h	XXh	XXh	XXh	ACC=FCh	Erase Software boot vector and boot status Byte. (SBV=FCh and BSB=FFh)
PROGRAM SSB	05h	XXh	DPH = 00h DPL = 00h	00h	ACC= SSB value	Set SSB level 1
			DPH = 00h DPL = 01h			Set SSB level 2
			DPH = 00h DPL = 10h			Set SSB level 0
			DPH = 00h DPL = 11h			Set SSB level 1
PROGRAM BSB	06h	New BSB value	0000h	XXh	none	Program boot status Byte
PROGRAM SBV	06h	New SBV value	0001h	XXh	none	Program software boot vector
READ SSB	07h	XXh	0000h	XXh	ACC=SSB	Read Software Security Byte
READ HSB	07h	XXh	0004h	XXh	ACC=HSB	Read Hardware Byte
READ BSB	07h	XXh	0001h	XXh	ACC=BSB	Read Boot Status Byte
READ SBV	07h	XXh	0002h	XXh	ACC=SBV	Read Software Boot Vector
PROGRAM DATA PAGE	09h	Number of Byte to program	Address of the first Byte to program in the Flash memory	Address in XRAM of the first data to program	ACC = 0 : DONE	Program up to 128 Bytes in user Flash. Remark: number of Bytes to program is limited such as the Flash write remains in a single 128 Bytes page. Hence, when ACC is 128, valid values of DPL are 00h, or 80h.
READ BOOT ID1	0Eh	XXh	DPL = 00h	XXh	ACC=ID1	Read boot ID1
READ BOOT ID2	0Eh	XXh	DPL = 01h	XXh	ACC=ID2	Read boot ID2
READ BOOT VERSION	0Fh	XXh	XXXXh	XXh	ACC=Boot_Version	Read bootloader version

Figure 35. I_{CC} Test Condition, Power-Down Mode

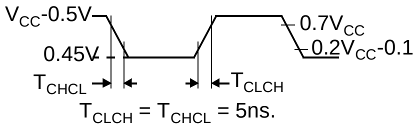
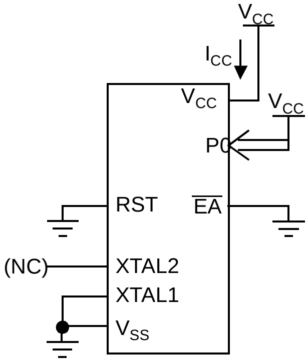


Figure 36. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes



All other pins are disconnected.

AC Parameters

Explanation of the AC Symbols

Each timing symbol has 5 characters. The first character is always a “T” (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

Example:T_{AVLL} = Time for Address Valid to ALE Low.
T_{LLPL} = Time for ALE Low to $\overline{PSEN}$ Low.

TA = 0 to +70°C; V_{SS} = 0 V; V_{CC} = 5 V ± 10%; M range.
TA = -40°C to +85°C; V_{SS} = 0 V; V_{CC} = 5 V ± 10%; M range.
TA = 0 to +70°C; V_{SS} = 0 V; 2.7 V < V_{CC} < 3.3 V; L range.
TA = -40°C to +85°C; V_{SS} = 0 V; 2.7 V < V_{CC} < 3.3 V; L range.

AC characteristics of -M parts at 3 volts are similar to -L parts

(Load Capacitance for port 0, ALE and PSEN = 100 pF; Load Capacitance for all other outputs = 80 pF.)

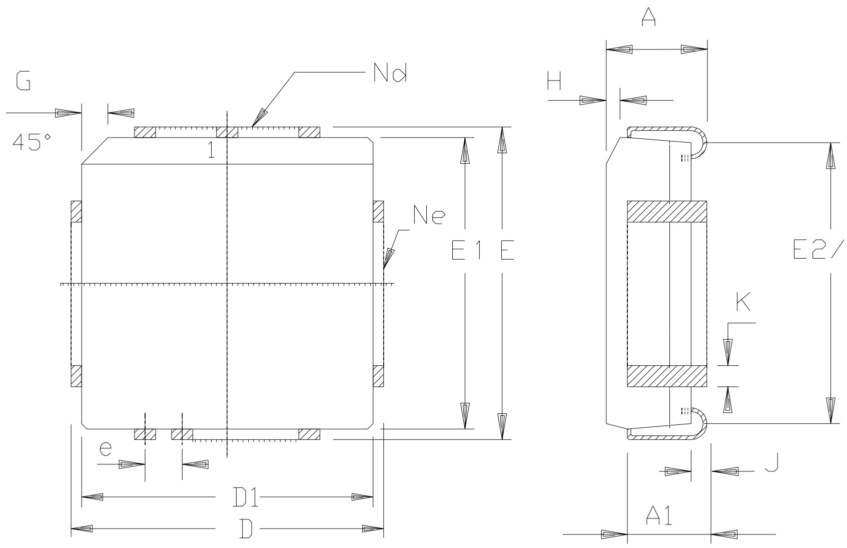
Table 44, Table 48 and Table 50 give the description of each AC symbols.

Table 46, Table 49 and Table 51 give for each range the AC parameter.

Table 47, Table 50 and Table 52 give the frequency derating formula of the AC parameter for each speed range description. To calculate each AC symbols. take the x value in the correponding column (-M or -L) and use this value in the formula.

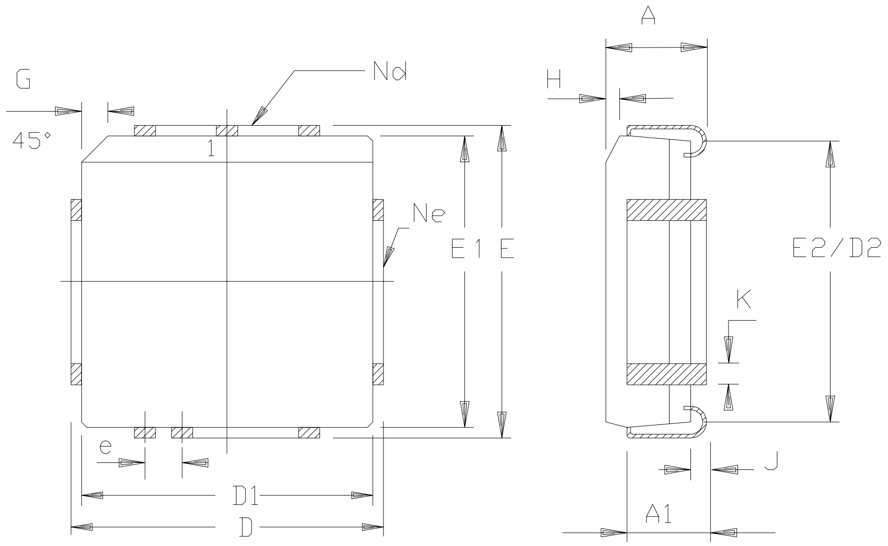
Example: T_{LLIU} for -M and 20 MHz, Standard clock.
x = 35 ns
T = 50 ns
T_{CCIV} = 4T - x = 165 ns

PLCC44



	MM		INCH	
A	4.20	4.57	.165	.180
A1	2.29	3.04	.090	.120
D	17.40	17.65	.685	.695
D1	16.44	16.66	.647	.656
D2	14.99	16.00	.590	.630
E	17.40	17.65	.685	.695
E1	16.44	16.66	.647	.656
E2	14.99	16.00	.590	.630
e	1.27	BSC	.050	BSC
G	1.07	1.22	.042	.048
H	1.07	1.42	.042	.056
J	0.51	-	.020	-
K	0.33	0.53	.013	.021
Nd	11		11	
Ne	11		11	
PKG STD	00			

PLCC68



	MM		INCH	
A	4.20	5.08	.165	.200
A1	2.29	3.30	.090	.130
D	25.02	25.27	.985	.995
D1	24.13	24.33	.950	.958
D2	22.61	23.62	.890	.930
E	25.02	25.27	.985	.995
E1	24.13	24.33	.950	.958
E2	22.61	23.62	.890	.930
e	1.27	BSC	.050	BSC
G	1.07	1.22	.042	.048
H	1.07	1.42	.042	.056
J	0.51	-	.020	-
K	0.33	0.53	.013	.021
Nd	17		17	
Ne	17		17	
PKG STD	00			