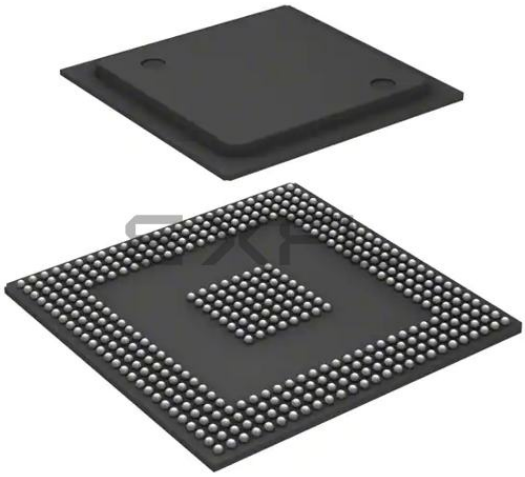
Infineon Technologies - SAK-TC1197-512F180E AC Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	TriCore™
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	ASC, CANbus, EBI/EMI, MLI, MSC, SSC
Peripherals	DMA, POR, WDT
Number of I/O	219
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	224K x 8
Voltage - Supply (Vcc/Vdd)	1.42V ~ 1.58V
Data Converters	A/D 48x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BBGA
Supplier Device Package	PG-BGA-416-10
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/sak-tc1197-512f180e-ac

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Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- The package and the type of delivery.

For the available ordering codes for the TC1197 please refer to the **“Product Catalog Microcontrollers”**, which summarizes all available microcontroller variants.

This document describes the derivatives of the device.The **Table 1** enumerates these derivatives and summarizes the differences.

Table 1 TC1197 Derivative Synopsis

Derivative	Ambient Temperature Range	Program Flash	CPU frequency
SAK-TC1197-512F180E	T_A = -40°C to +125°C	4 MBytes	180MHz
SAK-TC1197-256F180E	T_A = -40°C to +125°C	2 MBytes	180MHz

2.2 System Architecture of the TC1197

The TC1197 combines three powerful technologies within one silicon die, achieving new levels of power, speed, and economy for embedded applications:

- Reduced Instruction Set Computing (RISC) processor architecture
- Digital Signal Processing (DSP) operations and addressing modes
- On-chip memories and peripherals

DSP operations and addressing modes provide the computational power necessary to efficiently analyze complex real-world signals. The RISC load/store architecture provides high computational bandwidth with low system cost. On-chip memory and peripherals are designed to support even the most demanding high-bandwidth real-time embedded control-systems tasks.

Additional high-level features of the TC1197 include:

- Efficient memory organization: instruction and data scratch memories, caches
- Serial communication interfaces – flexible synchronous and asynchronous modes
- Peripheral Control Processor – standalone data operations and interrupt servicing
- DMA Controller – DMA operations and interrupt servicing
- General-purpose timers
- High-performance on-chip buses
- On-chip debugging and emulation facilities
- Flexible interconnections to external components
- Flexible power-management

The TC1197 is a high-performance microcontroller with TriCore CPU, program and data memories, buses, bus arbitration, an interrupt controller, a peripheral control processor and a DMA controller and several on-chip peripherals. The TC1197 is designed to meet the needs of the most demanding embedded control systems applications where the competing issues of price/performance, real-time responsiveness, computational power, data bandwidth, and power consumption are key design elements.

The TC1197 offers several versatile on-chip peripheral units such as serial controllers, timer units, and Analog-to-Digital converters. Within the TC1197, all these peripheral units are connected to the TriCore CPU/system via the Flexible Peripheral Interconnect (FPI) Bus and the Local Memory Bus (LMB). Several I/O lines on the TC1197 ports are reserved for these peripheral units to communicate with the external world.

- Trigger sources that need a clock in order to be asserted, such as the input signals ESR0, ESR1, the WDT trigger, the parity trigger, or the SW trigger.

2.3.4.4 External Interface

The SCU provides interface pads for system purpose. Various functions are covered by these pins. Due to the different tasks some of the pads can not be shared with other functions but most of them can be shared with other functions. The following functions are covered by the SCU controlled pads:

- Reset request triggers
- Reset indication
- Trap request triggers
- Interrupt request triggers
- Non SCU module triggers

The first three points are covered by the ESR pads and the last two points by the ERU pads.

2.3.4.5 Die Temperature Measurement

The Die Temperature Sensor (DTS) generates a measurement result that indicates directly the current temperature. The result of the measurement can be read via an DTS register.

2.3.5 General Purpose I/O Ports and Peripheral I/O Lines

The TC1197 includes a flexible Ports structure with the following features:

Features

- Digital General-Purpose Input/Output (GPIO) port lines
- Input/output functionality individually programmable for each port line
- Programmable input characteristics (pull-up, pull-down, no pull device)
- Programmable output driver strength for EMI minimization (weak, medium, strong)
- Programmable output characteristics (push-pull, open drain)
- Programmable alternate output functions
- Output lines of each port can be updated port-wise or set/reset/toggled bit-wise

2.3.6 Program Memory Unit (PMU)

The devices of the AudoF family contain at least one Program Memory Unit. This is named “PMU0”. Some devices contain additional PMUs which are named “PMU1”, …

In the TC1197, the PMU0 contains the following submodules:

- The Flash command and fetch control interface for Program Flash and Data Flash.
- The Overlay RAM interface with Online Data Acquisition (OLDA) support.

- Overlay support with SRAM for calibration applications.
- Configurable wait state selection for different CPU frequencies.
- Endurance = 1000; minimum 1000 program/erase cycles per physical sector; reduced endurance of 100 per 16 KB sector.
- Operating lifetime (incl. Retention): 20 years with endurance=1000.
- For further operating conditions see data sheet section “Flash Memory Parameters”.

Data Flash Features and Functions

Note: Only available in PMU0.

- 64 Kbyte on-chip Flash, configured in two independent Flash banks of equal size.
- 64 bit read interface.
- Erase/program one bank while data read access from the other bank.
- Programming one bank while erasing the other bank using an automatic suspend/resume function.
- Dynamic correction of single-bit errors during read access.
- Sector architecture:
  - Two sectors of equal size.
  - Each sector separately erasable.
- 128 byte pages to be written in one step.
- Operational control per command sequences (unlock sequences, same as those of Program Flash) for protection against unintended operation.
- End-of-busy as well as error reporting with interrupt and bus error trap.
- Write state machine for automatic program and erase.
- Margin check for detection of problematic Flash bits.
- Endurance = 30000 (can be device dependent); i.e. 30000 program/erase cycles per sector are allowed, with a retention of min. 5 years.
- Dedicated DFlash status information.
- Other characteristics: Same as Program Flash.

– Up to 16 interrupt output lines are available. Interrupt requests can be routed individually to one of the 16 interrupt output lines.
– Message post-processing notifications can be combined flexibly into a dedicated register field of 256 notification bits.

On-chip Trigger Unit

- 16 on-chip trigger signals

I/O Sharing Unit

- Interconnecting inputs and outputs from internal clocks, FPC, GTC, LTC, ports, and MSC interface

2.5.6.2 Functionality of LTCA2

The Local Timer Cell Array (LTCA2) provides a set of hardware modules required for high-speed digital signal processing:

- Local Timer Cells (LTC) operating in Timer, Capture, or Compare Mode may also be logically tied together to drive a common external port pin with a complex signal waveform. LTCs – enabled in Timer Mode or Capture Mode – can be clocked or triggered by various external or internal events.

The following list summarizes the specific features of the LTCA unit.

The Local Timer Arrays (LTCA2) provides a set of hardware modules required for high-speed digital signal processing:

Signal Generation Unit

- Local Timer Cell (LTC)
  - 32 independent units
  - Three basic operating modes (Timer, Capture and Compare) for 63 units
  - Special compare modes for one unit
  - 16-bit data width
  - f_{GPTA} maximum resolution
  - $f_{GPTA}/2$ maximum input signal frequency

I/O Sharing Unit

- Interconnecting inputs and outputs from internal clocks, LTC, ports, and MSC interface

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
A10	P3.14	I/O0	A1/ PU	**Port 3 General Purpose I/O Line 14**
	IN22	I		**IN22 Line of GPTA0**
	IN22	I		**IN22 Line of GPTA1**
	IN22	I		**IN22 Line of LTCA2**
	OUT22	O1		**OUT22 Line of GPTA0**
	OUT22	O2		**OUT22 Line of GPTA1**
	OUT22	O3		**OUT22 Line of LTCA2**
B9	P3.15	I/O0	A1/ PU	**Port 3 General Purpose I/O Line 15**
	IN23	I		**IN23 Line of GPTA0**
	IN23	I		**IN23 Line of GPTA1**
	IN23	I		**IN23 Line of LTCA2**
	OUT23	O1		**OUT23 Line of GPTA0**
	OUT23	O2		**OUT23 Line of GPTA1**
	OUT23	O3		**OUT23 Line of LTCA2**
Port 4				
AD10	P4.0	I/O0	A2/ PU	**Port 4 General Purpose I/O Line 0**
	IN24	I		**IN24 Line of GPTA0**
	IN24	I		**IN24 Line of GPTA1**
	IN24	I		**IN24 Line of LTCA2**
	OUT24	O1		**OUT24 Line of GPTA0**
	OUT24	O2		**OUT24 Line of GPTA1**
	OUT24	O3		**OUT24 Line of LTCA2**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
H1	P8.1	I/O0	A1/ PU	**Port 8 General Purpose I/O Line 1**
	IN41	I		**I/O Line of GPTA0**
	IN41	I		**I/O Line of GPTA1**
	TREADY1A	I		**MLI1 Transmit Channel ready Input A**
	OUT41	O1		**I/O Line of GPTA0**
	OUT41	O2		**I/O Line of GPTA1**
	Reserved	O3		**-**
J3	P8.2	I/O0	A2/ PU	**Port 8 General Purpose I/O Line 2**
	IN42	I		**I/O Line of GPTA0**
	IN42	I		**I/O Line of GPTA1**
	OUT42	O1		**I/O Line of GPTA0**
	OUT42	O2		**I/O Line of GPTA1**
	TVALID1A	O3		**MLI1 Transmit Channel valid Output A**
J2	P8.3	I/O0	A2/ PU	**Port 8 General Purpose I/O Line 3**
	IN43	I		**I/O Line of GPTA0**
	IN43	I		**I/O Line of GPTA1**
	OUT43	O1		**I/O Line of GPTA0**
	OUT43	O2		**I/O Line of GPTA1**
	TData1	O3		**MLI1 Transmit Channel Data Output A**
J1	P8.4	I/O0	A1/ PU	**Port 8 General Purpose I/O Line 4**
	IN44	I		**I/O Line of GPTA0**
	IN44	I		**I/O Line of GPTA1**
	RCLK1A	I		**MLI1 Receive Channel Clock Input A**
	OUT44	O1		**I/O Line of GPTA0**
	OUT44	O2		**I/O Line of GPTA1**
	Reserved	O3		**-**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
K25	P11.1	I/O0	B1/ PU	**Port 11 General Purpose I/O Line 1**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A1	O		**EBU Address Bus Line 1**
K26	P11.2	I/O0	B1/ PU	**Port 11 General Purpose I/O Line 2**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A2	O		**EBU Address Bus Line 2**
J23	P11.3	I/O0	B1/ PU	**Port 11 General Purpose I/O Line 3**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A3	O		**EBU Address Bus Line 3**
K24	P11.4	I/O0	B1/ PU	**Port 11 General Purpose I/O Line 4**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A4	O		**EBU Address Bus Line 4**
L25	P11.5	I/O0	B1/ PU	**Port 11 General Purpose I/O Line 5**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A5	O		**EBU Address Bus Line 5**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
U25	P13.5	I/O0	B1/ PU	**Port 13 General Purpose I/O Line 5**
	AD5	I		**EBU Address/Data Bus Line 5**
	OUT93	O1		**OUT93 Line of GPTA0**
	OUT93	O2		**OUT93 Line of GPTA1**
	OUT85	O3		**OUT85 Line of LTCA2**
	AD5	O		**EBU Address/Data Bus Line 5**
U23	P13.6	I/O0	B1/ PU	**Port 13 General Purpose I/O Line 6**
	AD6	I		**EBU Address/Data Bus Line 6**
	OUT94	O1		**OUT94 Line of GPTA0**
	OUT94	O2		**OUT94 Line of GPTA1**
	OUT86	O3		**OUT86 Line of LTCA2**
	AD6	O		**EBU Address/Data Bus Line 6**
W26	P13.7	I/O0	B1/ PU	**Port 13 General Purpose I/O Line 7**
	AD7	I		**EBU Address/Data Bus Line 7**
	OUT95	O1		**OUT95 Line of GPTA0**
	OUT95	O2		**OUT95 Line of GPTA1**
	OUT87	O3		**OUT87 Line of LTCA2**
	AD7	O		**EBU Address/Data Bus Line 7**
V25	P13.8	I/O0	B1/ PU	**Port 13 General Purpose I/O Line 8**
	AD8	I		**EBU Address/Data Bus Line 8**
	OUT96	O1		**OUT96 Line of GPTA0**
	OUT96	O2		**OUT96 Line of GPTA1**
	OUT88	O3		**OUT88 Line of LTCA2**
	AD8	O		**EBU Address/Data Bus Line 8**

Table 9 Pin Groups for Overload / Short-Circuit Current Sum Parameter

Group	Pins
21	P9.[14:13, 10:9]
22	P9.[12:11, 8:7, 2]
23	P9.[6:5, 3, 1]
24	P9.[0, 4], P5.[10, 11]
25	P5.[15:14, 9:8]
26	P5.[13:12, 6, 4]
27	P5.[7:5, 3, 0]
28	P3.[7:0]
29	P3.[15:8]
30	P0.[7:0]
31	P0.[15:8]
32	P2.[15:9]
33	P2.[8:4]
34	P2.[3:2], P6[9:8]
35	P6[11, 6:4]
36	P6.[15:12, 10, 7]
37	P8.[7:0]
38	P1.[15:13, 11:8, 5]
39	P1.[12, 7, 6, 4, 3]
40	P1.[1:0], P7.0
41	P7.[5:1]
42	P7.[7:6]

5.3.6 BFCLKO Output Clock Timing

V_{SS} = 0 V;V_{DD} = 1.5 V ± 5%; V_{DDEBU} = 2.5 V ± 5% and 3.3 V ± 5%,;
T_A = -40 °C to +125 °C; C_L = 35 pF

Table 20 BFCLK0 Output Clock Timing Parameters[1)]

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
BFCLKO clock period	t_{BFCLKO}	CC	13.33[2)]	–	–	ns	–
BFCLKO high time	t_5	CC	3	–	–	ns	–
BFCLKO low time	t_6	CC	3	–	–	ns	–
BFCLKO rise time	t_7	CC	–	–	3	ns	–
BFCLKO fall time	t_8	CC	–	–	3	ns	–
BFCLKO duty cycle $t_5/(t_5 + t_6)$[3)]	DC		45	50	55	%	–

1) Not subject to production test, verified by design/characterization.

2) The PLL jitter characteristics add to this value according to the application settings. See the PLL jitter parameters.

3) The PLL jitter is not included in this parameter. If the BFCLKO frequency is equal to f_{CPU}, the K divider has to be regarded.

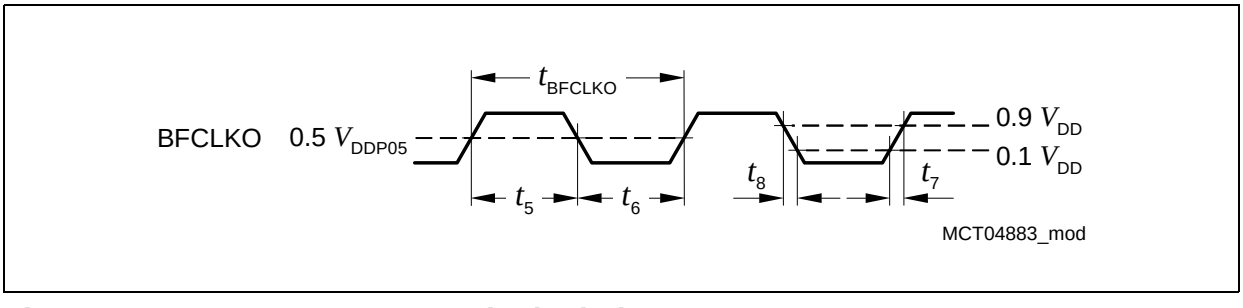

Figure 27 BFCLKO Output Clock Timing

5.3.7 JTAG Interface Timing

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Table 21 JTAG Interface Timing Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK clock period	t_1 SR	25	–	–	ns	–
TCK high time	t_2 SR	12	–	–	ns	–
TCK low time	t_3 SR	10	–	–	ns	–
TCK clock rise time	t_4 SR	–	–	4	ns	–
TCK clock fall time	t_5 SR	–	–	4	ns	–
TDI/TMS setup to TCK rising edge	t_6 SR	6	–	–	ns	–
TDI/TMS hold after TCK rising edge	t_7 SR	6	–	–	ns	–
TDO valid after TCK falling edge[1] (propagation delay)	t_8 CC	–	–	13	ns	C_L = 50 pF
	t_8 CC	–	–	3	ns	C_L = 20 pF
TDO hold after TCK falling edge[1]	t_{18} CC	2	–	–	ns	
TDO high imped. to valid from TCK falling edge[1)2)]	t_9 CC	–	–	14	ns	C_L = 50 pF
TDO valid to high imped. from TCK falling edge[1]	t_{10} CC	–	–	13.5	ns	C_L = 50 pF

1) The falling edge on TCK is used to generate the TDO timing.

2) The setup time for TDO is given implicitly by the TCK cycle time.

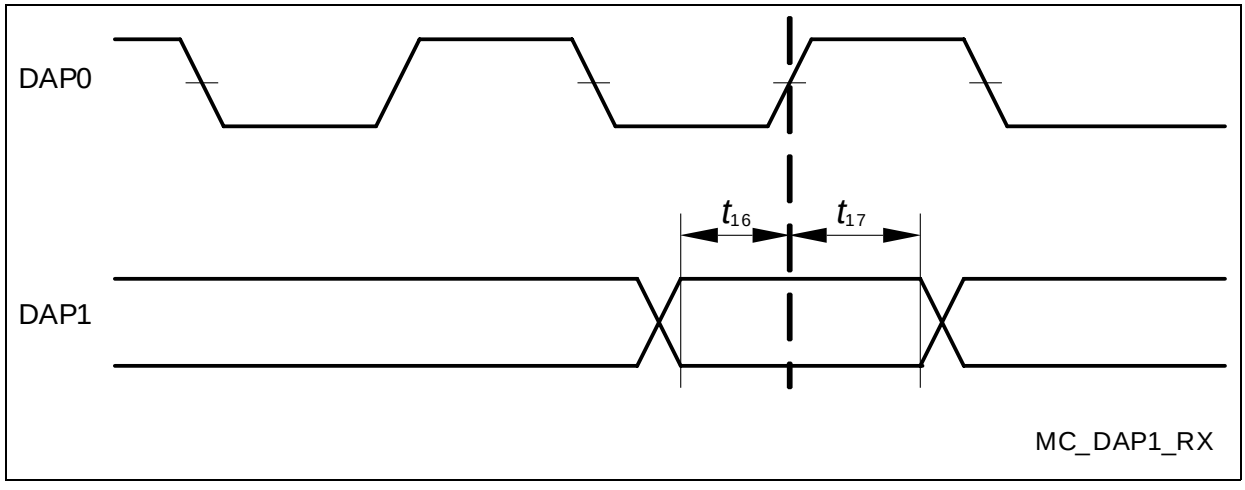

Figure 31 DAP Timing Host to Device

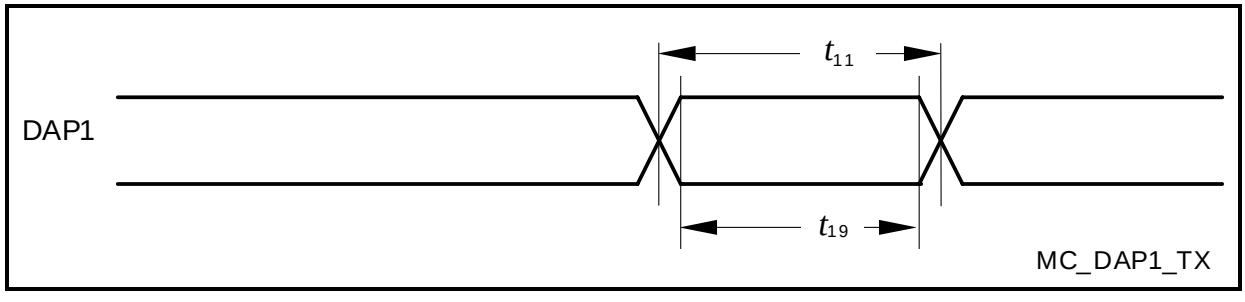

Figure 32 DAP Timing Device to Host

Multiplexed Write Timing

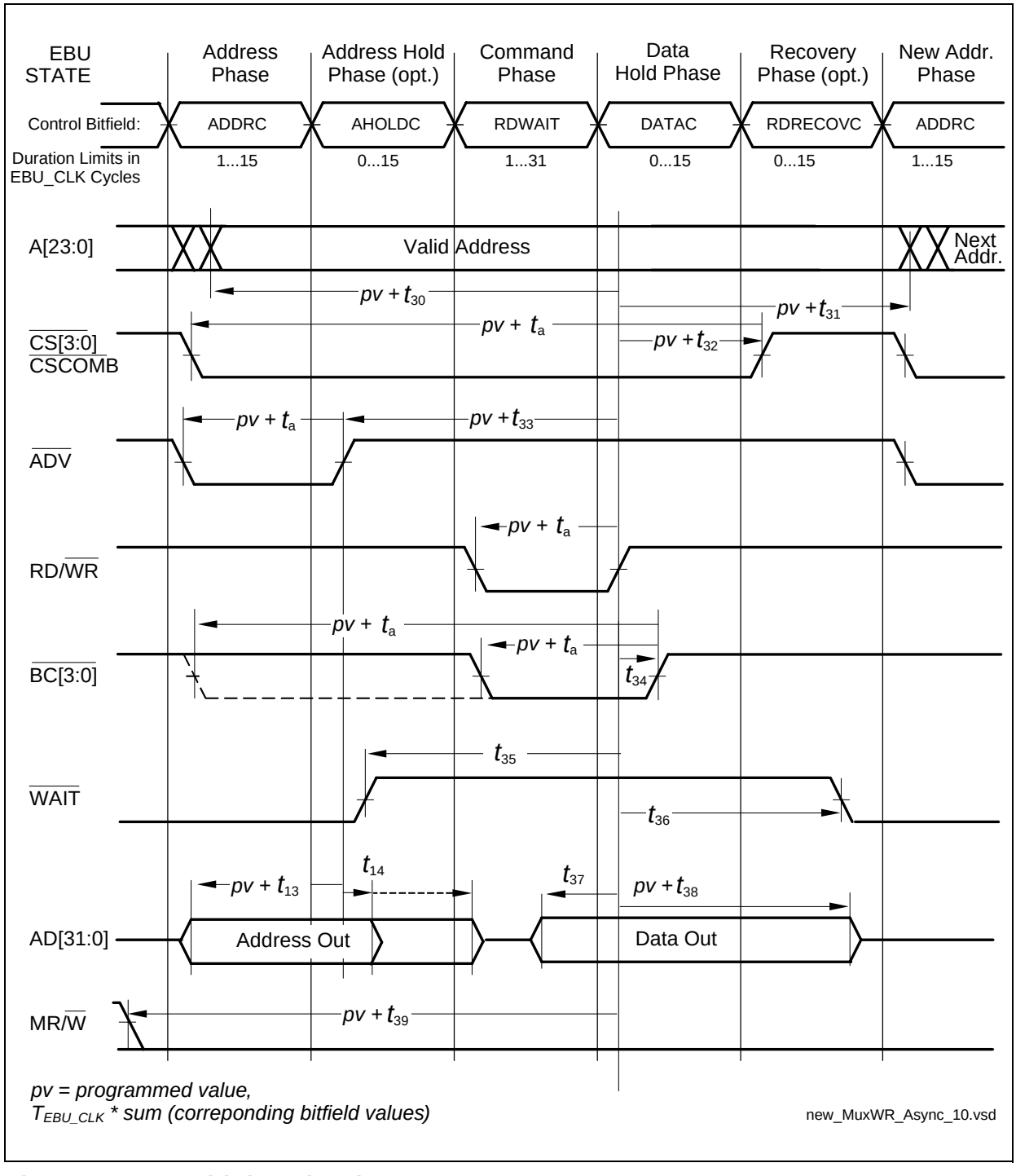

Figure 35 Multiplexed Write Access

Demultiplexed Write Timing

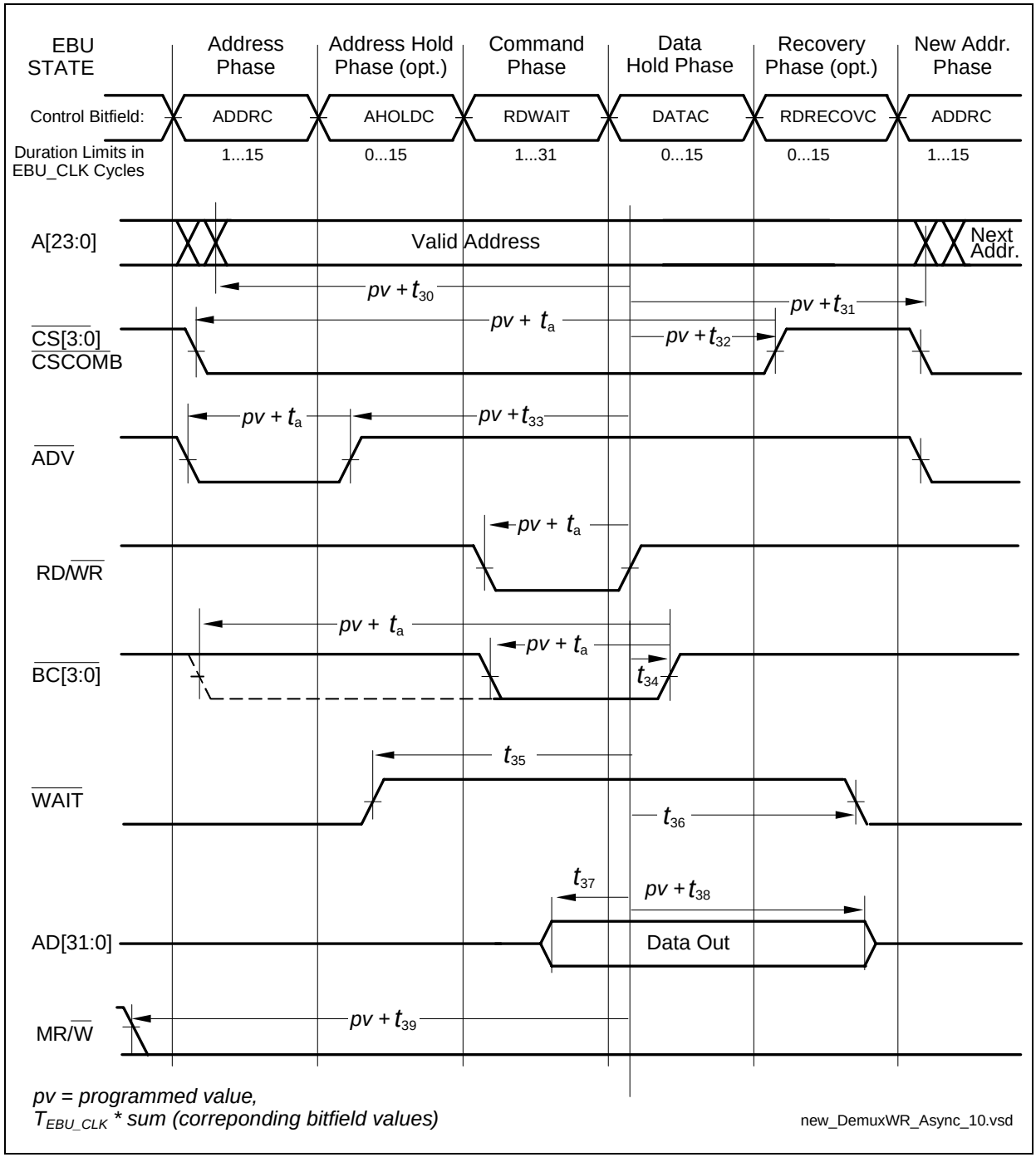

Figure 36 Demultiplexed Write Access

5.3.9.3 EBU Arbitration Signal Timing

V_{SS} = 0 V;V_{DD} = 1.5 V ± 5%; V_{DDEBU} = 2.5 V ± 5% and 3.3 V ± 5%, Class B pins;
T_A = -40°C to +125 °C; C_L = 35 pF;

Table 27 EBU Arbitration Signal Timing Parameters[1)]

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Output delay from BFCLKO rising edge	t_{27}	CC	–	–	3	ns	–
Data setup to BFCLKO falling edge	t_{28}	SR	11	–	–	ns	–
Data hold from BFCLKO falling edge	t_{29}	SR	2	–	–	ns	–

1) Not subject to production test, verified by design/characterization.

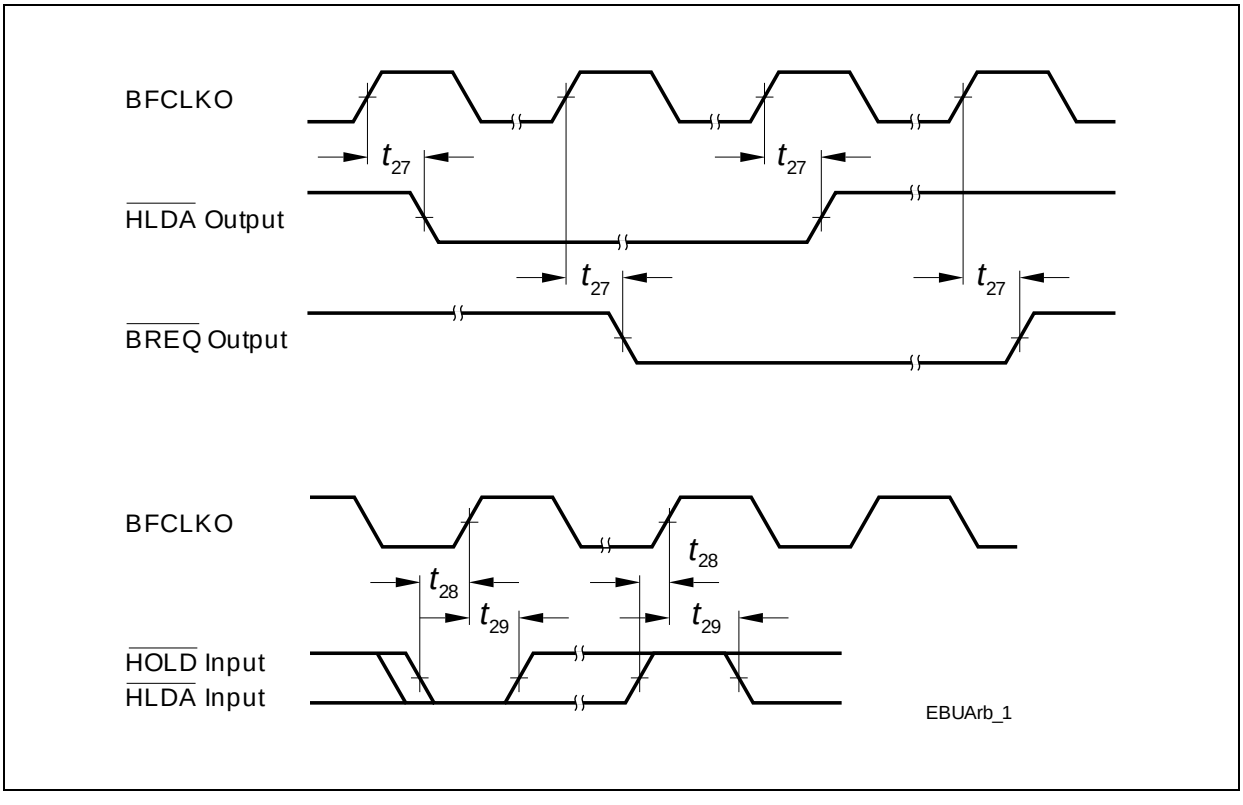

Figure 38 EBU Arbitration Signal Timing

5.4.2 Package Outline

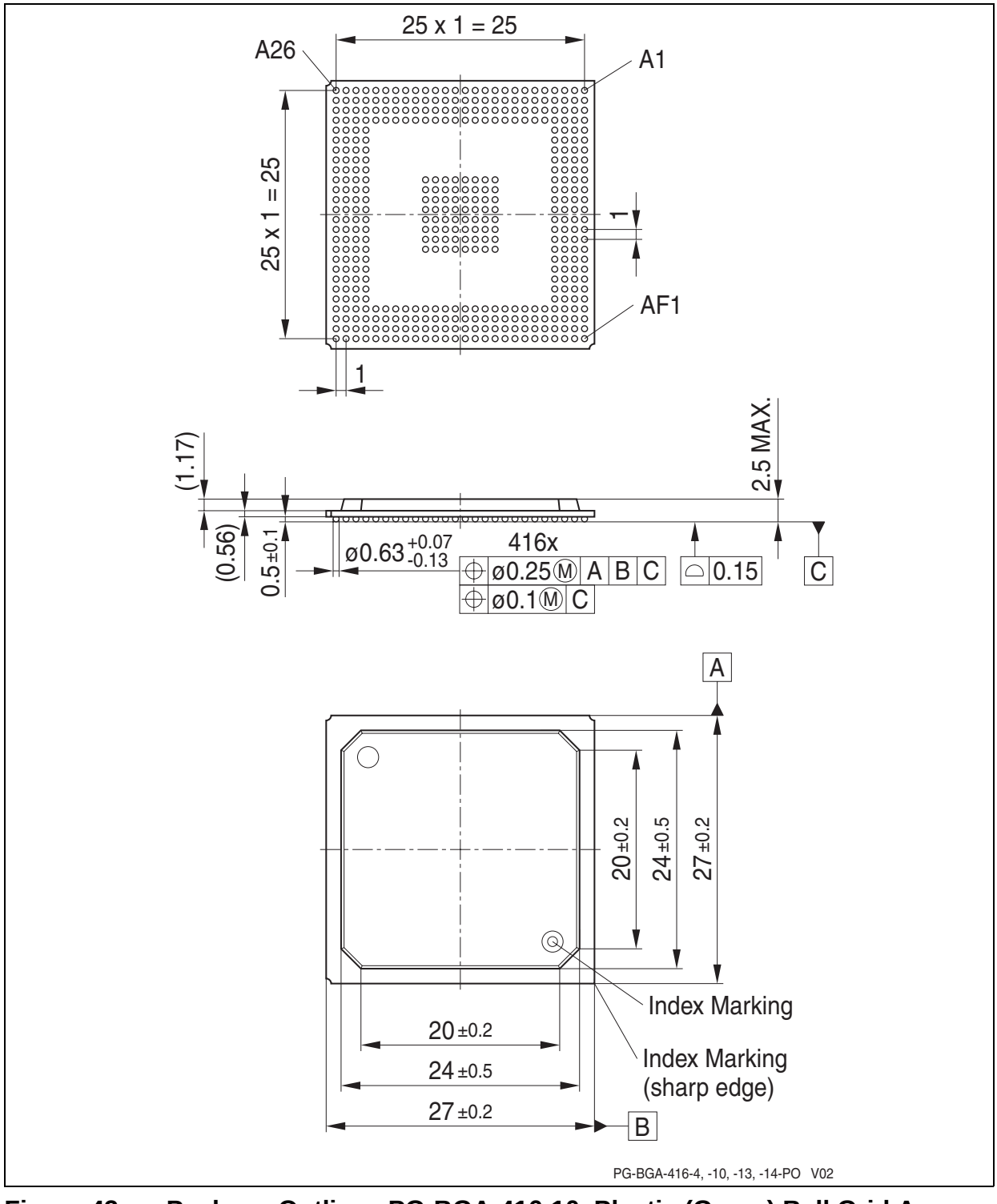

Figure 43 Package Outlines PG-BGA-416-10, Plastic (Green) Ball Grid Array