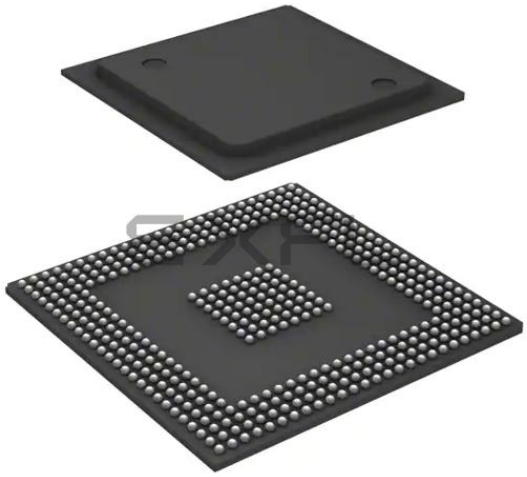
Infineon Technologies - TC1197256F180EACKXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	TriCore™
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	ASC, CANbus, EBI/EMI, MLI, MSC, SSC
Peripherals	DMA, POR, WDT
Number of I/O	219
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	224K x 8
Voltage - Supply (Vcc/Vdd)	1.42V ~ 1.58V
Data Converters	A/D 48x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BBGA
Supplier Device Package	PG-BGA-416-10
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tc1197256f180eackxuma1

Never stop thinking

32-Bit

TC1197

32-Bit Single-Chip Microcontroller

Data Sheet

V1.1 2009-05

Microcontrollers

Table 3 Access Terms

Symbol	Description
U	Access Mode: Access permitted in User Mode 0 or 1.
	Reset Value: Value or bit is not changed by a reset operation.
SV	Access permitted in Supervisor Mode.
R	Read-only register.
32	Only 32-bit word accesses are permitted to this register/address range.
E	Endinit-protected register/address.
PW	Password-protected register/address.
NC	No change, indicated register is not changed.
BE	Indicates that an access to this address range generates a Bus Error.
nBE	Indicates that no Bus Error is generated when accessing this address range, even though it is either an access to an undefined address or the access does not follow the given rules.
nE	Indicates that no Error is generated when accessing this address or address range, even though the access is to an undefined address or address range. True for CPU accesses (MTCR/MFCR) to undefined addresses in the CSFR range.

2.1.5 Abbreviations and Acronyms

The following acronyms and terms are used in this document:

ADC	Analog-to-Digital Converter
AGPR	Address General Purpose Register
ALU	Arithmetic and Logic Unit
ASC	Asynchronous/Synchronous Serial Controller
BCU	Bus Control Unit
BROM	Boot ROM & Test ROM
CAN	Controller Area Network
CMEM	PCP Code Memory
CISC	Complex Instruction Set Computing
CPS	CPU Slave Interface
CPU	Central Processing Unit

2.5.6.1 Functionality of GPTA0

The General Purpose Timer Array (GPTA0) provides a set of hardware modules required for high-speed digital signal processing:

- Filter and Prescaler Cells (FPC) support input noise filtering and prescaler operation.
- Phase Discrimination Logic units (PDL) decode the direction information output by a rotation tracking system.
- Duty Cycle Measurement Cells (DCM) provide pulse-width measurement capabilities.
- A Digital Phase Locked Loop unit (PLL) generates a programmable number of GPTA module clock ticks during an input signal's period.
- Global Timer units (GT) driven by various clock sources are implemented to operate as a time base for the associated Global Timer Cells.
- Global Timer Cells (GTC) can be programmed to capture the contents of a Global Timer on an external or internal event. A GTC may also be used to control an external port pin depending on the result of an internal compare operation. GTCs can be logically concatenated to provide a common external port pin with a complex signal waveform.
- Local Timer Cells (LTC) operating in Timer, Capture, or Compare Mode may also be logically tied together to drive a common external port pin with a complex signal waveform. LTCs – enabled in Timer Mode or Capture Mode – can be clocked or triggered by various external or internal events.
- On-chip Trigger and Gating Signals (OTGS) can be configured to provide trigger or gating signals to integrated peripherals.

Input lines can be shared by an LTC and a GTC to trigger their programmed operation simultaneously.

The following list summarizes the specific features of the GPTA units.

Clock Generation Unit

- Filter and Prescaler Cell (FPC)
  - Six independent units
  - Three basic operating modes:
    Prescaler, Delayed Debounce Filter, Immediate Debounce Filter
  - Selectable input sources:
    Port lines, GPTA module clock, FPC output of preceding FPC cell
  - Selectable input clocks:
    GPTA module clock, prescaled GPTA module clock, DCM clock, compensated or uncompensated PLL clock.
  - $f_{GPTA}/2$ maximum input signal frequency in Filter Modes
- Phase Discriminator Logic (PDL)
  - Two independent units
  - Two operating modes (2- and 3- sensor signals)

On-chip Trigger Unit

- 16 on-chip trigger signals

I/O Sharing Unit

- Interconnecting inputs and outputs from internal clocks, FPC, GTC, LTC, ports, and MSC interface

2.5.6.2 Functionality of LTCA2

The Local Timer Cell Array (LTCA2) provides a set of hardware modules required for high-speed digital signal processing:

- Local Timer Cells (LTC) operating in Timer, Capture, or Compare Mode may also be logically tied together to drive a common external port pin with a complex signal waveform. LTCs – enabled in Timer Mode or Capture Mode – can be clocked or triggered by various external or internal events.

The following list summarizes the specific features of the LTCA unit.

The Local Timer Arrays (LTCA2) provides a set of hardware modules required for high-speed digital signal processing:

Signal Generation Unit

- Local Timer Cell (LTC)
  - 32 independent units
  - Three basic operating modes (Timer, Capture and Compare) for 63 units
  - Special compare modes for one unit
  - 16-bit data width
  - f_{GPTA} maximum resolution
  - $f_{GPTA}/2$ maximum input signal frequency

I/O Sharing Unit

- Interconnecting inputs and outputs from internal clocks, LTC, ports, and MSC interface

2.5.7 Analog-to-Digital Converters

The TC1197 includes three Analog to Digital Converter modules (ADC0, ADC1, ADC2) and one Fast Analog to Digital Converter (FADC).

2.5.7.1 ADC Block Diagram

The analog to digital converter module (ADC) allows the conversion of analog input values into discrete digital values based on the successive approximation method.
This module contains 3 independent kernels (ADC0, ADC1, ADC2) that can operate autonomously or can be synchronized to each other. An ADC kernel is a unit used to convert an analog input signal (done by an analog part) and provides means for triggering conversions, data handling and storage (done by a digital part).

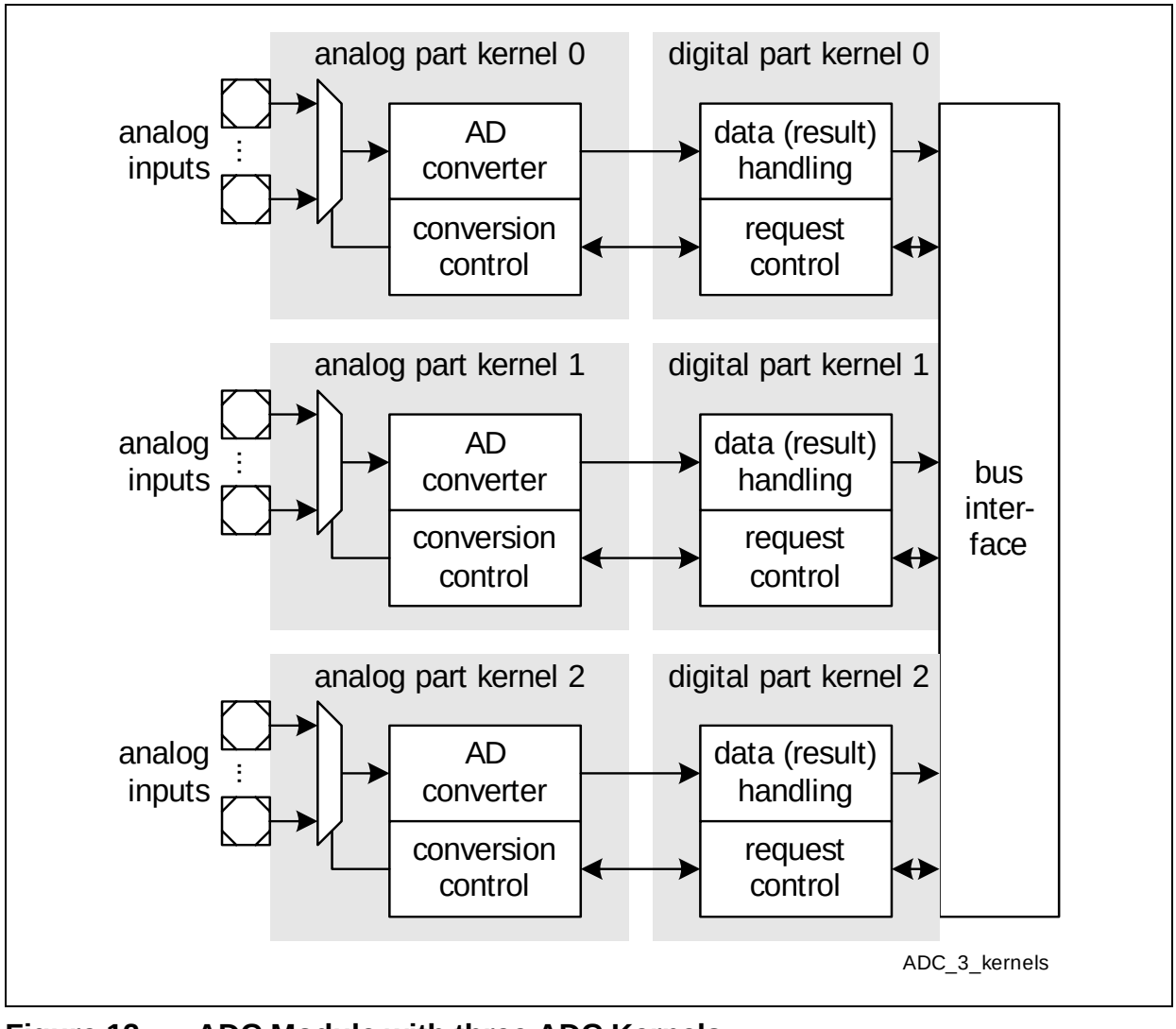

Figure 12 ADC Module with three ADC Kernels

Features of the analog part of each ADC kernel:

2.5.8 External Bus Interface

The External Bus Unit (EBU) of the TC1197 controls the accesses from peripheral units to external memories.

Features:

- 64-bit internal LMB interface
- 32-bit demultiplexed / 16-bit multiplexed external bus interface (3.3V, 2.5V)
  - Support for Intel-style and Motorola-style interface signals
  - Support for Burst Flash memory devices
  - Flexibly programmable access parameters
  - Programmable chip select lines
  - Little-endian support
- Examples for memories that has to be supported
  - Burst Flash:
  - Spansion: S29CD016, S29CD032
  - Spansion: S29CL032J1RFAM010 @3,3V
  - ST: M58BW016, M58BW032
  - ST: M58BW032GB B45ZA3T @3,3V
  - Flash (for 16 bit muxed mode):
  - http://www.spansion.com/products/Am29LV160B.html
  - SRAM (for 16 bit muxed mode):
  - http://www.idt.com/products/files/10372/71V016saautomotive.pdf
  - http://213.174.55.51/zmd.biz/pdf/ UL62H1616A.pdf
  - IDT 71V416YS15BEI
- Scalable external bus frequency
  - Derived from LMB frequency (f_{CPU}) divided by 1, 2, 3, or 4
  - Maximum 75 MHz[1)]
- Data buffering supported
  - Code prefetch buffer
  - Read/write buffer

2.6 On-Chip Debug Support (OCDS)

The TC1197 contains resources for different kinds of “debugging”, covering needs from software development to real-time-tuning. These resources are either embedded in specific modules (e.g. breakpoint logic of the TriCore) or part of a central peripheral (known as CERBERUS).

1) Maximum frequency of today available automotive Burst Flash devices.

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
B5	P0.9	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 9**
	Reserved	I		-
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
C6	P0.10	I/O0	A2/ PU	**Port 0 General Purpose I/O Line 10**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
D6	P0.11	I/O0	A2/ PU	**Port 0 General Purpose I/O Line 11**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
C5	P0.12	I/O0	A2/ PU	**Port 0 General Purpose I/O Line 12**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
D5	P0.13	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 13**
	Reserved	I		-
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
A5	P0.14	I/O0	A2/ PU	**Port 0 General Purpose I/O Line 14**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
M1	P1.10	I/O0	A1/ PU	**Port 1 General Purpose I/O Line 10**
	RVALID0A	I		**MLI0 Receive Channel valid Input A**
	OUT66	O1		**OUT66 Line of GPTA0**
	OUT66	O2		**OUT66 Line of GPTA1**
	OUT90	O3		**OUT90 Line of LTCA2**
L4	P1.11	I/O0	A1/ PU	**Port 1 General Purpose I/O Line 11**
	RData0A	I		**MLI0 Receive Channel Data Input A**
	OUT67	O1		**OUT67 Line of GPTA0**
	OUT67	O2		**OUT67 Line of GPTA1**
	OUT91	O3		**OUT91 Line of LTCA2**
P4	P1.12	I/O0	A2/ PU	**Port 1 General Purpose I/O Line 12**
	EXTCLK0	O1		**External Clock Output 0**
	OUT68	O2		**OUT68 Line of GPTA0**
	OUT68	O3		**OUT68 Line of GPTA1**
L3	P1.13	I/O0	A1/ PU	**Port 1 General Purpose I/O Line 13**
	RCLK0B	I		**MLI0 Receive Channel Clock Input B**
	OUT69	O1		**OUT69 Line of GPTA0**
	OUT69	O2		**OUT69 Line of GPTA1**
	OUT93	O3		**OUT93 Line of LTCA2**
L2	P1.14	I/O0	A1/ PU	**Port 1 General Purpose I/O Line 14**
	RVALID0B	I		**MLI0 Receive Channel valid Input B**
	OUT70	O1		**OUT70 Line of GPTA0**
	OUT70	O2		**OUT70 Line of GPTA1**
	OUT94	O3		**OUT94 Line of LTCA2**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
H1	P8.1	I/O0	A1/ PU	**Port 8 General Purpose I/O Line 1**
	IN41	I		**I/O Line of GPTA0**
	IN41	I		**I/O Line of GPTA1**
	TREADY1A	I		**MLI1 Transmit Channel ready Input A**
	OUT41	O1		**I/O Line of GPTA0**
	OUT41	O2		**I/O Line of GPTA1**
	Reserved	O3		**-**
J3	P8.2	I/O0	A2/ PU	**Port 8 General Purpose I/O Line 2**
	IN42	I		**I/O Line of GPTA0**
	IN42	I		**I/O Line of GPTA1**
	OUT42	O1		**I/O Line of GPTA0**
	OUT42	O2		**I/O Line of GPTA1**
	TVALID1A	O3		**MLI1 Transmit Channel valid Output A**
J2	P8.3	I/O0	A2/ PU	**Port 8 General Purpose I/O Line 3**
	IN43	I		**I/O Line of GPTA0**
	IN43	I		**I/O Line of GPTA1**
	OUT43	O1		**I/O Line of GPTA0**
	OUT43	O2		**I/O Line of GPTA1**
	TData1	O3		**MLI1 Transmit Channel Data Output A**
J1	P8.4	I/O0	A1/ PU	**Port 8 General Purpose I/O Line 4**
	IN44	I		**I/O Line of GPTA0**
	IN44	I		**I/O Line of GPTA1**
	RCLK1A	I		**MLI1 Receive Channel Clock Input A**
	OUT44	O1		**I/O Line of GPTA0**
	OUT44	O2		**I/O Line of GPTA1**
	Reserved	O3		**-**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
A19	P9.0	I/O0	A2/ PU	**Port 9 General Purpose I/O Line 0**
	IN48	I		**I/O Line of GPTA0**
	IN48	I		**I/O Line of GPTA1**
	OUT48	O1		**I/O Line of GPTA0**
	OUT48	O2		**I/O Line of GPTA1**
	EN12	O3		**MSC1 Device Select Output 2**
B19	P9.1	I/O0	A2/ PU	**Port 9 General Purpose I/O Line 1**
	IN49	I		**I/O Line of GPTA0**
	IN49	I		**I/O Line of GPTA1**
	OUT49	O1		**I/O Line of GPTA0**
	OUT49	O2		**I/O Line of GPTA1**
	EN11	O3		**MSC1 Device Select Output 1**
B20	P9.2	I/O0	A2/ PU	**Port 9 General Purpose I/O Line 2**
	IN50	I		**I/O Line of GPTA0**
	IN50	I		**I/O Line of GPTA1**
	OUT50	O1		**I/O Line of GPTA0**
	OUT50	O2		**I/O Line of GPTA1**
	SOP1B	O3		**MSC1 serial Data Output**
A20	P9.3	I/O0	A2/ PU	**Port 9 General Purpose I/O Line 3**
	IN51	I		**I/O Line of GPTA0**
	IN51	I		**I/O Line of GPTA1**
	OUT51	O1		**I/O Line of GPTA0**
	OUT51	O2		**I/O Line of GPTA1**
	FCLP1B	O3		**MSC1 Clock Output**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
U24	P13.9	I/O0	B1/ PU	**Port 13 General Purpose I/O Line 9**
	AD9	I		**EBU Address/Data Bus Line 9**
	OUT97	O1		**OUT97 Line of GPTA0**
	OUT97	O2		**OUT97 Line of GPTA1**
	OUT89	O3		**OUT89 Line of LTCA2**
	AD9	O		**EBU Address/Data Bus Line 9**
Y26	P13.10	I/O0	B1/ PU	**Port 13 General Purpose I/O Line 10**
	AD10	I		**EBU Address/Data Bus Line 10**
	OUT98	O1		**OUT98 Line of GPTA0**
	OUT98	O2		**OUT98 Line of GPTA1**
	OUT90	O3		**OUT90 Line of LTCA2**
	AD10	O		**EBU Address/Data Bus Line 10**
AA26	P13.11	I/O0	B1/ PU	**Port 13 General Purpose I/O Line 11**
	AD11	I		**EBU Address/Data Bus Line 11**
	OUT99	O1		**OUT99 Line of GPTA0**
	OUT99	O2		**OUT99 Line of GPTA1**
	OUT91	O3		**OUT91 Line of LTCA2**
	AD11	O		**EBU Address/Data Bus Line 11**
W25	P13.12	I/O0	B1/ PU	**Port 13 General Purpose I/O Line 12**
	AD12	I		**EBU Address/Data Bus Line 12**
	OUT100	O1		**OUT100 Line of GPTA0**
	OUT100	O2		**OUT100 Line of GPTA1**
	OUT92	O3		**OUT92 Line of LTCA2**
	AD12	O		**EBU Address/Data Bus Line 12**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AA25	P14.1	I/O0	B1/ PU	**Port 14 General Purpose I/O Line 1**
	AD17	I		**EBU Address/Data Bus Line 17**
	OUT97	O1		**OUT97 Line of GPTA0**
	OUT97	O2		**OUT97 Line of GPTA1**
	OUT97	O3		**OUT97 Line of LTCA2**
	AD17	O		**EBU Address/Data Bus Line 17**
Y24	P14.2	I/O0	B1/ PU	**Port 14 General Purpose I/O Line 2**
	AD18	I		**EBU Address/Data Bus Line 18**
	OUT98	O1		**OUT98 Line of GPTA0**
	OUT98	O2		**OUT98 Line of GPTA1**
	OUT98	O3		**OUT98 Line of LTCA2**
	AD18	O		**EBU Address/Data Bus Line 18**
AA23	P14.3	I/O0	B1/ PU	**Port 14 General Purpose I/O Line 3**
	AD19	I		**EBU Address/Data Bus Line 19**
	OUT99	O1		**OUT99 Line of GPTA0**
	OUT99	O2		**OUT99 Line of GPTA1**
	OUT99	O3		**OUT99 Line of LTCA2**
	AD19	O		**EBU Address/Data Bus Line 19**
AB25	P14.4	I/O0	B1/ PU	**Port 14 General Purpose I/O Line 4**
	AD20	I		**EBU Address/Data Bus Line 20**
	OUT100	O1		**OUT100 Line of GPTA0**
	OUT100	O2		**OUT100 Line of GPTA1**
	OUT100	O3		**OUT100 Line of LTCA2**
	AD20	O		**EBU Address/Data Bus Line 20**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AE20	P15.11	I/O0	B1/ PU	**Port 15 General Purpose I/O Line 11**
	WAIT	I		**Wait Input for inserting Wait-States**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
AF19	P15.12	I/O0	B1/ PU	**Port 15 General Purpose I/O Line 12**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
	MR/W	O		**Motorola-style Read/Write Control Signal**
AF23	P15.13	I/O0	B1/ PU	**Port 15 General Purpose I/O Line 13**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
	BAA	O		**Burst Address Advance Output**
AF24	P15.14	I/O0	B1/ PU	**Port 15 General Purpose I/O Line 14**
	BFCLKI	I		**Burst FLASH Clock Input (Clock Feedback).**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
AF25	P15.15	I/O0	B2/ PU	**Port 15 General Purpose I/O Line 15**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
	BFCLKO	O		**Burst Mode Flash Clock Output (Non-Differential)**

5.1.2 Pad Driver and Pad Classes Summary

This section gives an overview on the different pad driver classes and its basic characteristics. More details (mainly DC parameters) are defined in the **Section 5.2.1**.

Table 6 Pad Driver and Pad Classes Overview

Class	Power Supply	Type	Sub Class	Speed Grade	Load	Leakage[1)]	Termination
A	3.3 V	LVTTL I/O, LVTTL outputs	**A1** (e.g. GPIO)	6 MHz	100 pF	500 nA	No
			A2 (e.g. serial I/Os)	40 MHz	50 pF	6 µA	Series termination recommended
B	2.375 - 3.6 V[2)]	LVTTL I/O	**B1** (e.g. Ext. Bus Interface)	40 MHz	50 pF	6 µA	No
			B2 (e.g. Bus Clock)	75 MHz	35 pF		Series termination recommended (for f > 25 MHz)
F	3.3 V	LVDS/ CMOS	–	50 MHz	–	–	Parallel termination[3)], 100 Ω ± 10%
DE	5 V	ADC	–	–	–	–	see **Table 11**

1) Values are for T_{Jmax} = 150 °C.

2) AC characteristics for EBU pins are valid for 2.5 V ± 5% and 3.3 V ± 5%.

3) In applications where the LVDS pins are not used (disabled), these pins must be either left unconnected, or properly terminated with the differential parallel termination of 100 Ω ± 10%.

3) The I_{DD} decreases by typically 70 mA if the f_{CPU} is decreased by 50 MHz, at constant T_J = 150°C, for the Realistic Pattern.
The dependency in this range is, at constant junction temperature, linear.
4) Not tested in production separately, verified by design / characterization.
5) This value assumes worst case of reading flash line with all cells erased. In case of 50% cells written with “1” and 50% cells written with “0”, the maximum current drops down to 95 mA.
6) Relevant for the power supply dimensioning, not for thermal considerations.
In case of erase of Data Flash, internal flash array loading effects may generate transient current spikes of up to 15 mA for maximum 5 ms.
7) No GPIO and EBU activity, LVDS off
8) This value is relevant for the power supply dimensioning. The currents caused by the GPIO and EBU activity depend on the particular application and should be added separately. If two Flash modules are programmed in parallel, the current increase is 2 × 24 mA.

5.3.2 Output Rise/Fall Times

Table 17 Output Rise/Fall Times (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Class A1 Pads						
Rise/fall times[1)]	t_{RA1}, t_{FA1}	–	–	50 140 18000 150 550 65000	ns	Regular (medium) driver, 50 pF Regular (medium) driver, 150 pF Regular (medium) driver, 20 nF Weak driver, 20 pF Weak driver, 150 pF Weak driver, 20 000 pF
Class A2 Pads						
Rise/fall times[1)]	t_{RA2}, t_{FA2}	–	–	3.7 7.5 7 18 50 140 18000 150 550 65000	ns	Strong driver, sharp edge, 50 pF Strong driver, sharp edge, 100pF Strong driver, med. edge, 50 pF Strong driver, soft edge, 50 pF Medium driver, 50 pF Medium driver, 150 pF Medium driver, 20 000 pF Weak driver, 20 pF Weak driver, 150 pF Weak driver, 20 000 pF
Class B Pads 3.3V ± 5%						
Rise/fall times[1)2)]	t_{RB}, t_{FB}	–	–	3.0 3.7 7.5	ns	35 pF 50 pF 100 pF
Class B Pads 2.5V ± 5%						
Rise/fall times[1)3)]	t_{RB}, t_{FB}	–	–	3.7 4.6 9.0	ns	35 pF 50 pF 100 pF
Class F Pads						
Rise/fall times	t_{RF1}, t_{RF1}	–	–	2	ns	LVDS Mode
Rise/fall times	t_{RF2}, t_{RF2}	–	–	60	ns	CMOS Mode, 50 pF

1) Not all parameters are subject to production test, but verified by design/characterization and test correlation.

2) Parameter test correlation for V_{DDEBU} = 2.5 V ± 5%

3) Parameter test correlation for V_{DDEBU} = 2.5 V ± 5%

5.3.6 BFCLKO Output Clock Timing

V_{SS} = 0 V;V_{DD} = 1.5 V ± 5%; V_{DDEBU} = 2.5 V ± 5% and 3.3 V ± 5%,;
T_A = -40 °C to +125 °C; C_L = 35 pF

Table 20 BFCLK0 Output Clock Timing Parameters[1)]

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
BFCLKO clock period	t_{BFCLKO}	CC	13.33[2)]	–	–	ns	–
BFCLKO high time	t_5	CC	3	–	–	ns	–
BFCLKO low time	t_6	CC	3	–	–	ns	–
BFCLKO rise time	t_7	CC	–	–	3	ns	–
BFCLKO fall time	t_8	CC	–	–	3	ns	–
BFCLKO duty cycle $t_5/(t_5 + t_6)$[3)]	DC		45	50	55	%	–

1) Not subject to production test, verified by design/characterization.

2) The PLL jitter characteristics add to this value according to the application settings. See the PLL jitter parameters.

3) The PLL jitter is not included in this parameter. If the BFCLKO frequency is equal to f_{CPU}, the K divider has to be regarded.

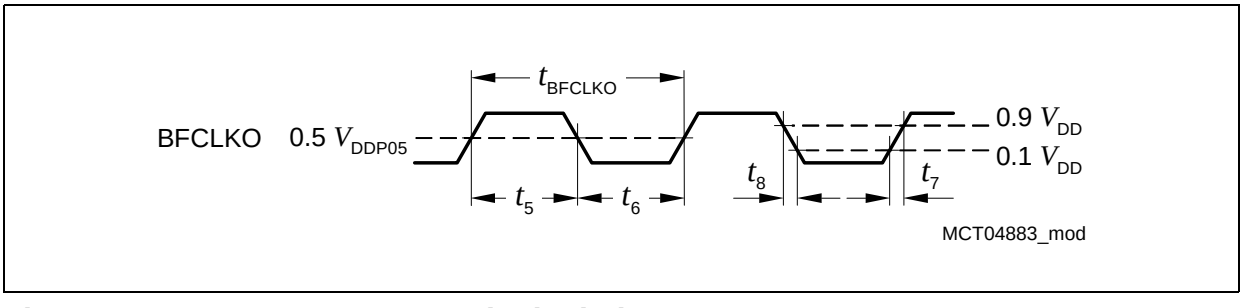

Figure 27 BFCLKO Output Clock Timing

5.3.7 JTAG Interface Timing

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Table 21 JTAG Interface Timing Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK clock period	t_1 SR	25	–	–	ns	–
TCK high time	t_2 SR	12	–	–	ns	–
TCK low time	t_3 SR	10	–	–	ns	–
TCK clock rise time	t_4 SR	–	–	4	ns	–
TCK clock fall time	t_5 SR	–	–	4	ns	–
TDI/TMS setup to TCK rising edge	t_6 SR	6	–	–	ns	–
TDI/TMS hold after TCK rising edge	t_7 SR	6	–	–	ns	–
TDO valid after TCK falling edge[1] (propagation delay)	t_8 CC	–	–	13	ns	C_L = 50 pF
	t_8 CC	–	–	3	ns	C_L = 20 pF
TDO hold after TCK falling edge[1]	t_{18} CC	2	–	–	ns	
TDO high imped. to valid from TCK falling edge[1)2)]	t_9 CC	–	–	14	ns	C_L = 50 pF
TDO valid to high imped. from TCK falling edge[1]	t_{10} CC	–	–	13.5	ns	C_L = 50 pF

1) The falling edge on TCK is used to generate the TDO timing.

2) The setup time for TDO is given implicitly by the TCK cycle time.

5.3.10.3 SSC Master/Slave Mode Timing

Table 30 SSC Master/Slave Mode Timing
(Operating Conditions apply), C_L = 50 pF

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Master Mode Timing							
SCLK clock period	t_{50}	CC	$2 \times T_{SSC}$	–	–	ns	1)2)3)
MTSR/SLSOx delay from SCLK rising edge	t_{51}	CC	0	–	8	ns	–
MRST setup to SCLK falling edge	t_{52}	SR	13	–	–	ns	3)
MRST hold from SCLK falling edge	t_{53}	SR	0	–	–	ns	3)
Slave Mode Timing							
SCLK clock period	t_{54}	SR	$4 \times T_{SSC}$	–	–	ns	1)3)
SCLK duty cycle	t_{55}/t_{54}	SR	45	–	55	%	–
MTSR setup to SCLK latching edge	t_{56}	SR	T_{SSC} + 5	–	–	ns	3)4)
MTSR hold from SCLK latching edge	t_{57}	SR	T_{SSC} + 5	–	–	ns	3)4)
SLSI setup to first SCLK shift edge	t_{58}	SR	T_{SSC} + 5	–	–	ns	3)
SLSI hold from last SCLK latching edge	t_{59}	SR	7	–	–	ns	–
MRST delay from SCLK shift edge	t_{60}	CC	0	–	15	ns	–
SLSI to valid data on MRST	t_{61}	CC	–	–	12	ns	–

1) SCLK signal rise/fall times are the same as the A2 Pads rise/fall times.

2) SCLK signal high and low times can be minimum $1 \times T_{SSC}$.

3) $T_{SSCmin} = T_{SYS} = 1/f_{SYS}$. When f_{SYS} = 90 MHz, t_{50} = 22.2 ns.

4) Fractional divider switched off, SSC internal baud rate generation used.

5.4 Package and Reliability

5.4.1 Package Parameters

Table 31 Thermal Characteristics of the Package

Device	Package	RΘJCT[1)]	RΘJCB[1)]	Unit	Note
TC1197	PG-BGA-416-10	4	6	K/W	

1) The top and bottom thermal resistances between the case and the ambient (R_{TCAT}, R_{TCAB}) are to be combined with the thermal resistances between the junction and the case given above (R_{TJCT}, R_{TJCB}), in order to calculate the total thermal resistance between the junction and the ambient (R_{TJA}). The thermal resistances between the case and the ambient (R_{TCAT}, R_{TCAB}) depend on the external system (PCB, case) characteristics, and are under user responsibility.
The junction temperature can be calculated using the following equation: $T_J = T_A + R_{TJA} \times P_D$, where the R_{TJA} is the total thermal resistance between the junction and the ambient. This total junction ambient resistance R_{TJA} can be obtained from the upper four partial thermal resistances.