Renesas Electronics America Inc - UPD78F0441GB-GAH-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	3-Wire SIO, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	46
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0441gb-gah-ax

CHAPTER 2 PIN FUNCTIONS

2.1 Pin Function List

There are three types of pin I/O buffer power supplies: AV_{REF}[Note 1], V_{LC0}, and V_{DD}. The relationship between these power supplies and the pins is shown below.

Table 2-1. Pin I/O Buffer Power Supplies

Power Supply	Corresponding Pins
AV_{REF}[Note 1]	P20 to P27
V_{LC0}	COM0 to COM7, SEG0 to SEG23, SEG24 to SEG31[Note 2], V_{LC0} to V_{LC3}
V_{DD}	Pins other than above

Notes 1. μPD78F045x and 78F046x only. The power supply is V_{DD} with μPD78F044x.

2. μPD78F044x and 78F045x only.

(1) Port pins **(1/2)**

Function Name	I/O	Function	After Reset	Alternate Function
P11	I/O	Port 1. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	$\overline{SCK10}$
P12				SI10/RxD0/<RxD6>
P13				SO10/TxD0/<TxD6>
P14				INTP4
P20	I/O	Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units.	Digital input port	SEG31[Note 1]/ANI0[Note 2]/DS0−[Note 3]
P21				SEG30[Note 1]/ANI1[Note 2]/DS0+[Note3]
P22				SEG29[Note 1]/ANI2[Note 2]/DS1−[Note3]
P23				SEG28[Note 1]/ANI3[Note 2]/DS1+[Note3]
P24				SEG27[Note 1]/ANI4[Note 2]/DS2−[Note 3]
P25				SEG26[Note 1]/ANI5[Note 2]/DS2+[Note 3]
P26				SEG25[Note 1]/ANI6[Note 2]/REF−[Note 3]
P27				SEG24[Note 1]/ANI7[Note 2]/REF+[Note 3]

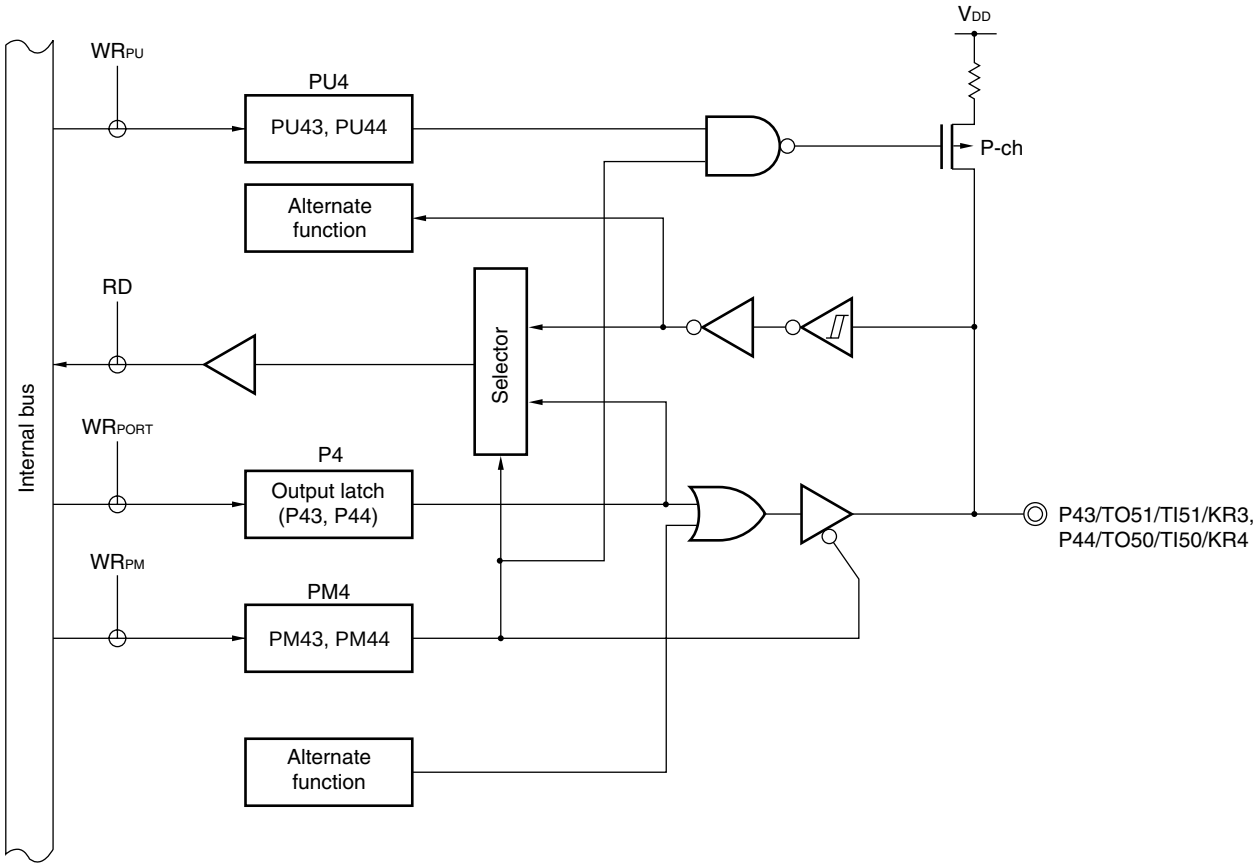
Notes 1. μPD78F044x and 78F045x only.

2. μPD78F045x and 78F046x only.

3. μPD78F046x only.

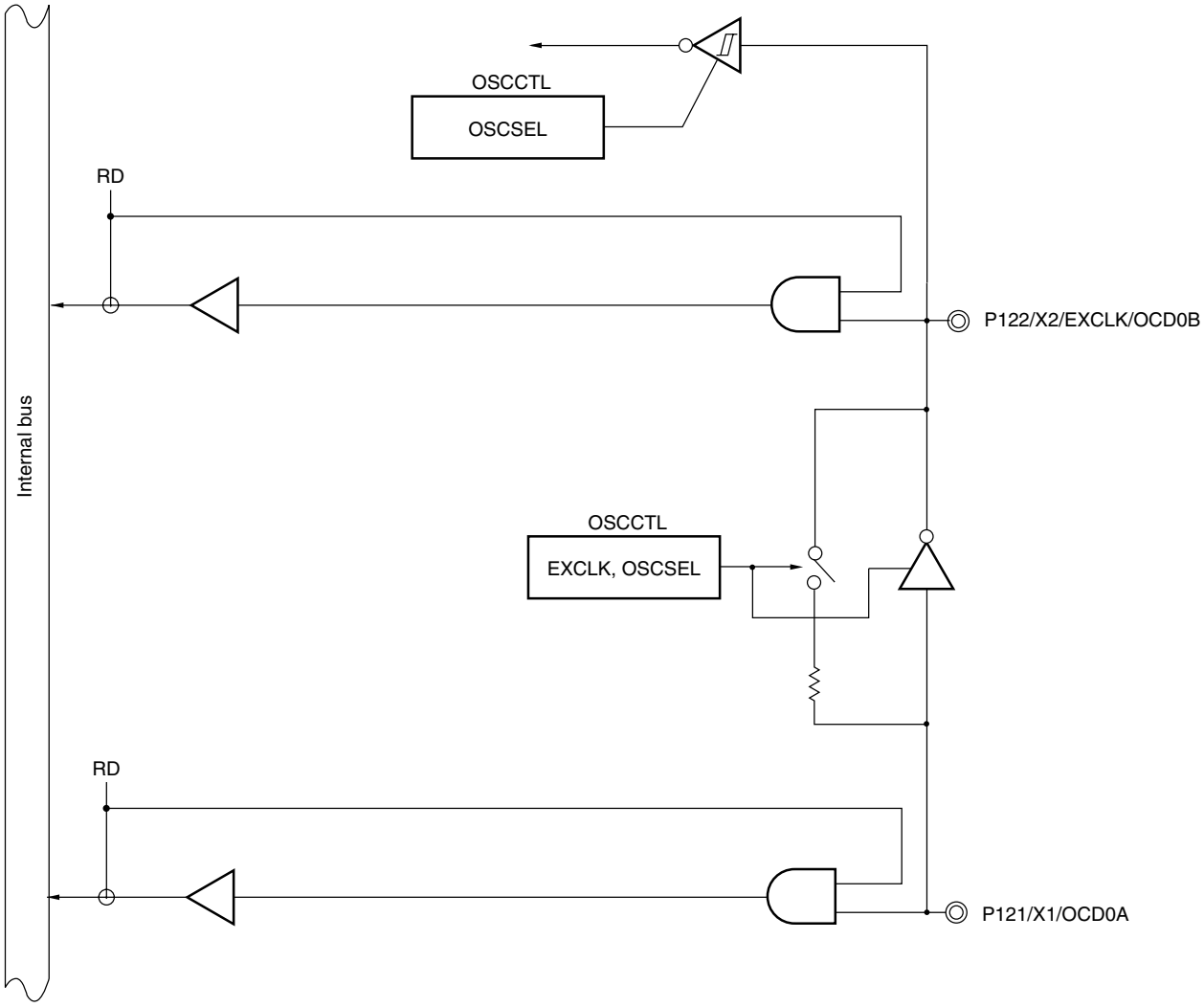
Remark The functions within arrowheads (< >) can be assigned by setting the input switch control register (ISC).

Figure 4-10. Block Diagram of P43 and P44



P4: Port register 4
PU4: Pull-up resistor option register 4
PM4: Port mode register 4
RD: Read signal
WR××: Write signal

Figure 4-17. Block Diagram of P121 and P122



OSCCTL: Clock operation mode select register
RD: Read signal

4.2.9 Port 14

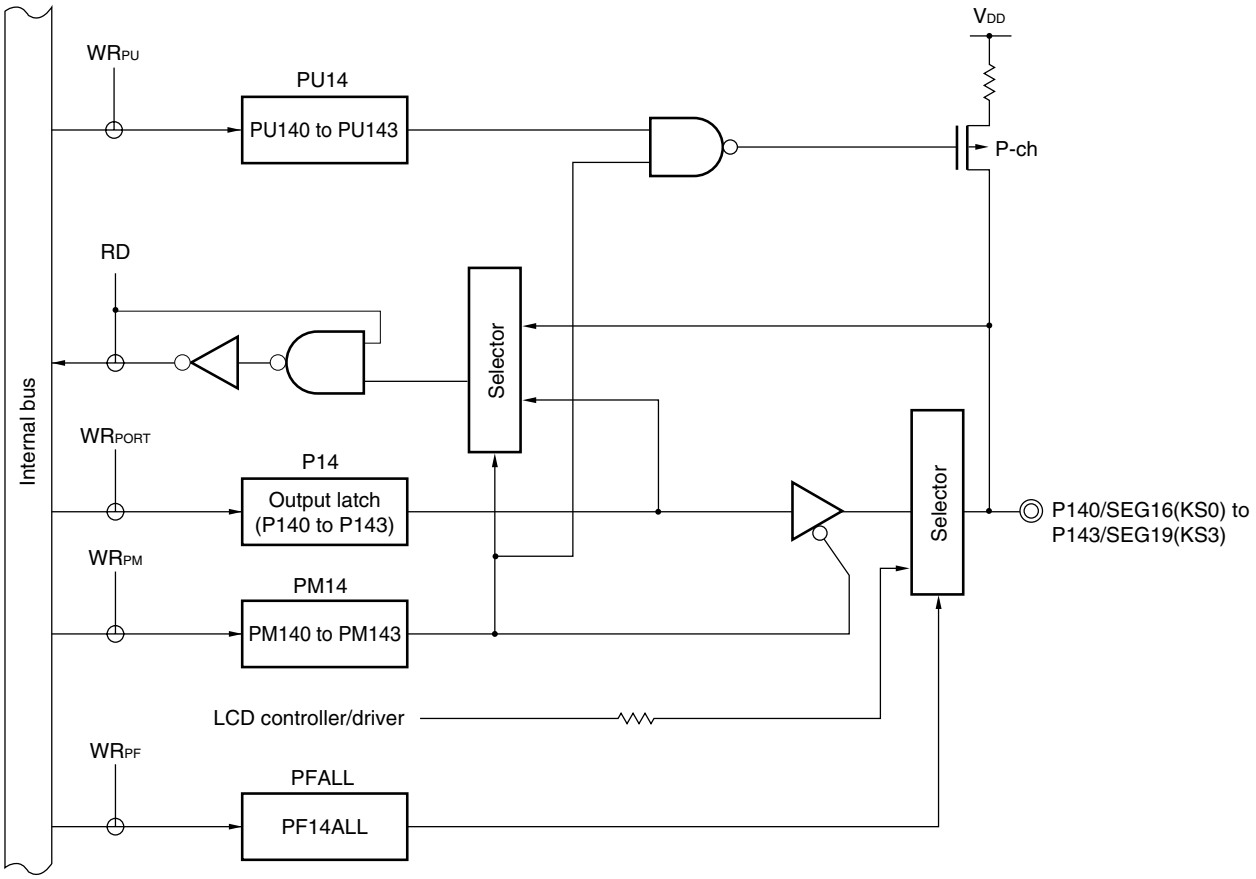
Port 14 is a 4-bit I/O port with an output latch. Port 14 can be set to the input mode or output mode in 1-bit units using port mode register 14 (PM14). When the P140 to P143 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 14 (PU14).

This port can also be used for segment output.

Reset signal generation sets port 14 to input mode.

Figure 4-19 shows a block diagram of port 14.

Figure 4-19. Block Diagram of P140 and P143



P14: Port register 14
PU14: Pull-up resistor option register 14
PM14: Port mode register 14
PFALL: Port function register ALL
RD: Read signal
WR××: Write signal

5.6.10 Peripheral hardware and source clocks

The following lists peripheral hardware and source clocks incorporated in the 78K0/LE3.

Table 5-10. Peripheral Hardware and Source Clocks

Peripheral Hardware \ Source Clock		Peripheral Hardware Clock (f_{PRS})	Subsystem Clock (f_{SUB})	Internal Low-Speed Oscillation Clock (f_{RL})	TM50 Output	TM52 Output	TMH1 Output	External Clock from Peripheral Hardware Pins
16-bit timer/ event counter	00	Y	Y	N	N	Y	N	Y (TI000 pin)[Note]
8-bit timer/ event counter	50	Y	N	N	N	N	N	Y (TI50 pin)[Note]
	51	Y	N	N	N	N	Y	Y (TI51 pin)[Note]
	52	Y	N	N	N	N	N	Y (TI52 pin)[Note]
8-bit timer	H0	Y	N	N	Y	N	N	N
	H1	Y	N	Y	N	N	N	N
	H2	Y	N	N	N	N	N	N
Real-time counter		Y	Y	N	N	N	N	N
Watchdog timer		N	N	Y	N	N	N	N
Buzzer output		Y	N	N	N	N	N	N
Successive approximation type A/D converter		Y	N	N	N	N	N	N
ΔΣ type A/D converter		Y	Y	N	N	N	N	N
Serial interface	UART0	Y	N	N	Y	N	N	N
	UART6	Y	N	N	Y	N	N	N
	CSI10	Y	N	N	N	N	N	Y ($\overline{SCK10}$ pin)[Note]
LCD controller/driver		Y	Y	Y	N	N	N	N
Manchester code generator		Y	N	N	N	N	N	N
Remote controller receiver		Y	Y	N	N	N	N	N

Note When the CPU is operating on the subsystem clock and the internal high-speed oscillation clock has been stopped, do not start operation of these functions on the external clock input from peripheral hardware pins.

Remark Y: Can be selected, N: Cannot be selected

(5) Input switch control register (ISC)

The input source to TI000 becomes the input signal from the P33/TI000 pin, by setting ISC1 to 0.

ISC can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets ISC to 00H.

Figure 6-10. Format of Input Switch Control Register (ISC)

Address: FF4FH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ISC	0	0	ICS5	ICS4	ICS3	ICS2	ICS1	ICS0

ICS5	ICS4	TxD6, RxD6 input source selection
0	0	TxD6:P112, RxD6: P113
1	0	TxD6:P13, RxD6: P12
Other than above		Setting prohibited

ISC3	RxD6/P113 input enabled/disabled
0	RxD6/P113 input disabled
1	RxD6/P113 input enabled

ISC2	TI52 input source control
0	No enable control of TI52 input (P34)
1	Enable controlled of TI52 input (P34)Note 1

ISC1	TI000 input source selection
0	TI000 (P33)
1	RxD6 (P12 or P113Note 2)

ISC0	INTP0 input source selection
0	INTP0 (P120)
1	RxD6 (P12 or P113Note 2)

Notes 1. TI52 input is controlled by TOH2 output signal.

<R> **2.** This is selected by ISC5 and ISC4.

Figure 7-1. Block Diagram of 8-Bit Timer/Event Counter 50

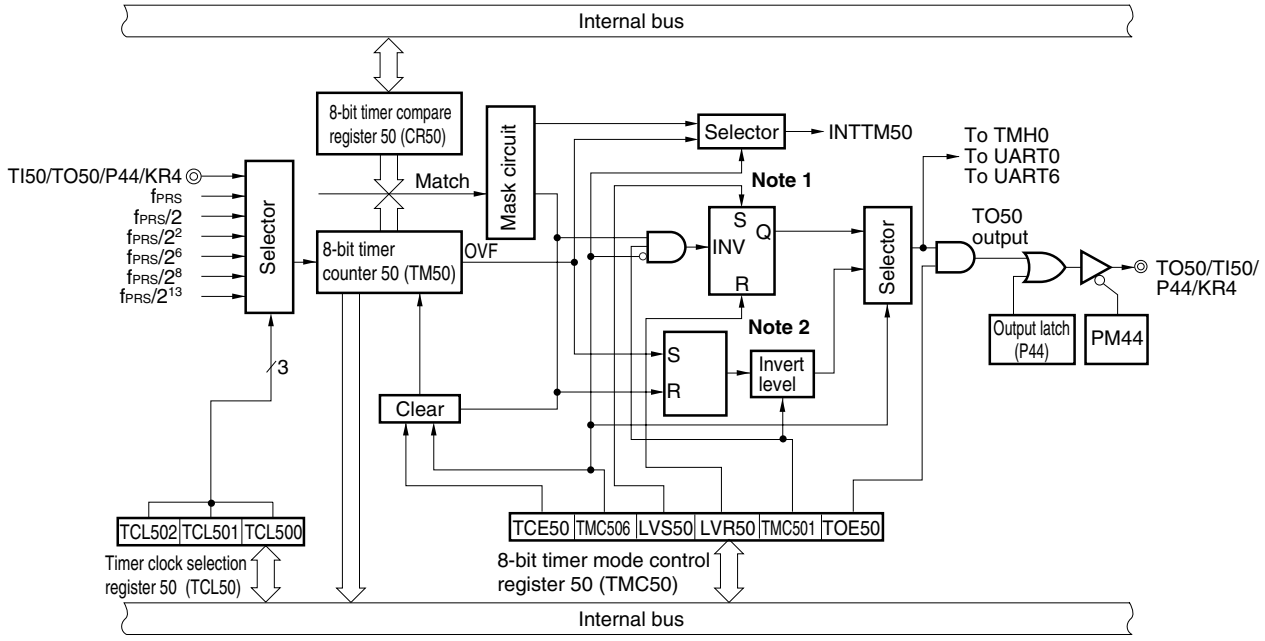
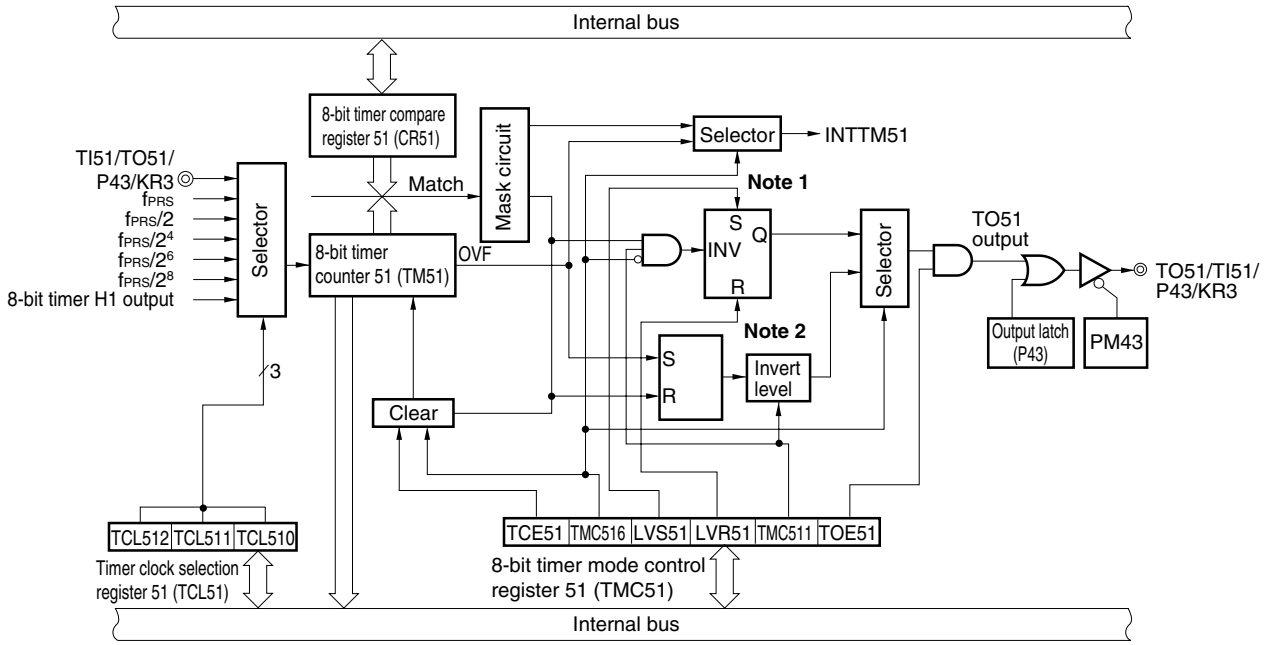


Figure 7-2. Block Diagram of 8-Bit Timer/Event Counter 51



Notes 1. Timer output F/F

2. PWM output F/F

CHAPTER 8 8-BIT TIMERS H0, H1, AND H2

8.1 Functions of 8-Bit Timers H0, H1, and H2

8-bit timers H0, H1, and H2 have the following functions.

- Interval timer
- Square-wave output[Note 1]
- PWM output[Note 2]
- Carrier generator (8-bit timer H1 only)[Note 3]

Notes 1. TMH0 and TMH1 only.

2. However, TOH0 and TOH1 only for TOHn

3. TMH1 only. TM51 and TMH1 can be used in combination as a carrier generator mode.

8.2 Configuration of 8-Bit Timers H0, H1, and H2

8-bit timers H0, H1, and H2 include the following hardware.

Table 8-1. Configuration of 8-Bit Timers H0, H1, and H2

Item	Configuration
Timer register	8-bit timer counter Hn
Registers	8-bit timer H compare register 0n (CMP0n) 8-bit timer H compare register 1n (CMP1n)
Timer output	TOHn[Note 1], output controller
Control registers	8-bit timer H mode register n (TMHMDn) 8-bit timer H carrier control register 1 (TMCYC1)[Note 2] Port mode register 3 (PM3) Port register 3 (P3)

Notes 1. TMH2 does not have an output pin (TOH2). It can only be used as an internal interrupt (INTTMH2) or an external event input enable signal for the TI52 pin.

2. 8-bit timer H1 only

Remark n = 0-2, however, TOH0 and TOH1 only for TOHn

Figures 8-1 and 8-3 show the block diagrams.

8.4.2 Operation as PWM output

In PWM output mode, a pulse with an arbitrary duty and arbitrary cycle can be output.

The 8-bit timer compare register 0n (CMP0n) controls the cycle of timer output (TOHn). Rewriting the CMP0n register during timer operation is prohibited.

The 8-bit timer compare register 1n (CMP1n) controls the duty of timer output (TOHn). Rewriting the CMP1n register during timer operation is possible.

The operation in PWM output mode is as follows.

PWM output (TOHn output) outputs an active level and 8-bit timer counter Hn is cleared to 0 when 8-bit timer counter Hn and the CMP0n register match after the timer count is started. PWM output (TOHn output) outputs an inactive level when 8-bit timer counter Hn and the CMP1n register match.

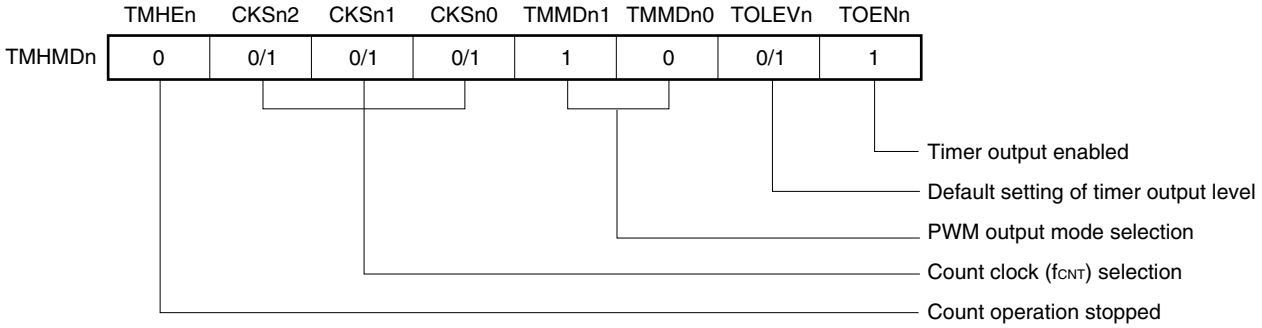
The timer output of TMH2 (PWM output) can only be used as an external event input enable signal of TM52. Note, no pins for external output are available.

Setting

<1> Set each register.

Figure 8-13. Register Setting in PWM Output Mode

(i) Setting timer H mode register n (TMHMDn)



(ii) Setting CMP0n register

- Compare value (N): Cycle setting

(iii) Setting CMP1n register

- Compare value (M): Duty setting

Remarks 1. n = 0 to 2, however, TOH0 and TOH1 only for TOHn

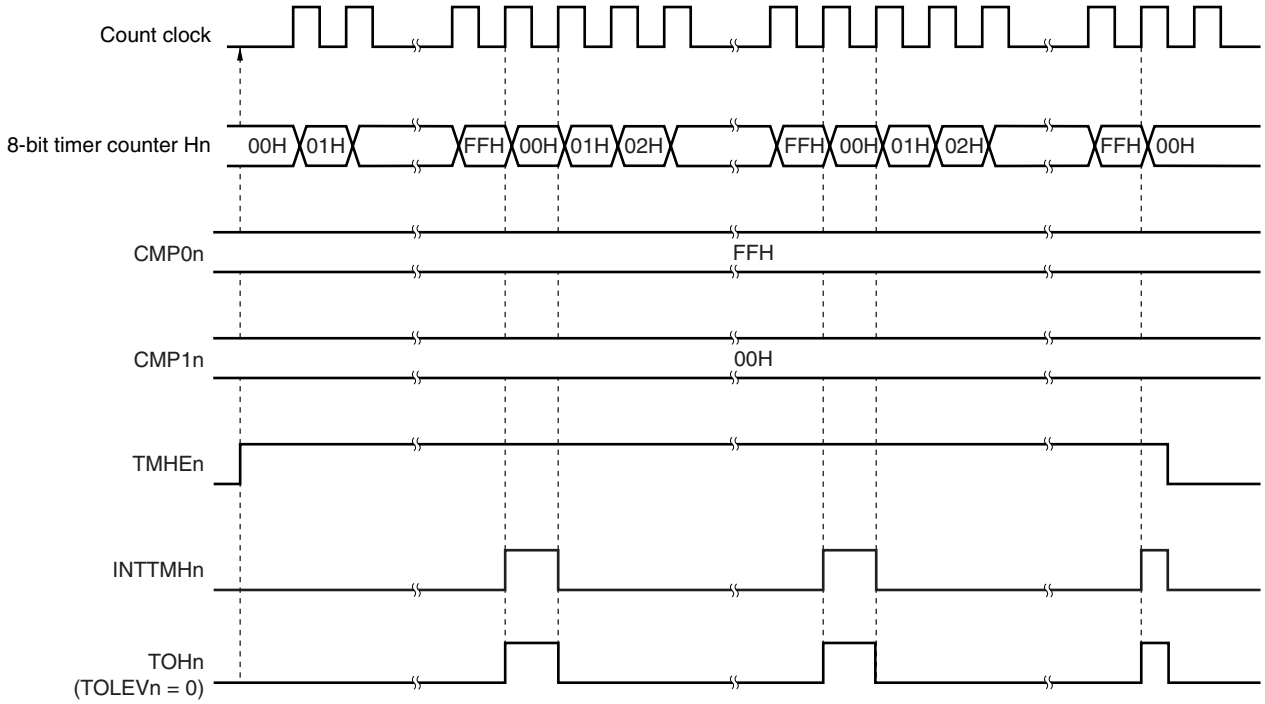
2. 00H ≤ CMP1n (M) < CMP0n (N) ≤ FFH

<2> The count operation starts when TMHEn = 1.

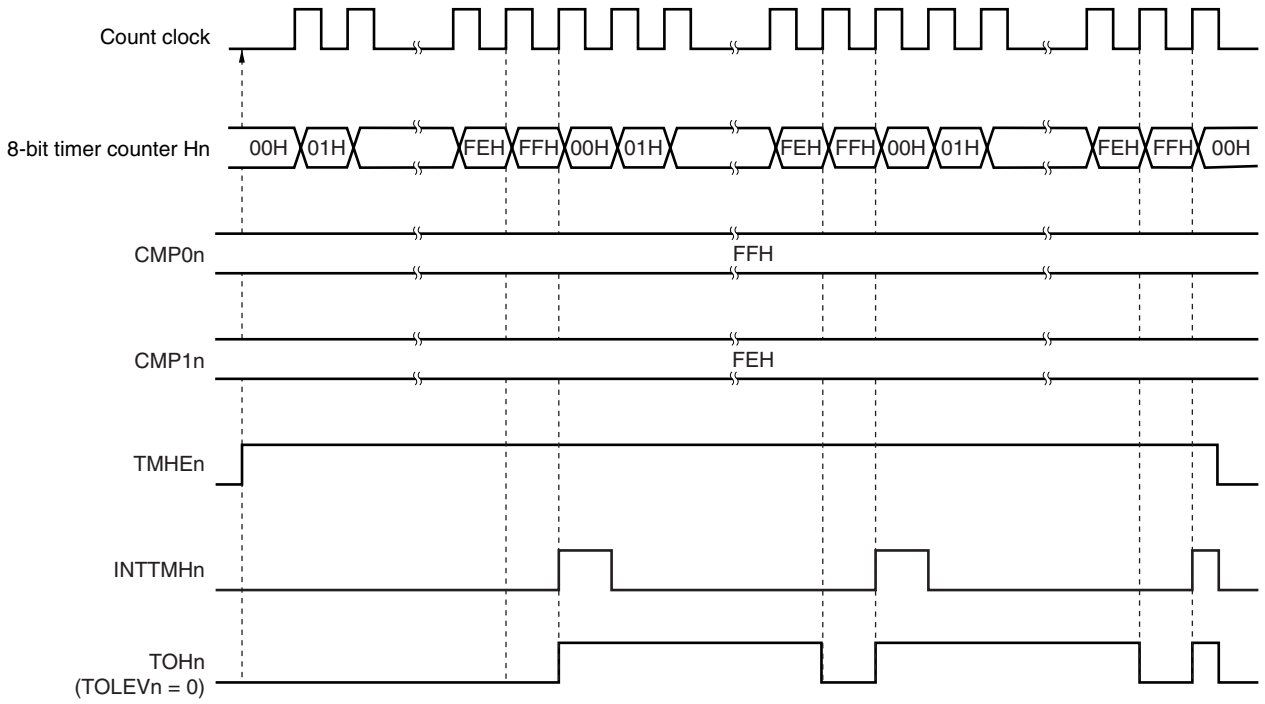
<3> The CMP0n register is the compare register that is to be compared first after counter operation is enabled. When the values of the 8-bit timer counter Hn and the CMP0n register match, the 8-bit timer counter Hn is cleared, an interrupt request signal (INTTMHn) is generated, an active level is output. At the same time, the compare register to be compared with the 8-bit timer counter Hn is changed from the CMP0n register to the CMP1n register.

Figure 8-14. Operation Timing in PWM Output Mode (2/4)

(b) Operation when CMP0n = FFH, CMP1n = 00H



(c) Operation when CMP0n = FFH, CMP1n = FEH



Remark n = 0 to 2, however, TOH0 and TOH1 only for TOHn

8.4.3 Carrier generator operation (8-bit timer H1 only)

In the carrier generator mode, the 8-bit timer H1 is used to generate the carrier signal of an infrared remote controller, and the 8-bit timer/event counter 51 is used to generate an infrared remote control signal (time count).

The carrier clock generated by the 8-bit timer H1 is output in the cycle set by the 8-bit timer/event counter 51.

In carrier generator mode, the output of the 8-bit timer H1 carrier pulse is controlled by the 8-bit timer/event counter 51, and the carrier pulse is output from the TOH1 output.

(1) Carrier generation

In carrier generator mode, the 8-bit timer H compare register 01 (CMP01) generates a low-level width carrier pulse waveform and the 8-bit timer H compare register 11 (CMP11) generates a high-level width carrier pulse waveform.

Rewriting the CMP11 register during the 8-bit timer H1 operation is possible but rewriting the CMP01 register is prohibited.

(2) Carrier output control

Carrier output is controlled by the interrupt request signal (INTTM51) of the 8-bit timer/event counter 51 and the NRZB1 and RMC1 bits of the 8-bit timer H carrier control register (TMCYC1). The relationship between the outputs is shown below.

RMC1 Bit	NRZB1 Bit	Output
0	0	Low-level output
0	1	High-level output at rising edge of INTTM51 signal input
1	0	Low-level output
1	1	Carrier pulse output at rising edge of INTTM51 signal input

(4) Real-time counter control register 2 (RTCC2)

The RTCC2 register is an 8-bit register that is used to control the interval interrupt function and the RTCDIV pin.

RTCC2 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 9-5. Format of Real-Time Counter Control Register 2 (RTCC2)

Address: FF8BH After reset: 00H R/W

Symbol	<7>	<6>	<5>	4	3	2	1	0
RTCC2	RINTE	RCLOE2	RCKDIV	0	0	ICT2	ICT1	ICT0

RINTE	ICT2	ICT1	ICT0	Interval interrupt (INTRTCI) selection
0	×	×	×	Interval interrupt is not generated.
1	0	0	0	$2^6/f_{RTC}$ (1.953125 ms)
1	0	0	1	$2^7/f_{RTC}$ (3.90625 ms)
1	0	1	0	$2^8/f_{RTC}$ (7.8125 ms)
1	0	1	1	$2^9/f_{RTC}$ (15.625 ms)
1	1	0	0	$2^{10}/f_{RTC}$ (31.25 ms)
1	1	0	1	$2^{11}/f_{RTC}$ (62.5 ms)
1	1	1	×	$2^{12}/f_{RTC}$ (125 ms)

RCLOE2[Note]	RTCDIV pin output control
0	Output of RTCDIV pin is disabled.
1	Output of RTCDIV pin is enabled.

RCKDIV	Selection of RTCDIV pin output frequency
0	RTCDIV pin outputs 512 Hz (1.95 ms).
1	RTCDIV pin outputs 16.384 kHz (0.061 ms).

Note RCLOE0 and RCLOE2 must not be enabled at the same time.

Cautions 1. Change ICT2, ICT1, and ICT0 when RINTE = 0.

2. When the output from RTCDIV pin is stopped, the output continues after a maximum of two clocks of f_{RTC} and enters the low level. While 512 Hz is output, and when the output is stopped immediately after entering the high level, a pulse of at least one clock width of f_{XT} may be generated.

(11) Month count register (MONTH)

The MONTH register is an 8-bit register that takes a value of 1 to 12 (decimal) and indicates the count value of months.

It counts up when the day counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (32.768 kHz) later. Set a decimal value of 01 to 12 to this register in BCD code. If a value outside this range is set, the register value returns to the normal value after 1 period.

MONTH can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 01H.

Figure 9-12. Format of Month Count Register (MONTH)

Address: FF67H After reset: 01H R/W

Symbol	7	6	5	4	3	2	1	0
MONTH	0	0	0	MONTH10	MONTH8	MONTH4	MONTH2	MONTH1

(12) Year count register (YEAR)

The YEAR register is an 8-bit register that takes a value of 0 to 99 (decimal) and indicates the count value of years.

It counts up when the month counter overflows.

Values 00, 04, 08, …, 92, and 96 indicate a leap year.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (32.768 kHz) later. Set a decimal value of 00 to 99 to this register in BCD code. If a value outside this range is set, the register value returns to the normal value after 1 period.

YEAR can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 9-13. Format of Year Count Register (YEAR)

Address: FF68H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
YEAR	YEAR80	YEAR40	YEAR20	YEAR10	YEAR8	YEAR4	YEAR2	YEAR1

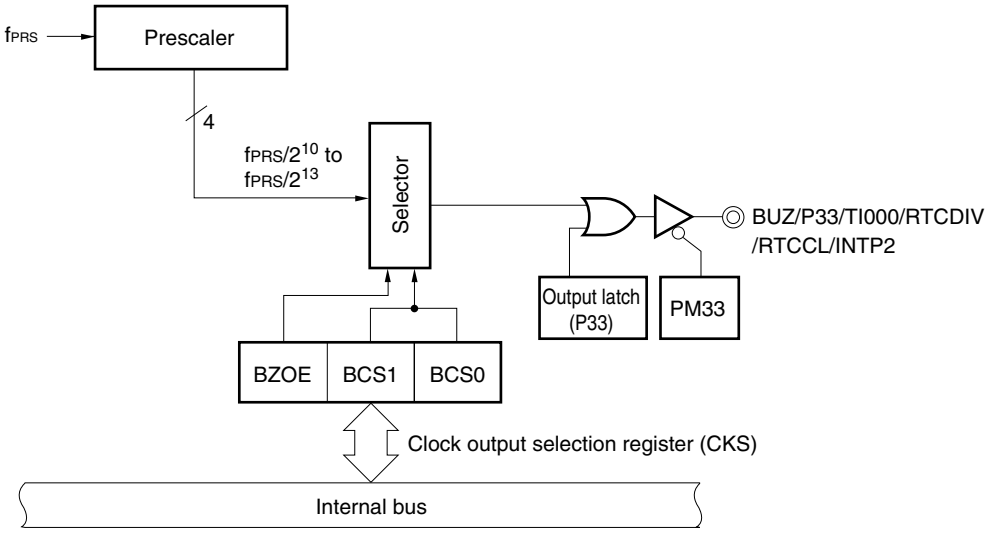
CHAPTER 11 BUZZER OUTPUT CONTROLLER

11.1 Functions of Buzzer Output Controller

The buzzer output is intended for square-wave output of buzzer frequency selected with CKS.

Figure 11-1 shows the block diagram of buzzer output controller.

Figure 11-1. Block Diagram of Buzzer Output Controller



Notes 1. When LCD display is not to be performed or not required, power consumption can be reduced by using the following settings.

<1> Set both SCOC and VAON to 0.

<2> When the internal resistance division method is used, assume MDSET1, MDSET0 = (0, 0). (The current flowing to the internal resistors can be reduced.)

2. This bit is used to control boosting of the internal gate signal of the LCD controller/driver.

If set to "Internal gate voltage boosting", the LCD drive performance can be enhanced.

Set VAON based on the following conditions.

<When set to the static display mode>

- When 2.0 V ≤ V_{LCD} ≤ V_{DD} ≤ 5.5 V: VAON = 0
- When 1.8 V ≤ V_{LCD} ≤ V_{DD} ≤ 3.6 V: VAON = 1

<When set to the 1/3 bias method>

- When 2.5 V ≤ V_{LCD} ≤ V_{DD} ≤ 5.5 V: VAON = 0
- When 1.8 V ≤ V_{LCD} ≤ V_{DD} ≤ 3.6 V: VAON = 1

<When set to the 1/2 bias method or 1/4 bias method >

- When 2.7 V ≤ V_{LCD} ≤ V_{DD} ≤ 5.5 V: VAON = 0
- When 1.8 V ≤ V_{LCD} ≤ V_{DD} ≤ 3.6 V: VAON = 1

3. When using the segment key scan function (KSON = 1), “number of time slices + 1” is added for segment key scan signal output.

4. When the P40/KR0/V_{LC3} pin is set to the 1/4 bias method, it is used as V_{LC3}. When the pin is set to another bias method, it is used for the port function (P40) or the key interrupt function (KR0).

Cautions 1. Bits 3 and 5 must be set to 0.

2. When displaying in a mode with a large number of COMs, such as 8 COM, V_{LC0} may not be able to obtain sufficient contrast under the low-voltage conditions, depending on the panel characteristics. Use the LCD controller/driver after having performed thorough LCD display evaluation and confirmed that there are no problems regarding the display quality.

(b) μPD78F046x

The segment signals correspond to 24 bytes of the LCD display data memory (FA40H to FA57H) during an LCD display period, bits 0, 1, 2, and 3 of each byte are read in synchronization with COM0, COM1, COM2, and COM3, respectively. If a bit is 1, it is converted to the select voltage, and if it is 0, it is converted to the deselect voltage. The conversion results are output to the segment pins (SEG0 to SEG23).

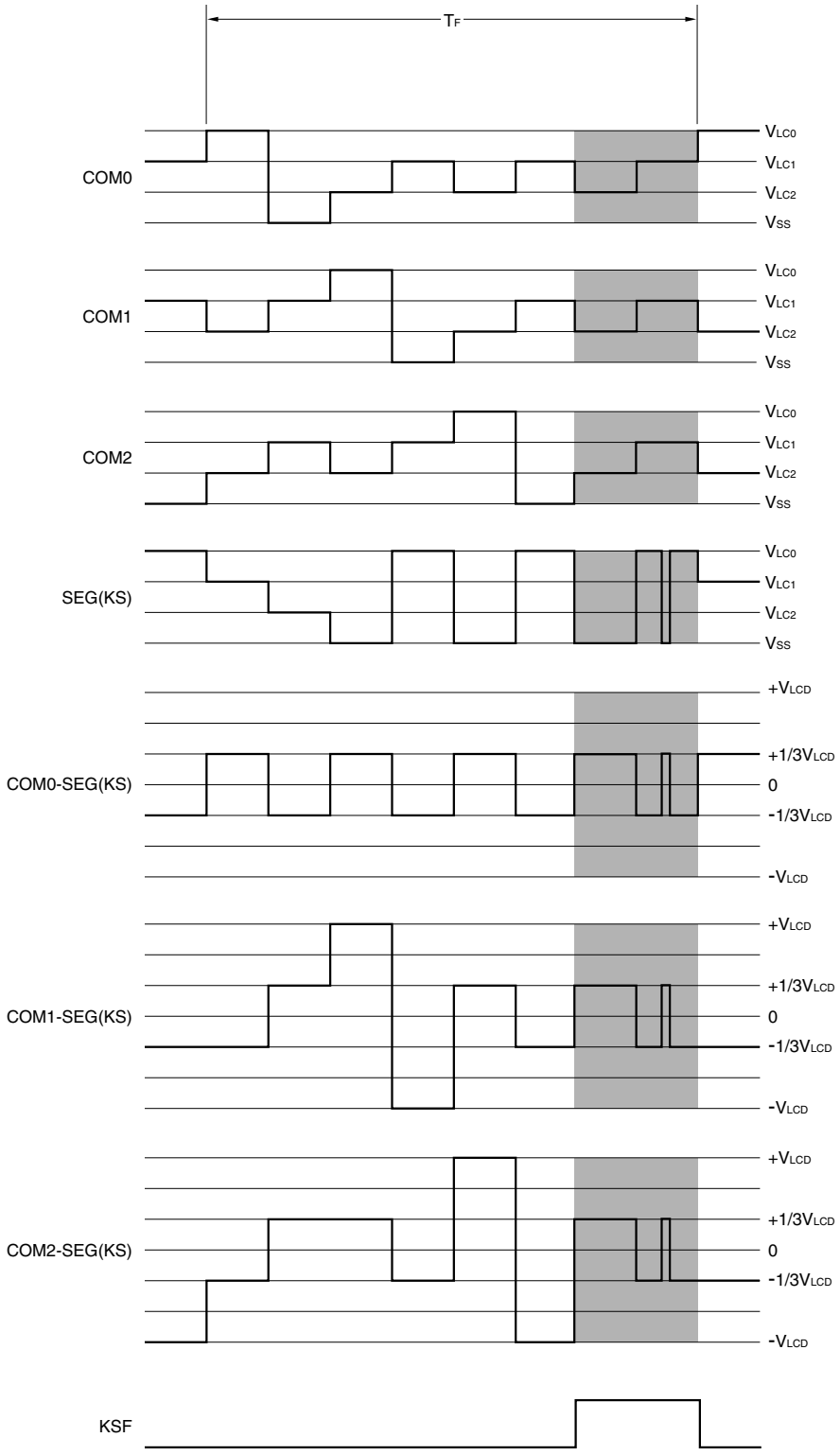
Furthermore, segment signals correspond to the setting values of port registers 14 and 15 during a segment key scan output period. Bits 0 to 3 and bits 4 to 7 of each port register will be read in synchronization with the first half and latter half of the segment key scan output period, respectively, and if the content of each bit is 1 or 0, high levels or low levels will be output to the segment pins (SEG16 to SEG23), respectively.

Check, with the information given above, what combination of front-surface electrodes (corresponding to the segment signals) and rear-surface electrodes (corresponding to the common signals) forms display patterns in the LCD display data memory, and write the bit data that corresponds to the desired display pattern on a one-to-one basis.

LCD display data memory bits 1 to 3, bits 2 and 3, and bit 3 are not used for LCD display in the static display, two-time slot, and three-time slot modes, respectively. So these bits can be used for purposes other than display.

The higher 4 bits of FA40H to FA43H are fixed to 0.

<Key identification>



Shaded sections: Segment key scan output period

Remark During key identification, the residual charge of the LCD panel can be eliminated by outputting a signal with an inverted relationship between its first half and latter half.

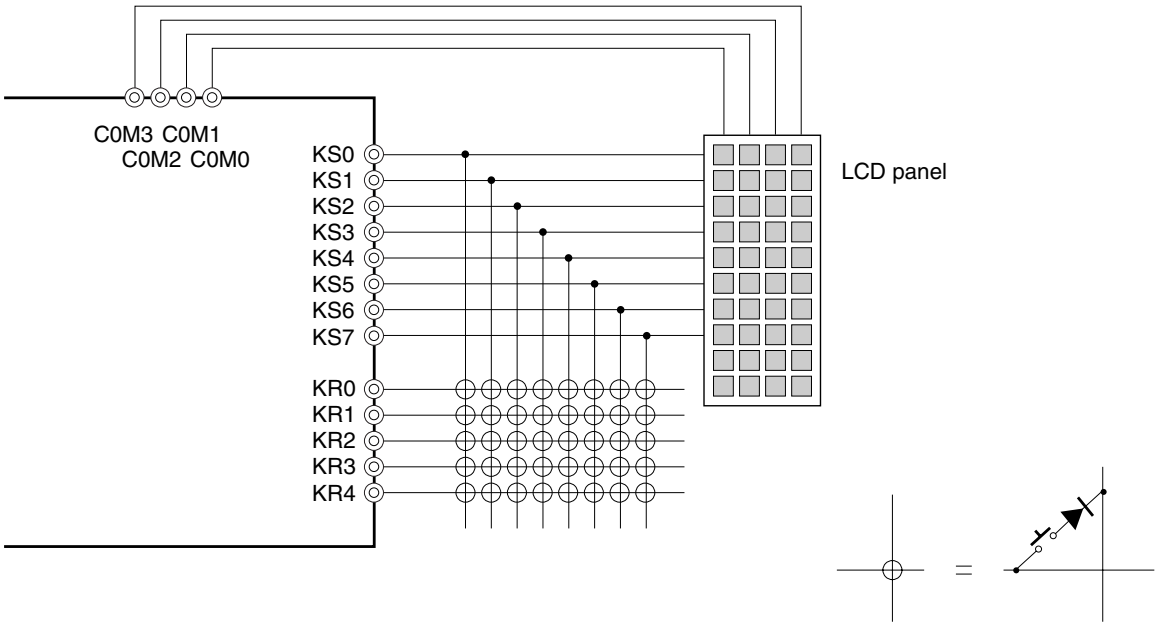
17.8 Operation of Segment Key Scan Function

The segment key scan function is used to reduce the number of pins used by outputting LCD display segment output and key scan signals from the same pin.

Caution This function may affect the LCD panel, depending on how it is used.
Use the function after thorough evaluation.

17.8.1 Circuit configuration example

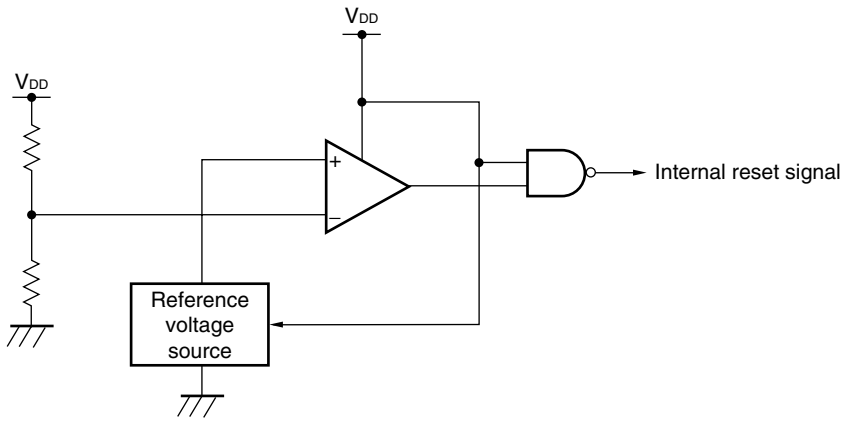
Figure 17-33. Circuit configuration example



24.2 Configuration of Power-on-Clear Circuit

The block diagram of the power-on-clear circuit is shown in Figure 24-1.

Figure 24-1. Block Diagram of Power-on-Clear Circuit



24.3 Operation of Power-on-Clear Circuit

(1) In 1.59 V POC mode (option byte: POCMODE = 0)

- An internal reset signal is generated on power application. When the supply voltage (V_{DD}) exceeds the detection voltage (V_{POC} = 1.59 V ±0.15 V), the reset status is released.
- The supply voltage (V_{DD}) and detection voltage (V_{POC} = 1.59 V ±0.15 V) are compared. When $V_{DD} < V_{POC}$, the internal reset signal is generated. It is released when $V_{DD} \geq V_{POC}$.

(2) In 2.7 V/1.59 V POC mode (option byte: POCMODE = 1)

- An internal reset signal is generated on power application. When the supply voltage (V_{DD}) exceeds the detection voltage (V_{DDPOC} = 2.7 V ±0.2 V), the reset status is released.
- The supply voltage (V_{DD}) and detection voltage (V_{POC} = 1.59 V ±0.15 V) are compared. When $V_{DD} < V_{POC}$, the internal reset signal is generated. It is released when $V_{DD} \geq V_{DDPOC}$.

The timing of generation of the internal reset signal by the power-on-clear circuit and low-voltage detector is shown below.

(2) Low-voltage detection level selection register (LVIS)

This register selects the low-voltage detection level.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

The generation of a reset signal other than an LVI reset clears this register to 00H.

Figure 25-3. Format of Low-Voltage Detection Level Selection Register (LVIS)

Address: FFBFH After reset: 00H[Note] R/W

Symbol	7	6	5	4	3	2	1	0
LVIS	0	0	0	0	LVIS3	LVIS2	LVIS1	LVIS0

LVIS3	LVIS2	LVIS1	LVIS0	Detection level
0	0	0	0	V_{LVI0} (4.24 V ±0.1 V)
0	0	0	1	V_{LVI1} (4.09 V ±0.1 V)
0	0	1	0	V_{LVI2} (3.93 V ±0.1 V)
0	0	1	1	V_{LVI3} (3.78 V ±0.1 V)
0	1	0	0	V_{LVI4} (3.62 V ±0.1 V)
0	1	0	1	V_{LVI5} (3.47 V ±0.1 V)
0	1	1	0	V_{LVI6} (3.32 V ±0.1 V)
0	1	1	1	V_{LVI7} (3.16 V ±0.1 V)
1	0	0	0	V_{LVI8} (3.01 V ±0.1 V)
1	0	0	1	V_{LVI9} (2.85 V ±0.1 V)
1	0	1	0	V_{LVI10} (2.70 V ±0.1 V)
1	0	1	1	V_{LVI11} (2.55 V ±0.1 V)
1	1	0	0	V_{LVI12} (2.39 V ±0.1 V)
1	1	0	1	V_{LVI13} (2.24 V ±0.1 V)
1	1	1	0	V_{LVI14} (2.08 V ±0.1 V)
1	1	1	1	V_{LVI15} (1.93 V ±0.1 V)

Note The value of LVIS is not reset but retained as is, upon a reset by LVI. It is cleared to 00H upon other resets.

Cautions 1. Be sure to clear bits 4 to 7 to "0".

2. Do not change the value of LVIS during LVI operation.

3. When an input voltage from the external input pin (EXLVI) is detected, the detection voltage (V_{EXLVI} = 1.21 V (TYP.)) is fixed. Therefore, setting of LVIS is not necessary.