Renesas Electronics America Inc - UPD78F0443GB-GAH-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	3-Wire SIO, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	46
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0443gb-gah-ax

(2) Non-port pins **(2/3)**

Function Name	I/O	Function	After Reset	Alternate Function
SEG24[Note 1]		LCD controller/driver segment signal outputs	Digital input port	P27/ANI7[Note 2]
SEG25[Note 1]				P26/ANI6[Note 2]
SEG26[Note 1]				P25/ANI5[Note 2]
SEG27[Note 1]				P24/ANI4[Note 2]
SEG28[Note 1]				P23/ANI3[Note 2]
SEG29[Note 1]				P22/ANI2[Note 2]
SEG30[Note 1]				P21/ANI1[Note 2]
SEG31[Note 1]				P20/ANI0[Note 2]
COM0 to COM3	Output	LCD controller/driver common signal outputs	Output	–
COM4 to COM7				SEG0 to SEG3
V_{LC0} to V_{LC2}	–	LCD drive voltage	–	–
V_{LC3}			Input port	P40/KR0
BUZ	Output	Buzzer output	Input port	P33/TI000/RTCDIV /RTCCL/INTP2
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input port	P120/EXLVI
INTP1				P34/TI52/TI010/ TO00/RTC1HZ
INTP2				P33/TI000/RTCDIV /RTCCL/BUZ
INTP3				P31/TOH1
INTP4				P14
<R> KR0	Input	Key interrupt input or segment key scan input	Input port	P40/V_{LC3}
KR1				P41/RIN
KR2				P42
KR3				P43/TO51/TI51
KR4				P44/TO50/TI50
MCGO	Output	Manchester code output	Input port	P32/TOH0
REGC	–	Connecting regulator output (2.4 V) stabilization capacitance for internal operation. Connect to V_{SS} via a capacitor (0.47 to 1 μF: recommended).	–	–
$\overline{\text{RESET}}$	Input	System reset input	–	–
RIN	Input	Remote control reception data input	Input port	P41/KR1
RTCDIV	Output	Real-time counter clock (32 kHz divided frequency) output	Input port	P33/TI000/RTCCL /BUZ/INTP2
RTCCL	Output	Real-time counter clock (32 kHz original oscillation) output	Input port	P33/TI000/RTCDIV /BUZ/INTP2
RTC1HZ	Output	Real-time counter clock (1 Hz) output	Input port	P34/TI52/TI010/ TO00/INTP1

Notes 1. μPD78F044x and 78F045x only.

2. μPD78F045x and 78F046x only.

2.3 Pin I/O Circuits and Recommended Connection of Unused Pins

Table 2-2 shows the types of pin I/O circuits and the recommended connections of unused pins.
See **Figure 2-1** for the configuration of the I/O circuit of each type.

Table 2-2. Pin I/O Circuit Types (1/2)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P11/$\overline{SCK10}$	5-AH	I/O	Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P12/SI10/RxD0/<RxD6>			
P13/SO10/TxD0/<TxD6>			
P14/INTP4			
P20/SEG31/ANI0/DS0- to P27/SEG24/ANI7/REF+ Notes 1, 2, 3, 4	17-R		<Analog setting> Connect to AV_{REF} or AV_{SS}. <Digital setting> Input: Independently connect to AV_{REF} or AV_{SS} via a resistor.[Note 5] Output: Leave open. <Segment setting> Leave open.
P31/TOH1/INTP3	5-AH		Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P32/TOH0/MCGO	5-AG		
P33/TI000/RTCDIV/ RTCCL/BUZ/INTP2	5-AH		
P34/TI52/TI010/TO00/ RTC1HZ/INTP1			
P40/V_{LC3}/KR0	5-AO		
P41/RIN/KR1	5-AH		
P42/KR2			
P43/TO51/TI51/KR3			
P44/TO50/TI50/KR4			
P80/SEG4 to P83/SEG7	17-P		<Port setting> Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open. <Segment setting> Leave open.
P100/SEG8 to P103/SEG11			
P110/SEG16, P111/SEG17			
P112/SEG18/TxD6			
P113/SEG19/RxD6	17-Q		

Notes 1. SEGx is provided to the μPD78F044x and 78F045x only.
2. ANIx is provided to the μPD78F045x and 78F046x only.
3. DSx and REFx are provided to the 78F046x only.
4. P20/SEG31/ANI0/DS0- to P27/SEG24/ANI7/REF+ are set in the digital input mode after release of reset.
5. With μPD78F044x, independently connect to V_{DD} or V_{SS} via a resistor.

Remark The functions within arrowheads (< >) can be assigned by setting the input switch control register (ISC).

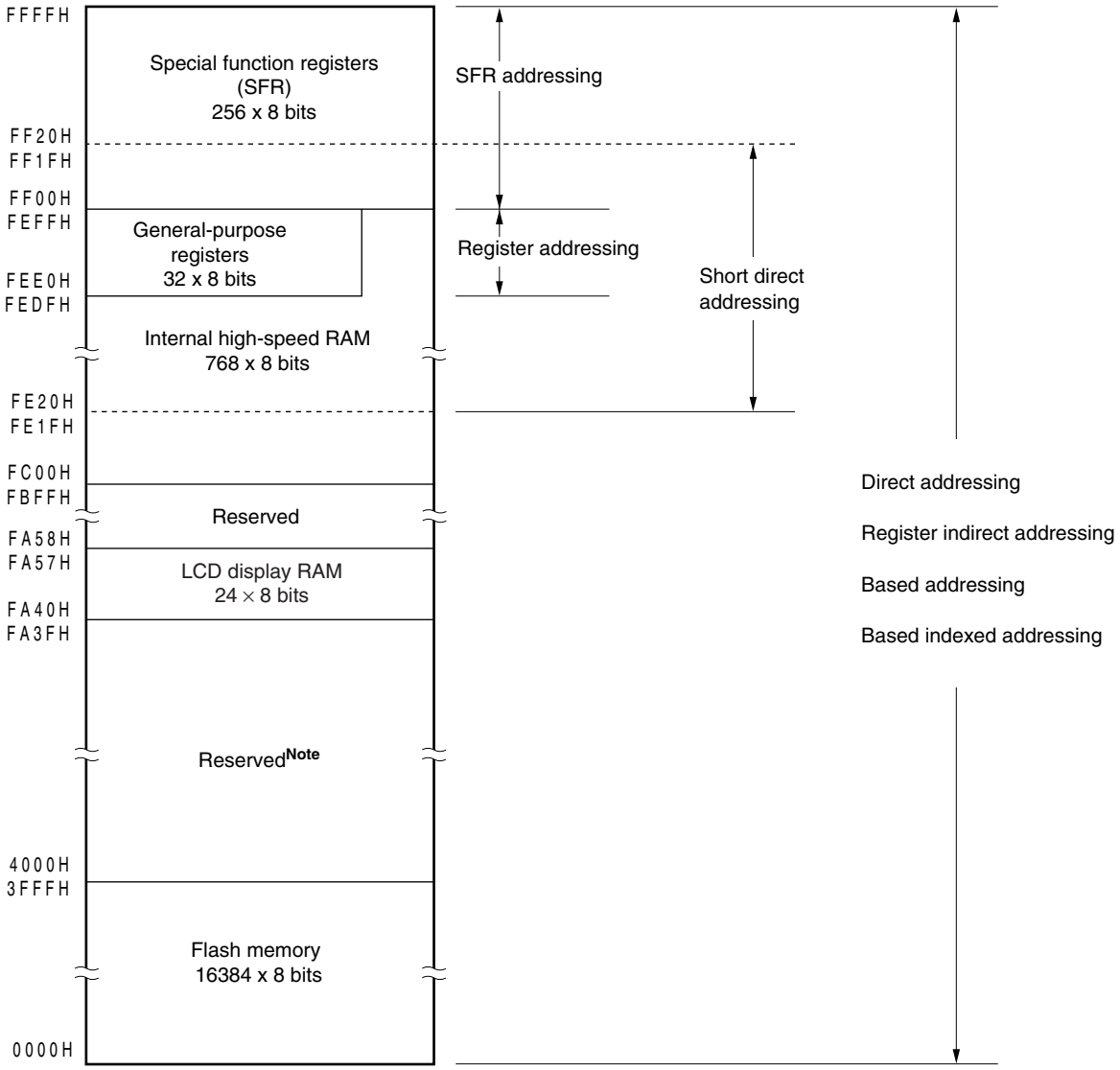
Correspondence between the address values and block numbers in the flash memory are shown below.

Table 3-2. Correspondence Between Address Values and Block Numbers in Flash Memory

Address Value	Block Number	Address Value	Block Number	Address Value	Block Number	Address Value	Block Number
0000H to 03FFH	00H	4000H to 43FFH	10H	8000H to 83FFH	20H	C000H to C3FFH	30H
0400H to 07FFH	01H	4400H to 47FFH	11H	8400H to 87FFH	21H	C400H to C7FFH	31H
0800H to 0BFFH	02H	4800H to 4BFFH	12H	8800H to 8BFFH	22H	C800H to CBFFH	32H
0C00H to 0FFFH	03H	4C00H to 4FFFH	13H	8C00H to 8FFFH	23H	CC00H to CFFFH	33H
1000H to 13FFH	04H	5000H to 53FFH	14H	9000H to 93FFH	24H	D000H to D3FFH	34H
1400H to 17FFH	05H	5400H to 57FFH	15H	9400H to 97FFH	25H	D400H to D7FFH	35H
1800H to 1BFFH	06H	5800H to 5BFFH	16H	9800H to 9BFFH	26H	D800H to DBFFH	36H
1C00H to 1FFFH	07H	5C00H to 5FFFH	17H	9C00H to 9FFFH	27H	DC00H to DFFFH	37H
2000H to 23FFH	08H	6000H to 63FFH	18H	A000H to A3FFH	28H	E000H to E3FFH	38H
2400H to 27FFH	09H	6400H to 67FFH	19H	A400H to A7FFH	29H	E400H to E7FFH	39H
2800H to 2BFFH	0AH	6800H to 6BFFH	1AH	A800H to ABFFH	2AH	E800H to EBFFH	3AH
2C00H to 2FFFH	0BH	6C00H to 6FFFH	1BH	AC00H to AFFFH	2BH	EC00H to EFFFH	3BH
3000H to 33FFH	0CH	7000H to 73FFH	1CH	B000H to B3FFH	2CH		
3400H to 37FFH	0DH	7400H to 77FFH	1DH	B400H to B7FFH	2DH		
3800H to 3BFFH	0EH	7800H to 7BFFH	1EH	B800H to BBFFH	2EH		
3C00H to 3FFFH	0FH	7C00H to 7FFFH	1FH	BC00H to BFFFH	2FH		

Remark μPD78F0441, 78F0451, 78F0461: Block numbers 00H to 0FH
μPD78F0442, 78F0452, 78F0462: Block numbers 00H to 17H
μPD78F0443, 78F0453, 78F0463: Block numbers 00H to 1FH
μPD78F0444, 78F0454, 78F0464: Block numbers 00H to 2FH
μPD78F0445, 78F0455, 78F0465: Block numbers 00H to 3BH

Figure 3-12. Correspondence Between Data Memory and Addressing (μPD78F0461)



<R> **Note** However, FA26H and FA27H can be used (See **13.3 Registers Used in 16-Bit ΔΣ Type A/D Converter**).

3.4.3 Direct addressing

[Function]

The memory to be manipulated is directly addressed with immediate data in an instruction word becoming an operand address.

[Operand format]

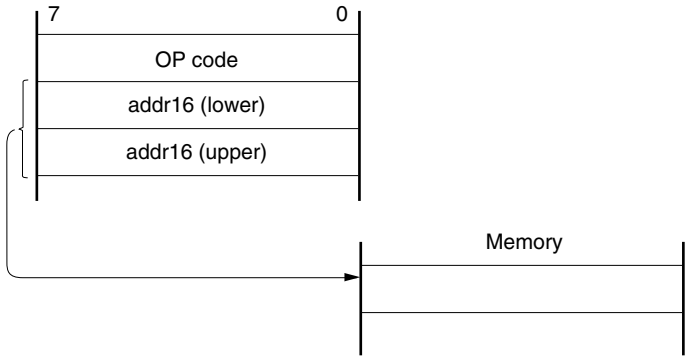
Identifier	Description
addr16	Label or 16-bit immediate data

[Description example]

MOV A, !0FE00H; when setting !addr16 to FE00H

Operation code	1 0 0 0 1 1 1 0	OP code
	0 0 0 0 0 0 0 0	00H
	1 1 1 1 1 1 1 0	FEH

[Illustration]



(3) Operation in clear & start mode by entered TI000 pin valid edge input (CR000: capture register, CR010: compare register)

Figure 6-27. Block Diagram of Clear & Start Mode Entered by TI000 Pin Valid Edge Input (CR000: Capture Register, CR010: Compare Register)

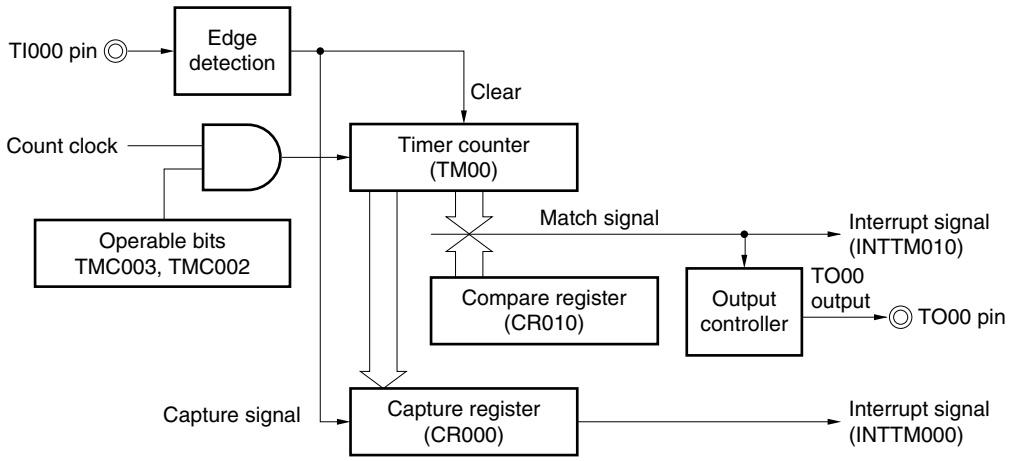
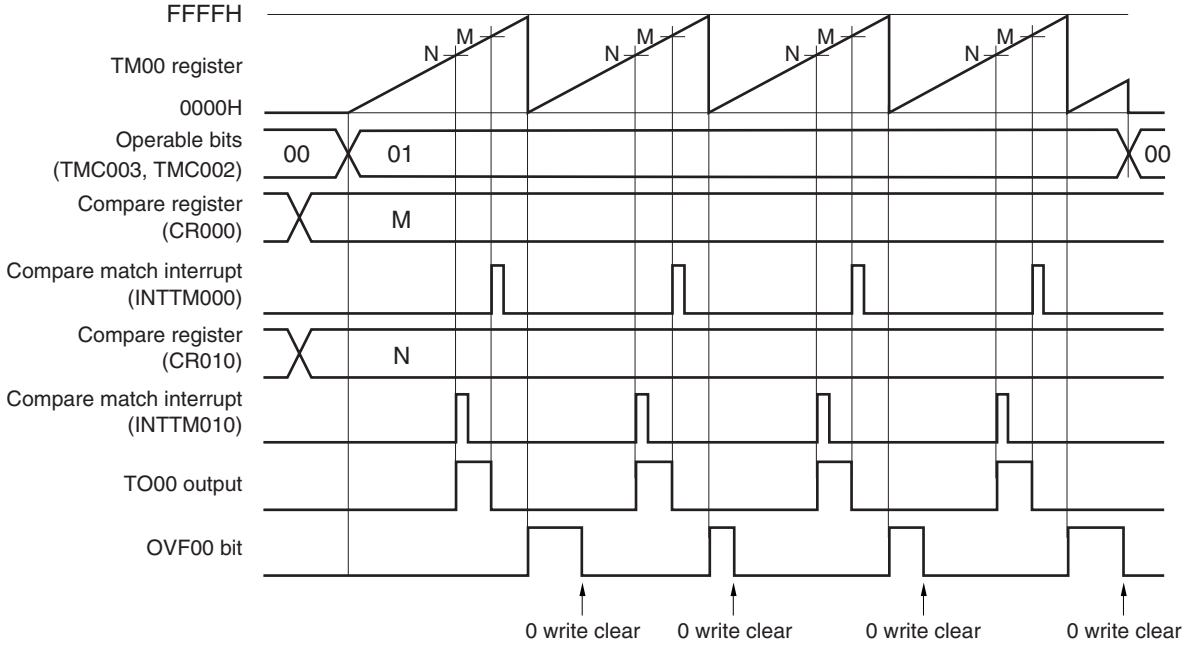


Figure 6-34. Timing Example of Free-Running Timer Mode
(CR000: Compare Register, CR010: Compare Register)

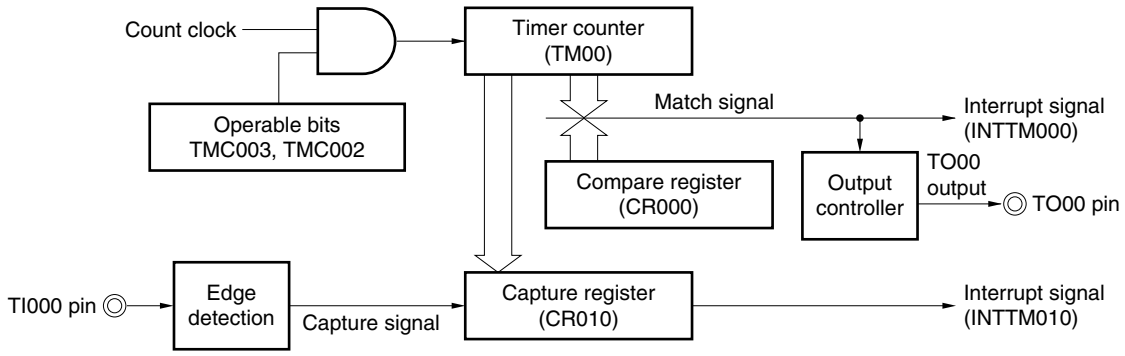
• TOC00 = 13H, PRM00 = 00H, CRC00 = 00H, TMC00 = 04H



This is an application example where two compare registers are used in the free-running timer mode.
The TO00 output level is reversed each time the count value of TM00 matches the set value of CR000 or CR010.
When the count value matches the register value, the INTTM000 or INTTM010 signal is generated.

(2) Free-running timer mode operation
(CR000: compare register, CR010: capture register)

Figure 6-35. Block Diagram of Free-Running Timer Mode
(CR000: Compare Register, CR010: Capture Register)



Setting

<1> Each mode of TM00 and TM52 is set.

(a) Set TM00 as an interval timer. Select TM52 output as the count clock.

- TMC00: Set to operation prohibited.
  (TMC00 = 00000000B)
- CRC00: Set to operation as a compare register.
  (CRC00 = 000000x0B, x = don't care)
- TOC00: Setting TO00 pin output is prohibited upon a match between CR000 and TM00
  (TOC00 = 00000000B)
- PRM00: TM52 output selected as a count clock.
  (PRM00 = 00000111B)
- CR000: Set the compare value to FFFFH.
  If the compare value is set to M, TM00 will only count up to M.
- CR010: Normally, CR010 is not used, however, a compare match interrupt (INTTM010) is generated upon a match between the CR010 setting value and TM00 value. Therefore, mask the interrupt request by using the interrupt mask flag (TMMK010).

(b) Set TM52 as an external event counter.

- TCL52: Edge selection of TI52 pin input
  Falling edge of TI52 pin → TCL52 = 00H
  Rising edge of TI52 pin → TCL52 = 01H
- CR52: Set the compare register value to FFH.
- TMC52: Count operation is stopped.
  (TMC52 = 00000000B)
- TMIF52: Clear this register.

Caution When operating 16-bit timer/event counter 00 as an external 24-bit event counter, INTTM52 must be masked (TMMK52 = 1). Also, the compare register 52 (CR52) value must be set to FFH.

(c) Set TMH2 to the input enable width adjust mode (PWM mode) for the TI52 pin.[Note]

- TMHMD2: Count operation is stopped, the count clock is selected, the mode is set to input enable width adjust mode (PWM mode), the timer output level default value is set to high level, and timer output is set to enable (TMHMD2 = 0xxx1011B, x = set based on usage conditions).
- CMP02: Compare value (N) frequency setting
- CMP12: Compare value (M) duty setting
  Remark 00H ≤ CMP12 (M) < CMP02 (N) ≤ FFH
- ISC2: Set to ISC2 = 1 (TI52 pin input enable controlled)

Note This setting is not required if input enable for the TI52 pin is not controlled.

<2> TM00, TM52, and TMH2 count operation is started. Timer operation must be started in accordance with the following procedure.

(a) Start TM00 counter operation by setting the TMC003 and TMC002 bits to 1 and 1.

(b) Start TM52 counter operation by setting TCE52 to 1.

(c) Start TMH2 counter operation by setting TMHE2 to 1.[Note]

Note This setting is not required if input enable for the TI52 pin is not controlled.

CHAPTER 7 8-BIT TIMER/EVENT COUNTERS 50, 51, AND 52

7.1 Functions of 8-Bit Timer/Event Counters 50, 51, and 52

8-bit timer/event counters 50 and 51 have the following functions.

- Interval timer
- External event counter[Note 1]
- Square-wave output[Note 2]
- PWM output[Note 2]

Notes 1. TM52 and TM00 can be connected in cascade to be used as an external 24-bit event counter. Also, the external event input of TM52 can be input enable-controlled via TMH2. For details, see **CHAPTER 6 16-BIT TIMER/EVENT COUNTER 00**.

2. TM50 and TM51 only.

7.2 Configuration of 8-Bit Timer/Event Counters 50, 51, and 52

8-bit timer/event counters 50, 51, and 52 include the following hardware.

Table 7-1. Configuration of 8-Bit Timer/Event Counters 50, 51, and 52

Item	Configuration
Timer register	8-bit timer counter 5n (TM5n)
Register	8-bit timer compare register 5n (CR5n)
Timer input	TI5n
Timer output	TO50, TO51
Control registers	Timer clock selection register 5n (TCL5n) 8-bit timer mode control register 5n (TMC5n) Input switch control register (ISC) Port mode register 3 (PM3) or port mode register 4 (PM4) Port register 3 (P3) or port register 4 (P4)

Remark n = 0 to 2

Figures 7-1 to 7-3 show the block diagrams of 8-bit timer/event counters 50, 51, and 52.

(4) Port mode registers 3 and 4 (PM3, PM4)

These registers set port 3 and 4 input/output in 1-bit units.

When using the P44/TO50/TI50/KR4 and P43/TO51/TI51/KR3 pins for timer output, clear PM44 and PM43 and the output latches of P44 and P43 to 0.

When using the P44/TO50/TI50/KR4, P43/TO51/TI51/KR3, and P34/TI52/TI010/TO00/RTC1HZ/INTP1 pins for timer input, set PM44, PM43, and PM34 to 1. The output latches of P44, PM43, and PM34 at this time may be 0 or 1.

PM3 and PM4 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

Figure 7-13. Format of Port Mode Register 3 (PM3)

Address: FF23H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM3	1	1	1	PM34	PM33	PM32	PM31	1

PM3n	P1n pin I/O mode selection (n = 1 to 4)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Figure 7-14. Format of Port Mode Register 4 (PM4)

Address: FF24H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM4	1	1	1	PM44	PM43	PM42	PM41	PM40

PM4n	P4n pin I/O mode selection (n = 0 to 4)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Figure 8-7. Format of 8-Bit Timer H Mode Register 1 (TMHMD1)

Address: FF6CH After reset: 00H R/W

	<7>	6	5	4	3	2	<1>	<0>
TMHMD1	TMHE1	CKS12	CKS11	CKS10	TMMD11	TMMD10	TOLEV1	TOEN1

TMHE1	Timer operation enable
0	Stops timer count operation (counter is cleared to 0)
1	Enables timer count operation (count operation started by inputting clock)

CKS12	CKS11	CKS10	Count clock selection[Note 1]			
				f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 10 MHz
0	0	0	f_{PRS}[Note 2]	2 MHz	5 MHz	10 MHz
0	0	1	$f_{PRS}/2^2$	500 kHz	1.25 MHz	2.5 MHz
0	1	0	$f_{PRS}/2^4$	125 kHz	312.5 kHz	625 kHz
0	1	1	$f_{PRS}/2^6$	31.25 kHz	78.13 kHz	156.25 kHz
1	0	0	$f_{PRS}/2^{12}$	0.49 kHz	1.22 kHz	2.44 kHz
1	0	1	$f_{RL}/2^7$	1.88 kHz (TYP.)		
1	1	0	$f_{RL}/2^9$	0.47 kHz (TYP.)		
1	1	1	f_{RL}	240 kHz (TYP.)		

TMMD11	TMMD10	Timer operation mode
0	0	Interval timer mode
0	1	Carrier generator mode
1	0	PWM output mode
1	1	Setting prohibited

TOLEV1	Timer output level control (in default mode)
0	Low level
1	High level

TOEN1	Timer output control
0	Disables output
1	Enables output

Notes 1. If the peripheral hardware clock (f_{PRS}) operates on the high-speed system clock (f_{XH}) (XSEL = 1), the f_{PRS} operating frequency varies depending on the supply voltage.

- V_{DD} = 2.7 to 5.5 V: $f_{PRS} \leq$ 10 MHz
- V_{DD} = 1.8 to 2.7 V: $f_{PRS} \leq$ 5 MHz

2. If the peripheral hardware clock (f_{PRS}) operates on the internal high-speed oscillation clock (f_{RH}) (XSEL = 0), when 1.8 V $\leq V_{DD} <$ 2.7 V, the setting of CKS12 = CKS11 = CKS10 = 0 (count clock: f_{PRS}) is prohibited.

(7) Minute count register (MIN)

The MIN register is an 8-bit register that takes a value of 0 to 59 (decimal) and indicates the count value of minutes.

It counts up when the second counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (32.768 kHz) later. Set a decimal value of 00 to 59 to this register in BCD code. If a value outside this range is set, the register value returns to the normal value after 1 period.

MIN can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 9-8. Format of Minute Count Register (MIN)

Address: FF63H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
MIN	0	MIN40	MIN20	MIN10	MIN8	MIN4	MIN2	MIN1

(8) Hour count register (HOUR)

The HOUR register is an 8-bit register that takes a value of 00 to 23 or 01 to 12, 21 to 32 (decimal) and indicates the count value of hours.

It counts up when the minute counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (32.768 kHz) later. Set a decimal value of 00 to 23 or 01 to 12, 21 to 32 to this register in BCD code. If a value outside this range is set, the register value returns to the normal value after 1 period.

HOUR can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 12H.

However, the value of this register is 00H if the AMPM bit is set to 1 after reset.

Figure 9-9. Format of Hour Count Register (HOUR)

Address: FF64H After reset: 12H R/W

Symbol	7	6	5	4	3	2	1	0
HOUR	0	0	HOUR20	HOUR10	HOUR8	HOUR4	HOUR2	HOUR1

Caution Bit 5 (HOUR20) of HOUR indicates AM(0)/PM(1) if AMPM = 0 (if the 12-hour system is selected).

(2) LCD display mode register (LCDM)

LCDM specifies whether to enable display operation. It also specifies whether to enable segment pin/common pin output, gate booster circuit control, and the display mode.

LCDM is set using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets LCDM to 00H.

Figure 17-3. Format of LCD Display Mode Register

Address: FFB1H After reset: 00H R/W

Symbol	<7>	<6>	5	<4>	3	2	1	0
LCDM	LCDON	SCOC	0	VAON	0	LCDM2	LCDM1	LCDM0

LCDON	LCD display enable/disable
0	Display off (all segment outputs are deselected.)
1	Display on

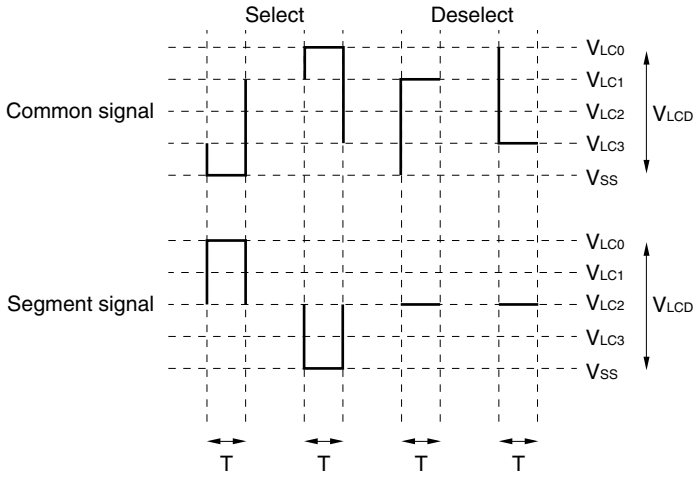
SCOC	Segment pin/common pin output control[Note 1]
0	Output ground level to segment/common pin
1	Output deselect level to segment pin and LCD waveform to common pin

VAON	Gate booster circuit control[Notes 1, 2]
0	No gate voltage boosting
1	Gate voltage boosting

LCDM2	LCDM1	LCDM0	LCD controller/driver display mode selection	
			Resistance division method	
			Number of time slices	Bias mode
1	1	1	8[Note 3]	1/4[Note 4]
0	0	0	4[Note 3]	1/3
0	0	1	3[Note 3]	1/3
0	1	0	2[Note 3]	1/2
0	1	1	3[Note 3]	1/2
1	0	0	Static	
Other than above			Setting prohibited	

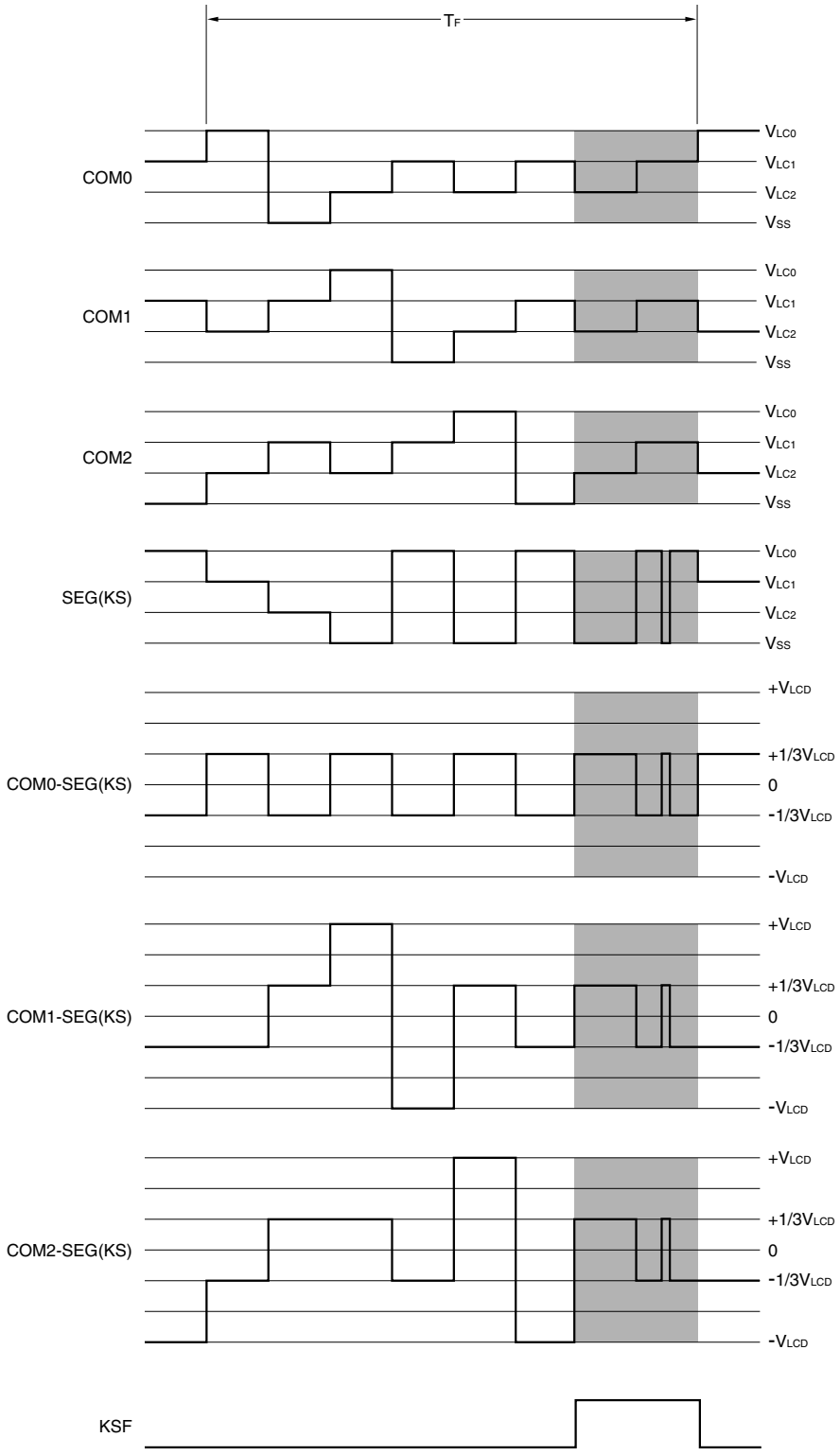
(Note and Caution are listed on the next page.)

(d) 1/4 bias method



T: One LCD clock period

<Key identification>



Shaded sections: Segment key scan output period

Remark During key identification, the residual charge of the LCD panel can be eliminated by outputting a signal with an inverted relationship between its first half and latter half.

(d) Port mode register 3 (PM3)

This register sets port 3 input/output in 1-bit units.

When using the P32/TOH0/MCGO pin for Manchester code output, clear PM32 to 0 and clear the output latch of P32 to 0.

PM3 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

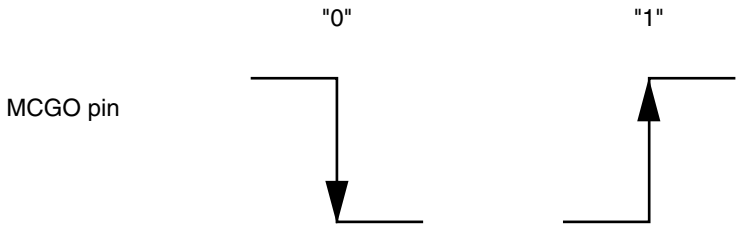
Address: FF23H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM3	1	1	1	PM34	PM33	PM32	PM31	1

PM3n	P3n pin I/O mode selection (n = 1 to 4)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

(2) Format of "0" and "1" of Manchester code output

The format of "0" and "1" of Manchester code output in 78K0/LE3 is as follows.



Cautions 3. When manipulating a flag of the interrupt request flag register, use a 1-bit memory manipulation instruction (CLR1). When describing in C language, use a bit manipulation instruction such as "IF0L.0 = 0;" or "_asm("clr1 IF0L, 0");" because the compiled assembler must be a 1-bit memory manipulation instruction (CLR1).
If a program is described in C language using an 8-bit memory manipulation instruction such as "IF0L &= 0xfe;" and compiled, it becomes the assembler of three instructions.

```
mov a, IF0L
and a, #0FEH
mov IF0L, a
```

In this case, even if the request flag of another bit of the same interrupt request flag register (IF0L) is set to 1 at the timing between "mov a, IF0L" and "mov IF0L, a", the flag is cleared to 0 at "mov IF0L, a". Therefore, care must be exercised when using an 8-bit memory manipulation instruction in C language.

Here is an example of description of the software for setting the option bytes.

```
OPT      CSEG  AT 0080H
OPTION:  DB    30H      ; Enables watchdog timer operation (illegal access detection operation),
                        ; Window open period of watchdog timer: 50%,
                        ; Overflow time of watchdog timer: 2^10/fRL,
                        ; Internal low-speed oscillator can be stopped by software.
         DB    00H      ; 1.59 V POC mode
         DB    00H      ; Reserved area
         DB    00H      ; Reserved area
         DB    00H      ; On-chip debug operation disabled
```

Remark Referencing of the option byte is performed during reset processing. For the reset processing timing, see **CHAPTER 23 RESET FUNCTION**.

29.1.2 Description of operation column

A: A register; 8-bit accumulator
X: X register
B: B register
C: C register
D: D register
E: E register
H: H register
L: L register
AX: AX register pair; 16-bit accumulator
BC: BC register pair
DE: DE register pair
HL: HL register pair
PC: Program counter
SP: Stack pointer
PSW: Program status word
CY: Carry flag
AC: Auxiliary carry flag
Z: Zero flag
RBS: Register bank select flag
IE: Interrupt request enable flag
( ): Memory contents indicated by address or register contents in parentheses
X_H, X_L: Higher 8 bits and lower 8 bits of 16-bit register
$\wedge$: Logical product (AND)
$\vee$: Logical sum (OR)
$\veebar$: Exclusive logical sum (exclusive OR)
$\overline{\ \ }$: Inverted data
addr16: 16-bit immediate data or label
jdisp8: Signed 8-bit data (displacement value)

29.1.3 Description of flag operation column

(Blank): Not affected
0: Cleared to 0
1: Set to 1
×: Set/cleared according to the result
R: Previously saved value is restored

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag		
				Note 1	Note 2		Z	AC	CY
8-bit operation	**SUB**	A, #byte	2	4	–	A, CY ← A – byte	×	×	×
		saddr, #byte	3	6	8	(saddr), CY ← (saddr) – byte	×	×	×
		A, r Note 3	2	4	–	A, CY ← A – r	×	×	×
		r, A	2	4	–	r, CY ← r – A	×	×	×
		A, saddr	2	4	5	A, CY ← A – (saddr)	×	×	×
		A, !addr16	3	8	9	A, CY ← A – (addr16)	×	×	×
		A, [HL]	1	4	5	A, CY ← A – (HL)	×	×	×
		A, [HL + byte]	2	8	9	A, CY ← A – (HL + byte)	×	×	×
		A, [HL + B]	2	8	9	A, CY ← A – (HL + B)	×	×	×
		A, [HL + C]	2	8	9	A, CY ← A – (HL + C)	×	×	×
	SUBC	A, #byte	2	4	–	A, CY ← A – byte – CY	×	×	×
		saddr, #byte	3	6	8	(saddr), CY ← (saddr) – byte – CY	×	×	×
		A, r Note 3	2	4	–	A, CY ← A – r – CY	×	×	×
		r, A	2	4	–	r, CY ← r – A – CY	×	×	×
		A, saddr	2	4	5	A, CY ← A – (saddr) – CY	×	×	×
		A, !addr16	3	8	9	A, CY ← A – (addr16) – CY	×	×	×
		A, [HL]	1	4	5	A, CY ← A – (HL) – CY	×	×	×
		A, [HL + byte]	2	8	9	A, CY ← A – (HL + byte) – CY	×	×	×
		A, [HL + B]	2	8	9	A, CY ← A – (HL + B) – CY	×	×	×
		A, [HL + C]	2	8	9	A, CY ← A – (HL + C) – CY	×	×	×
	AND	A, #byte	2	4	–	A ← A ∧ byte	×		
		saddr, #byte	3	6	8	(saddr) ← (saddr) ∧ byte	×		
		A, r Note 3	2	4	–	A ← A ∧ r	×		
		r, A	2	4	–	r ← r ∧ A	×		
		A, saddr	2	4	5	A ← A ∧ (saddr)	×		
		A, !addr16	3	8	9	A ← A ∧ (addr16)	×		
		A, [HL]	1	4	5	A ← A ∧ (HL)	×		
		A, [HL + byte]	2	8	9	A ← A ∧ (HL + byte)	×		
		A, [HL + B]	2	8	9	A ← A ∧ (HL + B)	×		
		A, [HL + C]	2	8	9	A ← A ∧ (HL + C)	×		

Notes 1. When the internal high-speed RAM area is accessed or for an instruction with no data access

2. When an area except the internal high-speed RAM area is accessed

3. Except “r = A”

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

2. This clock cycle applies to the internal ROM program.