Renesas Electronics America Inc - UPD78F0444GK-GAJ-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	3-Wire SIO, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	46
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0444gk-gaj-ax

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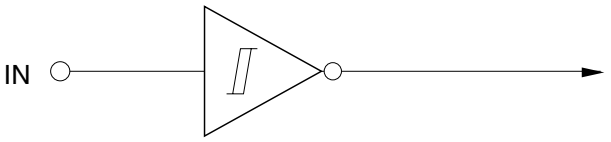
M8E 02. 11-1

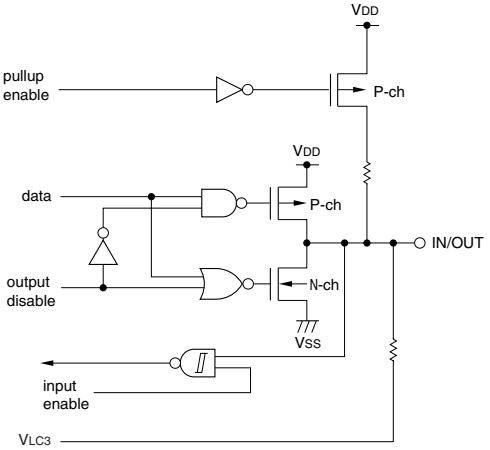
Figure 2-1. Pin I/O Circuit List (1/2)

Type 2

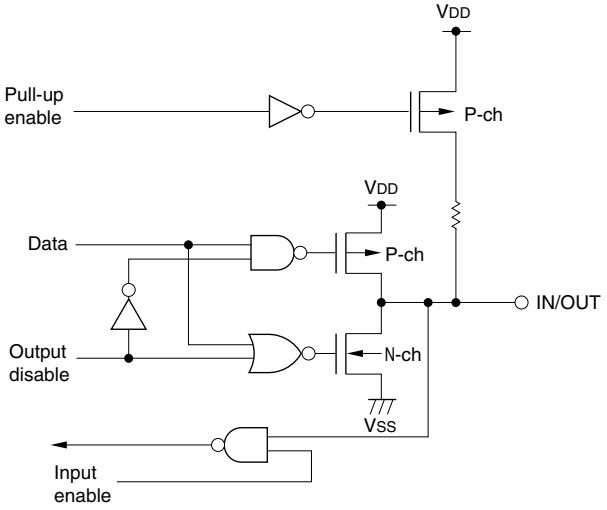


Schmitt-triggered input with hysteresis characteristics

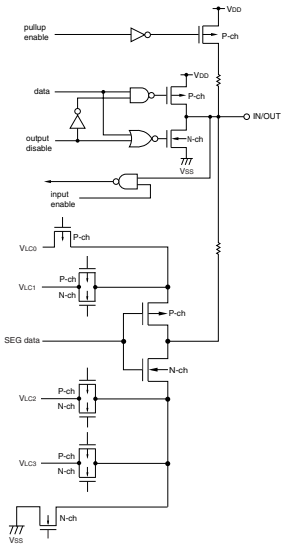
Type 5-AO



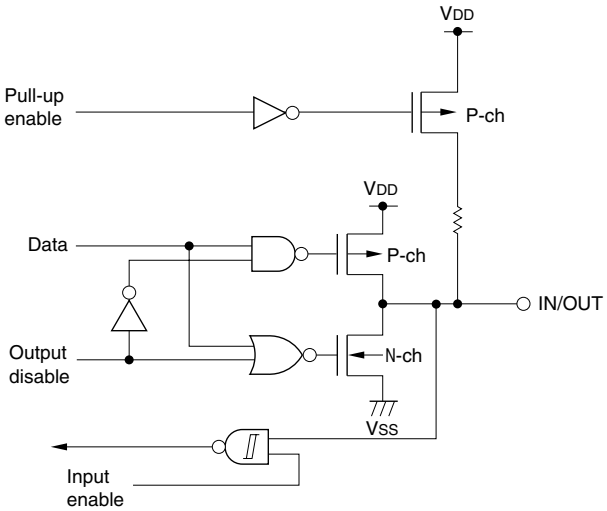
Type 5-AG



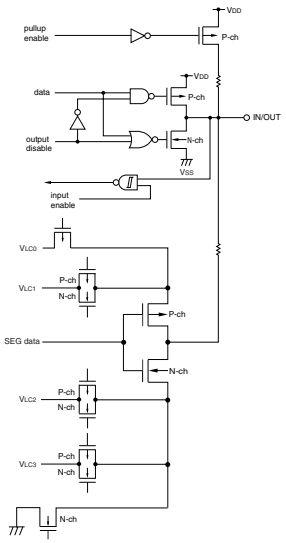
Type 17-P



Type 5-AH



Type 17-Q



3.1.4 Data memory addressing

Addressing refers to the method of specifying the address of the instruction to be executed next or the address of the register or memory relevant to the execution of instructions.

Several addressing modes are provided for addressing the memory relevant to the execution of instructions for the 78K0/LE3, based on operability and other considerations. For areas containing data memory in particular, special addressing methods designed for the functions of special function registers (SFR) and general-purpose registers are available for use. Figures 3-11 to 3-20 show correspondence between data memory and addressing. For details of each addressing mode, see **3.4 Operand Address Addressing**.

Figure 3-11. Correspondence Between Data Memory and Addressing (μPD78F0441, 78F0451)

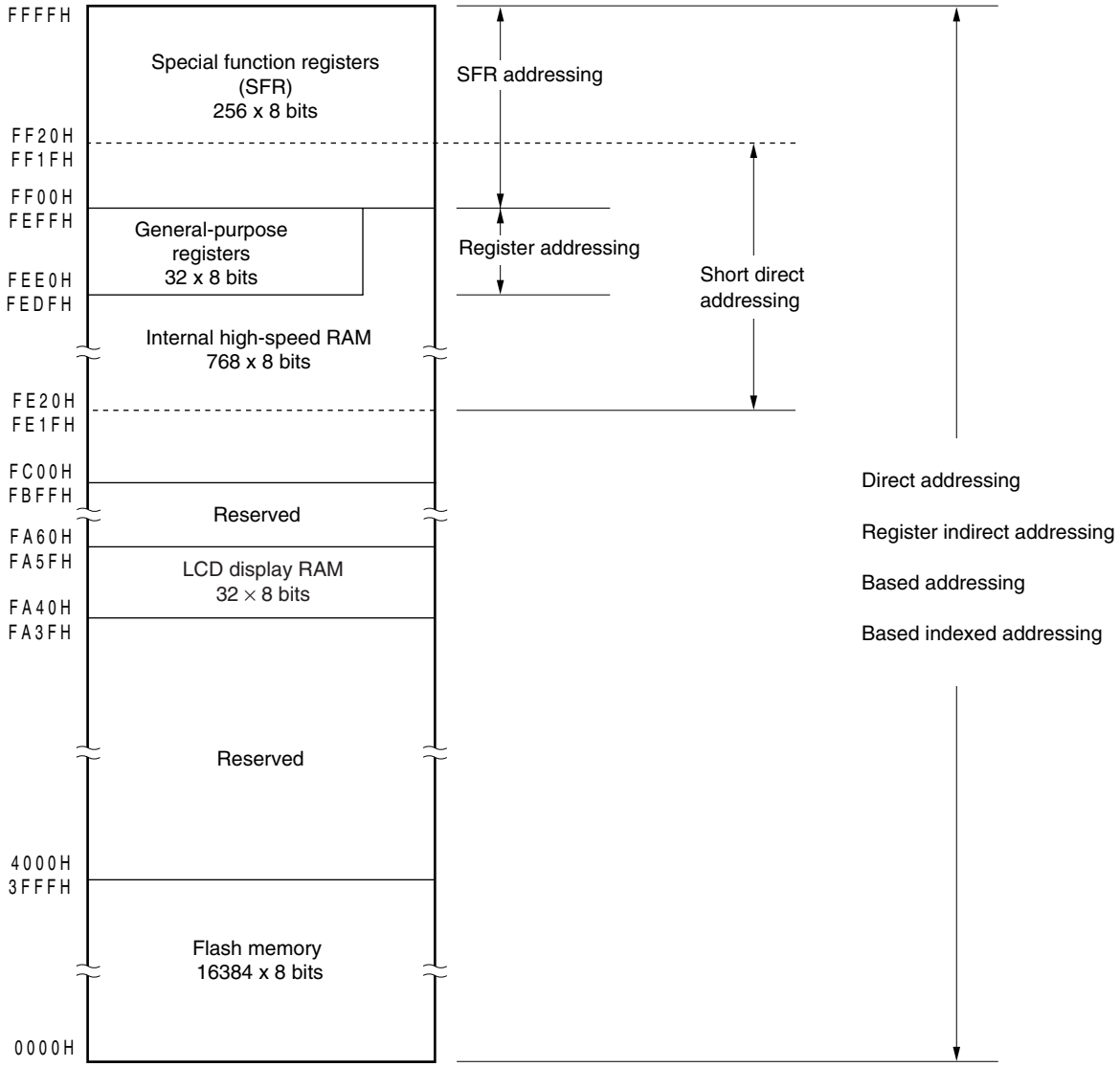


Table 5-5. CPU Clock Transition and SFR Register Setting Examples (4/4)

(9) CPU clock changing from subsystem clock (D) to high-speed system clock (C)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	EXCLK	OSCSEL	MSTOP	OSTC Register	XSEL[Note]	MCM0	CSS
(D) → (C) (X1 clock)	0	1	0	Must be checked	1	1	0
(D) → (C) (external main clock)	1	1	0	Must not be checked	1	1	0

Unnecessary if these registers are already set

Unnecessary if the CPU is operating with the high-speed system clock

Note The value of this flag can be changed only once after a reset release. This setting is not necessary if it has already been set.

Caution Set the clock after the supply voltage has reached the operable voltage of the clock to be set (see CHAPTER 30 ELECTRICAL SPECIFICATIONS (STANDARD PRODUCTS)).

(10) • HALT mode (E) set while CPU is operating with internal high-speed oscillation clock (B)
• HALT mode (F) set while CPU is operating with high-speed system clock (C)
• HALT mode (G) set while CPU is operating with subsystem clock (D)

Status Transition	Setting
(B) → (E) (C) → (F) (D) → (G)	Executing HALT instruction

(11) • STOP mode (H) set while CPU is operating with internal high-speed oscillation clock (B)
• STOP mode (I) set while CPU is operating with high-speed system clock (C)

(Setting sequence) →

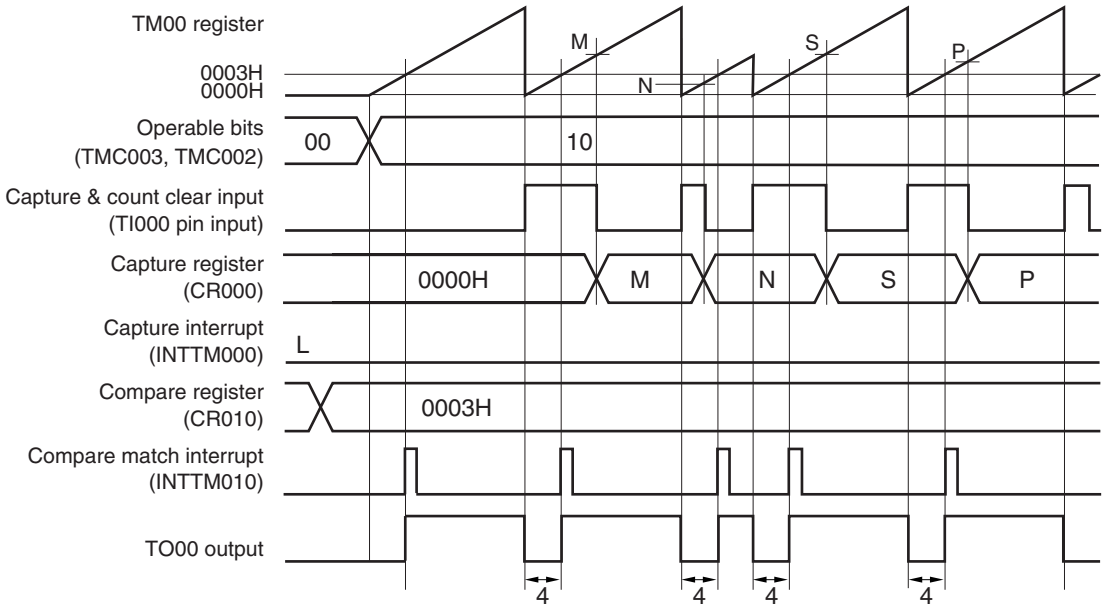
Status Transition	Setting	
(B) → (H) (C) → (I)	Stopping peripheral functions that cannot operate in STOP mode	Executing STOP instruction

Remarks 1. (A) to (I) in Table 5-5 correspond to (A) to (I) in Figure 5-15.

2. EXCLK, OSCSEL: Bits 7 and 6 of the clock operation mode select register (OSCCTL)
MSTOP: Bit 7 of the main OSC control register (MOC)
XSEL, MCM0: Bits 2 and 0 of the main clock mode register (MCM)
CSS: Bit 4 of the processor clock control register (PCC)

Figure 6-28. Timing Example of Clear & Start Mode Entered by TI000 Pin Valid Edge Input (CR000: Capture Register, CR010: Compare Register) (2/2)

(b) TOC00 = 13H, PRM00 = 10H, CRC00, = 03H, TMC00 = 0AH, CR010 = 0003H



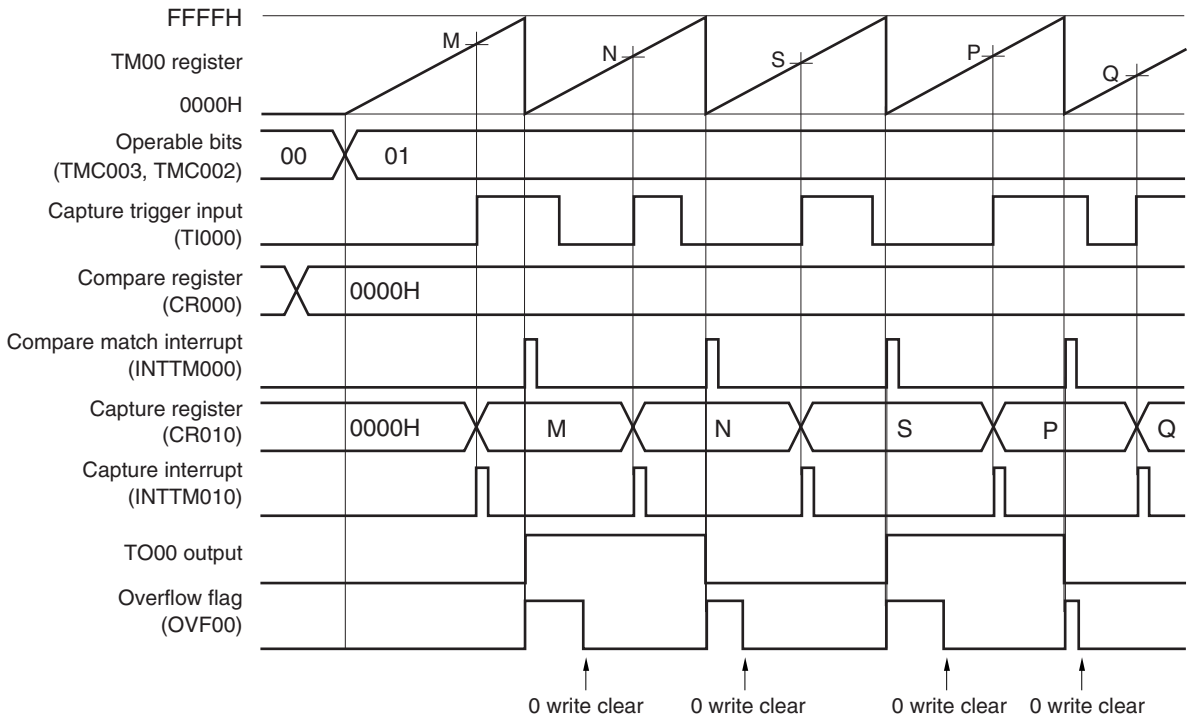
This is an application example where the width set to CR010 (4 clocks in this example) is to be output from the TO00 pin when the count value has been captured & cleared.

TM00 is cleared (to 0000H) at the rising edge detection of the TI000 pin and captured to CR000 at the falling edge detection of the TI000 pin. The TO00 output is inverted when TM00 is cleared (to 0000H) because the rising edge of the TI000 pin has been detected or when the value of TM00 matches that of a compare register (CR010).

When bit 1 (CRC001) of capture/compare control register 00 (CRC00) is 1, the count value of TM00 is captured to CR000 in the phase reverse to that of the input signal of the TI000 pin, but the capture interrupt signal (INTTM000) is not generated. However, the INTTM000 interrupt is generated when the valid edge of the TI010 pin is detected. Mask the INTTM000 signal when it is not used.

Figure 6-36. Timing Example of Free-Running Timer Mode (CR000: Compare Register, CR010: Capture Register)

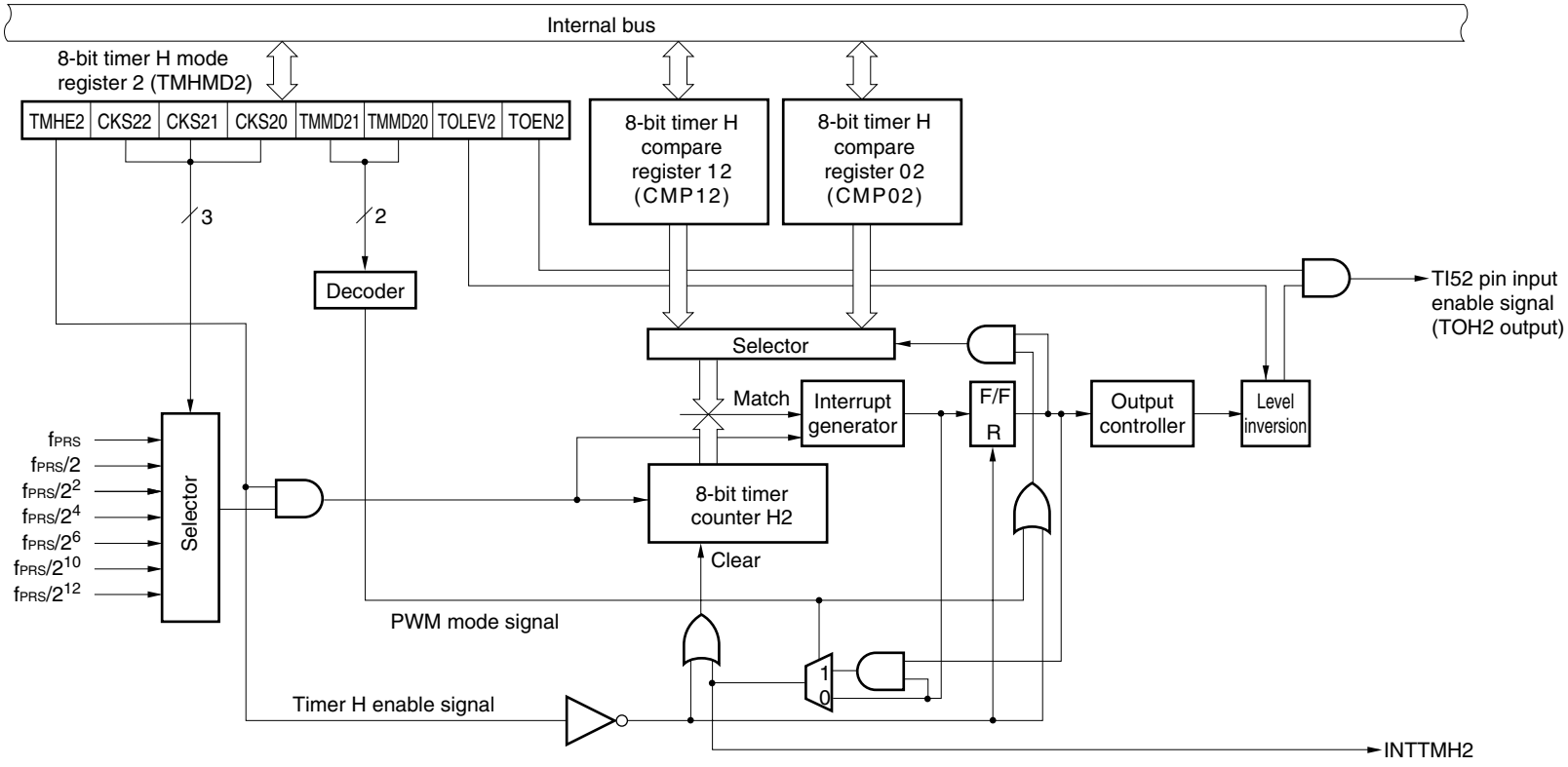
• TOC00 = 13H, PRM00 = 10H, CRC00 = 04H, TMC00 = 04H



This is an application example where a compare register and a capture register are used at the same time in the free-running timer mode.

In this example, the INTTM000 signal is generated and the TO00 output is reversed each time the count value of TM00 matches the set value of CR000 (compare register). In addition, the INTTM010 signal is generated and the count value of TM00 is captured to CR010 each time the valid edge of the TI000 pin is detected.

Figure 8-3. Block Diagram of 8-Bit Timer H2



CHAPTER 9 REAL-TIME COUNTER

9.1 Functions of Real-Time Counter

The real-time counter has the following features.

- Having counters of year, month, week, day, hour, minute, and second, and can count up to 99 years.
- Constant-period interrupt function (period: 1 month to 0.5 seconds)
- Alarm interrupt function (alarm: week, hour, minute)
- Interval interrupt function
- Pin output function of 1 Hz
- Pin output function of 512 Hz or 16.384 kHz or 32.768 kHz

9.2 Configuration of Real-Time Counter

The real-time counter includes the following hardware.

Table 9-1. Configuration of Real-Time Counter

Item	Configuration
Control registers	Real-time counter clock selection register (RTCCL)
	Real-time counter control register 0 (RTCC0)
	Real-time counter control register 1 (RTCC1)
	Real-time counter control register 2 (RTCC2)
	Sub-count register (RSUBC)
	Second count register (SEC)
	Minute count register (MIN)
	Hour count register (HOUR)
	Day count register (DAY)
	Week count register (WEEK)
	Month count register (MONTH)
	Year count register (YEAR)
	Watch error correction register (SUBCUD)
	Alarm minute register (ALARMWM)
	Alarm hour register (ALARMWH)
	Alarm week register (ALARMWW)

Cautions 4. The operation of the watchdog timer in the HALT and STOP modes differs as follows depending on the set value of bit 0 (LSROSC) of the option byte.

	LSROSC = 0 (Internal Low-Speed Oscillator Can Be Stopped by Software)	LSROSC = 1 (Internal Low-Speed Oscillator Cannot Be Stopped)
In HALT mode	Watchdog timer operation stops.	Watchdog timer operation continues.
In STOP mode		

If LSROSC = 0, the watchdog timer resumes counting after the HALT or STOP mode is released. At this time, the counter is not cleared to 0 but starts counting from the value at which it was stopped.

If oscillation of the internal low-speed oscillator is stopped by setting LSRSTOP (bit 1 of the internal oscillation mode register (RCM) = 1) when LSROSC = 0, the watchdog timer stops operating. At this time, the counter is not cleared to 0.

5. The watchdog timer continues its operation during self-programming and EEPROM emulation of the flash memory. During processing, the interrupt acknowledge time is delayed. Set the overflow time and window size taking this delay into consideration.

10.4.2 Setting overflow time of watchdog timer

Set the overflow time of the watchdog timer by using bits 3 to 1 (WDCS2 to WDCS0) of the option byte (0080H).

If an overflow occurs, an internal reset signal is generated. The present count is cleared and the watchdog timer starts counting again by writing “ACH” to WDTE during the window open period before the overflow time.

The following overflow time is set.

Table 10-3. Setting of Overflow Time of Watchdog Timer

WDCS2	WDCS1	WDCS0	Overflow Time of Watchdog Timer
0	0	0	$2^{10}/f_{RL}$ (3.88 ms)
0	0	1	$2^{11}/f_{RL}$ (7.76 ms)
0	1	0	$2^{12}/f_{RL}$ (15.52 ms)
0	1	1	$2^{13}/f_{RL}$ (31.03 ms)
1	0	0	$2^{14}/f_{RL}$ (62.06 ms)
1	0	1	$2^{15}/f_{RL}$ (124.12 ms)
1	1	0	$2^{16}/f_{RL}$ (248.24 ms)
1	1	1	$2^{17}/f_{RL}$ (496.48 ms)

Cautions 1. The combination of WDCS2 = WDCS1 = WDCS0 = 0 and WINDOW1 = WINDOW0 = 0 is prohibited.

2. The watchdog timer continues its operation during self-programming and EEPROM emulation of the flash memory. During processing, the interrupt acknowledge time is delayed. Set the overflow time and window size taking this delay into consideration.

Remarks 1. f_{RL}: Internal low-speed oscillation clock frequency

2. ( ): f_{RL} = 264 kHz (MAX.)

13.6 How to Read ΔΣ Type A/D Converter Characteristics Table

Here, special terms unique to the ΔΣ type A/D converter are explained.

(1) Resolution

This is the minimum analog input voltage that can be identified. That is, the percentage of the analog input voltage per bit of digital output is called 1LSB (Least Significant Bit). The percentage of 1LSB with respect to the full scale is expressed by %FSR (Full Scale Range).

1LSB is as follows when the resolution is 16 bits.

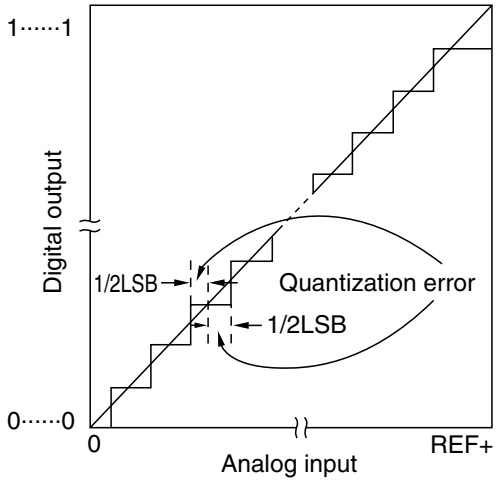
$1LSB = 1/2^{16} = 1/65536$
$\cong 0.0015\%FSR$

(2) Quantization error

When analog values are converted to digital values, a ±1/2LSB error naturally occurs. In an A/D converter, an analog input voltage in a range of ±1/2LSB is converted to the same digital code, so a quantization error cannot be avoided.

Note that the quantization error is not included in the offset, gain error, integral linearity error, and differential linearity error in the characteristics table.

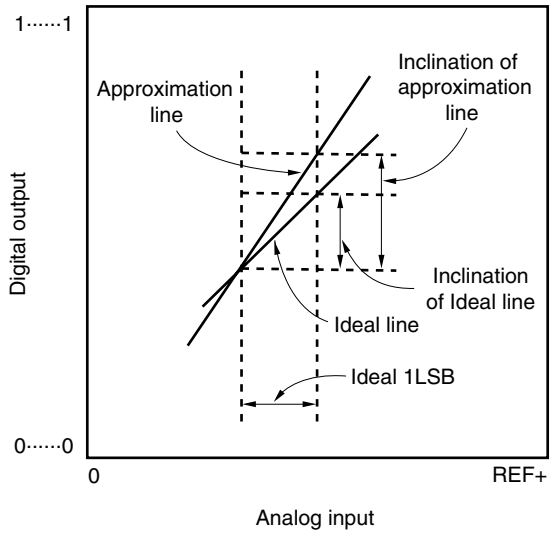
Figure 13-15. Quantization Error



(5) Gain error

The gain error is the ratio of the ideal inclination to the inclination of the approximation line.

Figure 13-18. Gain Error

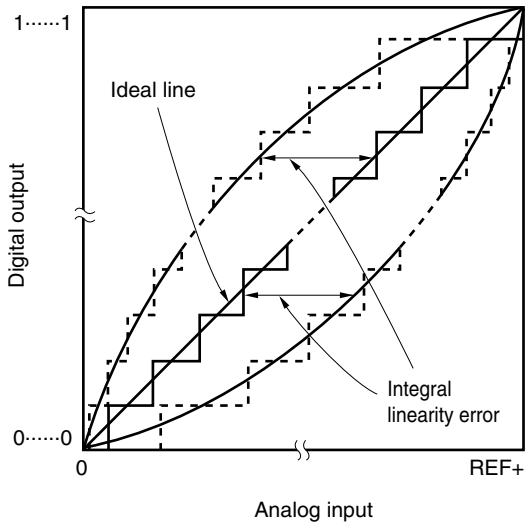


$$\text{Gain error} = \frac{\text{Inclination of approximation line} - 1}{\text{Inclination of Ideal line}} \times 100\ [\%]$$

(6) Integral linearity error

This shows the degree to which the conversion characteristics deviate from the approximation line. It expresses the maximum value of the difference between the actual measurement value and the ideal straight line when the offset and gain error are 0.

Figure 13-19. Integral linearity error



Notes 2. Set the serial clock to satisfy the following conditions.

- V_{DD} = 2.7 to 5.5 V: serial clock ≤ 4 MHz
- V_{DD} = 1.8 to 2.7 V: serial clock ≤ 2 MHz

Cautions 1. Do not write to CSIC10 while CSIE10 = 1 (operation enabled).

2. To use P11/$\overline{SCK10}$ and P13/SO10/TxD0/<TxD6> as general-purpose ports, set CSIC10 in the default status (00H).

3. The phase type of the data clock is type 1 after reset.

Remark f_{PRS}: Peripheral hardware clock oscillation frequency

(3) Port function register 1 (PF1)

This register sets the pin functions of P13/SO10/TxD0/<TxD6> pin.

PF1 is set using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets PF1 to 00H.

Figure 16-4. Format of Port Function Register 1 (PF1)

Address: FF20H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PF1	0	0	0	0	PF13	0	0	0

PF13	Port (P13), CSI10, UART0, and UART6 output specification
0	Used as P13 or SO10
1	Used as TxD0 or TxD6

16.4 Operation of Serial Interface CSI10

Serial interface CSI10 can be used in the following two modes.

- Operation stop mode
- 3-wire serial I/O mode

16.4.1 Operation stop mode

Serial communication is not executed in this mode. Therefore, the power consumption can be reduced. In addition, the P11/$\overline{\text{SCK10}}$, P12/SI10/RxD0, and P13/SO10/TxD0 pins can be used as ordinary I/O port pins in this mode.

(1) Register used

The operation stop mode is set by serial operation mode register 10 (CSIM10).

To set the operation stop mode, clear bit 7 (CSIE10) of CSIM10 to 0.

(a) Serial operation mode register 10 (CSIM10)

CSIM10 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets CSIM10 to 00H.

Address: FF80H After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	0
CSIM10	CSIE10	TRMD10	0	DIR10	0	0	0	CSOT10

CSIE10	Operation control in 3-wire serial I/O mode
0	Disables operation[Note 1] and asynchronously resets the internal circuit[Note 2].

Notes 1. To use P11/$\overline{\text{SCK10}}$, P12/SI10/RxD0/<RxD6>, and P13/SO10/TxD0/<TxD6> as general-purpose ports, set CSIM10 in the default status (00H).

2. Bit 0 (CSOT10) of CSIM10 and serial I/O shift register 10 (SIO10) are reset.

16.4.2 3-wire serial I/O mode

The 3-wire serial I/O mode is used for connecting peripheral ICs and display controllers with a clocked serial interface.

In this mode, communication is executed by using three lines: the serial clock ($\overline{\text{SCK10}}$), serial output (SO10), and serial input (SI10) lines.

(1) Registers used

- Serial operation mode register 10 (CSIM10)
- Serial clock selection register 10 (CSIC10)
- Port mode register 1 (PM1)
- Port register 1 (P1)

17.7.4 Four-time-slice display example

Figure 17-28 shows how the 12-digit LCD panel having the display pattern shown in Figure 17-27 is connected to the segment signals (SEG0 to SEG23) and the common signals (COM0 to COM3) of the 78K0/LE3 chip. This example displays data "123456.789012" in the LCD panel. The contents of the display data memory (addresses FA40H to FA57H) correspond to this display.

The following description focuses on numeral "6." (6.) displayed in the seventh digit. To display "6." in the LCD panel, it is necessary to apply the select or deselect voltage to the SEG12 and SEG13 pins according to Table 17-9 at the timing of the common signals COM0 to COM3; see Figure 17-27 for the relationship between the segment signals and LCD segments.

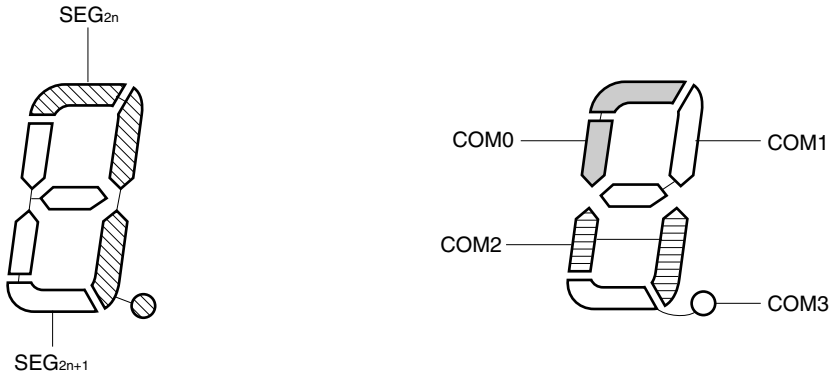
Table 17-9. Select and Deselect Voltages (COM0 to COM3)

Segment / Common	SEG12	SEG13
COM0	Select	Select
COM1	Deselect	Select
COM2	Select	Select
COM3	Select	Select

According to Table 17-9, it is determined that the display data memory location (FA4CH) that corresponds to SEG12 must contain 1101.

Figure 17-29 shows examples of LCD drive waveforms between the SEG12 signal and each common signal. When the select voltage is applied to SEG12 at the timing of COM0, an alternate rectangle waveform, $+V_{LCD}/-V_{LCD}$, is generated to turn on the corresponding LCD segment.

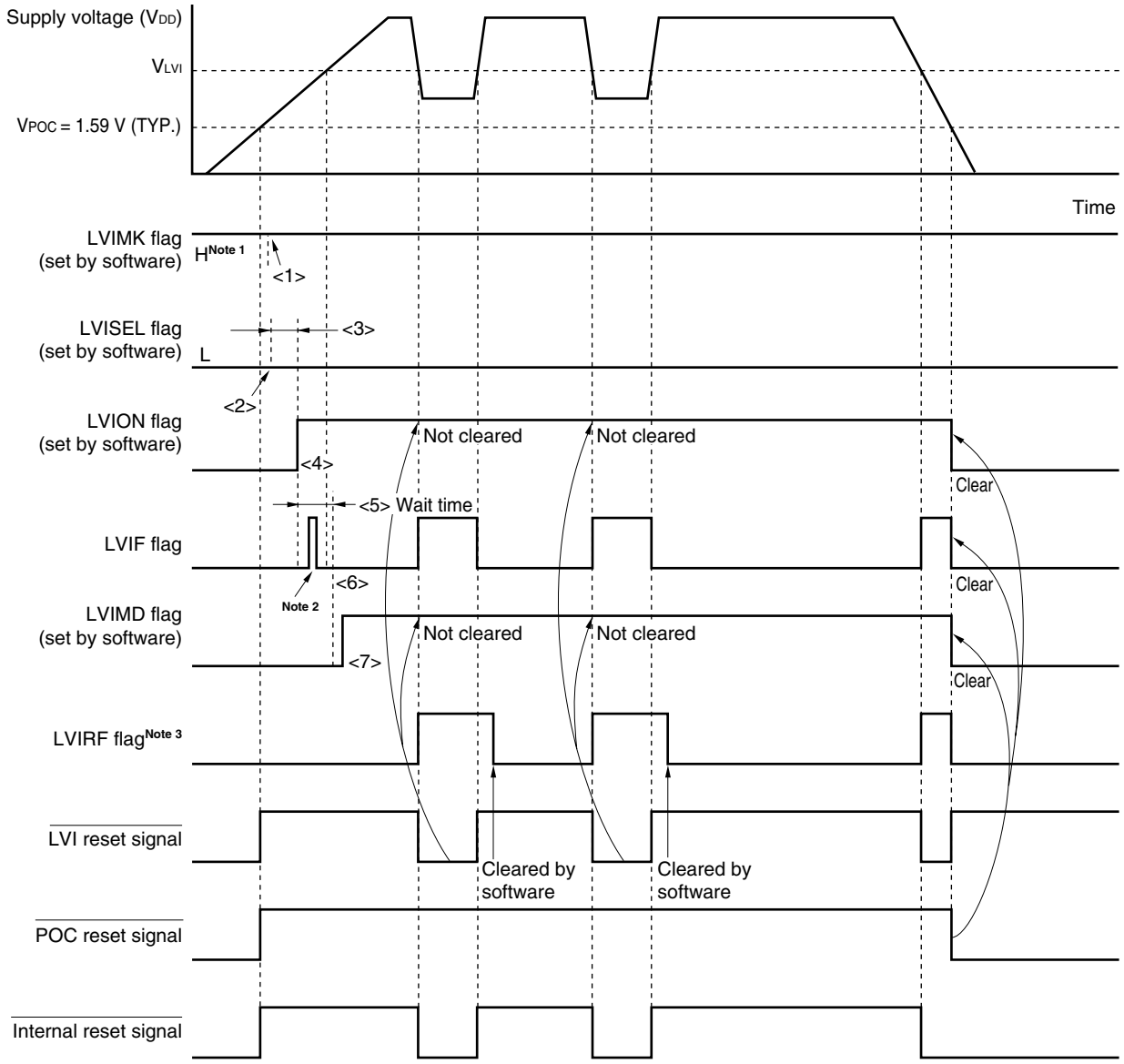
Figure 17-27. Four-Time-Slice LCD Display Pattern and Electrode Connections



Remark n = 0 to 11

Figure 25-5. Timing of Low-Voltage Detector Internal Reset Signal Generation (Detects Level of Supply Voltage (V_{DD})) (1/2)

(1) In 1.59 V POC mode (option byte: POCMODE = 0)



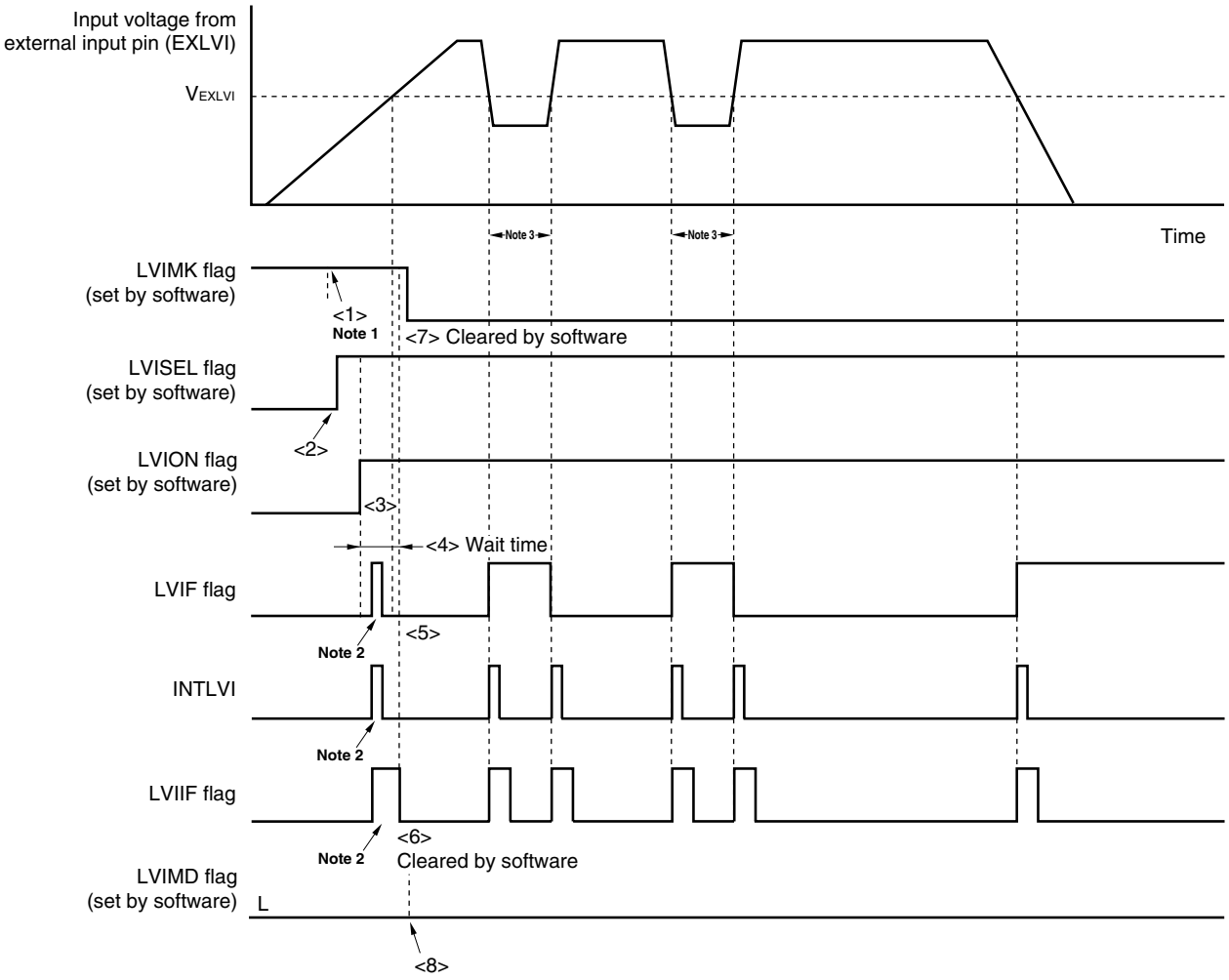
Notes 1. The LVIMK flag is set to "1" by reset signal generation.

2. The LVIF flag may be set (1).

3. LVIRF is bit 0 of the reset control flag register (RESF). For details of RESF, see **CHAPTER 23 RESET FUNCTION**.

Remark <1> to <7> in Figure 25-5 above correspond to <1> to <7> in the description of "When starting operation" in **25.4.1 (1) When detecting level of supply voltage (V_{DD})**.

Figure 25-8. Timing of Low-Voltage Detector Interrupt Signal Generation (Detects Level of Input Voltage from External Input Pin (EXLVI))



Notes 1. The LVIMK flag is set to "1" by reset signal generation.

2. The interrupt request signal (INTLVI) is generated and the LVIF and LVIIF flags may be set (1).

3. If LVION is cleared (0) in a state below the LVI detection voltage, an INTLVI signal is generated and LVIIF becomes 1.

Remark <1> to <8> in Figure 25-8 above correspond to <1> to <8> in the description of "When starting operation" in **25.4.2 (2) When detecting level of input voltage from external input pin (EXLVI)**.

Table 27-10. Relationship Between Enabling Security Function and Command

(1) During on-board/off-board programming

Valid Security	Executed Command		
	Batch Erase (Chip Erase)	Block Erase	Write
Prohibition of batch erase (chip erase)	Cannot be erased in batch	Blocks cannot be erased.	Can be performed[Note].
Prohibition of block erase	Can be erased in batch.		Can be performed.
Prohibition of writing			Cannot be performed.
Prohibition of rewriting boot cluster 0	Cannot be erased in batch	Boot cluster 0 cannot be erased.	Boot cluster 0 cannot be written.

Note Confirm that no data has been written to the write area. Because data cannot be erased after batch erase (chip erase) is prohibited, do not write data if the data has not been erased.

(2) During self programming

Valid Security	Executed Command	
	Block Erase	Write
Prohibition of batch erase (chip erase)	Blocks can be erased.	Can be performed.
Prohibition of block erase		
Prohibition of writing		
Prohibition of rewriting boot cluster 0	Boot cluster 0 cannot be erased.	Boot cluster 0 cannot be written.

Table 27-11 shows how to perform security settings in each programming mode.

Table 27-11. Setting Security in Each Programming Mode

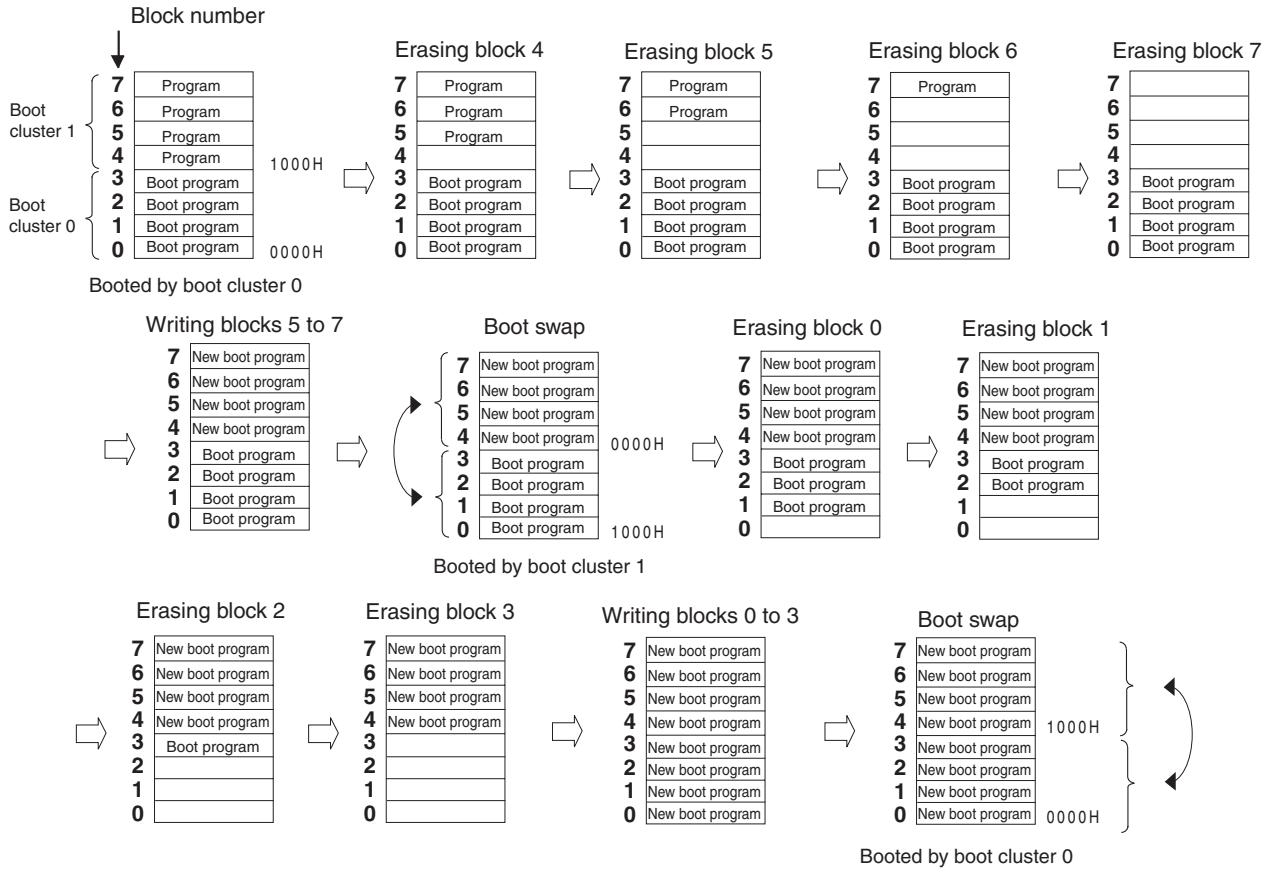
(1) On-board/off-board programming

Security	Security Setting	How to Disable Security Setting
Prohibition of batch erase (chip erase)	Set via GUI of dedicated flash memory programmer, etc.	Cannot be disabled after set.
Prohibition of block erase		Execute batch erase (chip erase) command
Prohibition of writing		
Prohibition of rewriting boot cluster 0		Cannot be disabled after set.

(2) Self programming

Security	Security Setting	How to Disable Security Setting
Prohibition of batch erase (chip erase)	Set by using information library.	Cannot be disabled after set.
Prohibition of block erase		Execute batch erase (chip erase) command during on-board/off-board programming (cannot be disabled during self programming)
Prohibition of writing		
Prohibition of rewriting boot cluster 0		Cannot be disabled after set.

Figure 27-18. Example of Executing Boot Swapping



<R> **Recommended Oscillator Constants**

(1) X1 Oscillator: Ceramic resonator (T_A = −40 to +85°C)

Manufacturer	Part Number	SMD/ Lead	Frequency (MHz)	Recommended circuit invariable		Oscillation Voltage Range	
				C1 (pF)	C2 (pF)	MIN.(V)	MAX.(V)
Murata Mfg.	CSTCC2M00G56-R0	SMD	2.00	Internal (47)	Internal (47)	1.8	5.5
	CSTLS4M00G56-B0	Lead	4.00	Internal (47)	Internal (47)		
	CSTCR4M00G55-R0	SMD		Internal (39)	Internal (39)		
	CSTLS4M19G56-B0	Lead	4.194	Internal (47)	Internal (47)		
	CSTCR4M19G55-R0	SMD		Internal (39)	Internal (39)		
	CSTLS4M91G56-B0	Lead	4.915	Internal (47)	Internal (47)	2.0	
	CSTCR4M91G55-R0	SMD		Internal (39)	Internal (39)	1.8	
	CSTLS5M00G56-B0	Lead	5.00	Internal (47)	Internal (47)	2.0	
	CSTCR5M00G55-R0	SMD		Internal (39)	Internal (39)	1.8	
	CSTLS6M00G56-B0	Lead	6.00	Internal (47)	Internal (47)	2.2	
	CSTCR6M00G55-R0	SMD		Internal (39)	Internal (39)	1.9	
	CSTLS8M00G56-B0	Lead	8.00	Internal (47)	Internal (47)	2.2	
	CSTCE8M00G55-R0	SMD		Internal (33)	Internal (33)	1.8	
	CSTLS8M38G56-B0	Lead	8.388	Internal (47)	Internal (47)	2.2	
	CSTCE8M38G55-R0	SMD		Internal (33)	Internal (33)	1.8	
	CSTLS10M0G53-B0	SMD	10.0	Internal (15)	Internal (15)	1.8	
	CSTCE10M0G55-R0	SMD		Internal (33)	Internal (33)	2.1	
Murata Mfg. (low-capacitance products)	CSTLS4M91G53-B0	Lead	4.915	Internal (15)	Internal (15)	1.8	5.5
	CSTLS5M00G53-B0	Lead	5.00	Internal (15)	Internal (15)	1.8	
	CSTCR6M00G53-R0	SMD	6.00	Internal (15)	Internal (15)	1.8	
	CSTLS6M00G53-B0	Lead		Internal (15)	Internal (15)	1.8	
	CSTLS8M00G53-B0	Lead	8.00	Internal (15)	Internal (15)	1.8	
	CSTLS8M38G53-B0	Lead	8.388	Internal (15)	Internal (15)	1.8	
	CSTCE10M0G52-R0	SMD	10.0	Internal (10)	Internal (10)	1.8	

Caution The oscillator constants shown above are reference values based on evaluation in a specific environment by the resonator manufacturer. If it is necessary to optimize the oscillator characteristics in the actual application, apply to the resonator manufacturer for evaluation on the implementation circuit. The oscillation voltage and oscillation frequency only indicate the oscillator characteristic. Use the 78K0/LE3 so that the internal operation conditions are within the specifications of the DC and AC characteristics.

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Page	Description	Classification
CHAPTER 23 RESET FUNCTION		
p. 622	Change of **Figure 23-2. Timing of Reset by $\overline{\text{RESET}}$ Input**	(c)
p. 622	Change of **Figure 23-3. Timing of Reset Due to Watchdog Timer Overflow**	(c)
p. 623	Change of **Figure 23-4. Timing of Reset in STOP Mode by $\overline{\text{RESET}}$ Input**	(c)
CHAPTER 24 POWER-ON-CLEAR CIRCUIT		
p. 632	Change of **Figure 24-2. Timing of Generation of Internal Reset Signal by Power-on-Clear Circuit and Low-Voltage Detector (1)**	(b)
p. 633	Change of **Caution 2** in **Figure 24-2. Timing of Generation of Internal Reset Signal by Power-on-Clear Circuit and Low-Voltage Detector (2)**	(b, c)
CHAPTER 27 FLASH MEMORY		
p. 661	Change of **Note 2** in and addition of **Caution** to **Table 27-3. Wiring Between 78K0/LE3 and Dedicated Flash memory programmer**	(c)
p. 665	Change of **Note 1** in **Table 27-4. Pin Connection**	(c)
p. 668	Change of **Caution 2** in **27.6.6 Other signal pins**	(c)
p. 669	Change of **Figure 27-12. Flash Memory Manipulation Procedure**	(b)
p. 670	Change of **Table 27-7. Communication Modes**	(b)
pp. 674 to 676	Addition of **27.9 Processing Time for Each Command When PG-FP5 Is Used (Reference)**	(b, c)
pp. 677 to 686	Revision of **27.10 Flash Memory Programming by Self-Programming**	(b, c)
CHAPTER 28 ON-CHIP DEBUG FUNCTION		
pp. 687, 688	Full-scale revision of chapter	(c)
CHAPTER 30 ELECTRICAL SPECIFICATIONS (STANDARD PRODUCTS)		
p. 702	Addition of **Caution**	(c)
p. 706	Addition of **Recommended Oscillator Constants**	(b)
p. 710	Change of **Notes 1**, **6** in and addition of **Note 5** to supply current of **DC Characteristics**	(b)
p. 711	Change of $\Delta\Sigma$ type A/D converter operating current value in **DC Characteristics**	(b)
p. 719	Change of **16-bit $\Delta\Sigma$ type A/D Converter Characteristics**	(b)
p. 720	Change of **Note 3** in **LCD Characteristics**	(b)
p. 723	Change of **Basic characteristics** in **Flash Memory Programming Characteristics** and addition of **Notes 1**, **4**	(b, c)
CHAPTER 32 RECOMMENDED SOLDERING CONDITIONS		
p. 726	Addition of chapter	(b, c)
APPENDIX A DEVELOPMENT TOOLS		
pp. 729 to 736	Addition of appendix A	(c)

Remark “Classification” in the above table classifies revisions as follows.

(a): Error correction, (b): Addition/change of specifications, (c): Addition/change of description or note, (d): Addition/change of package, part number, or management division, (e): Addition/change of related documents