Renesas Electronics America Inc - UPD78F0451GK-GAJ-AX Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	3-Wire SIO, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	46
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0451gk-gaj-ax

1.5 78K0/Lx3 Microcontroller Series Lineup

ROM	RAM	78K0/LC3	78K0/LD3	78K0/LE3	78K0/LF3
		48 Pins	52 Pins	64 Pins	80 Pins
60 KB	2 KB	–	–	μPD78F0465 μPD78F0455 μPD78F0445	μPD78F0495 μPD78F0485 μPD78F0475
48 KB	2 KB	–	–	μPD78F0464 μPD78F0454 μPD78F0444	μPD78F0494 μPD78F0484 μPD78F0474
32 KB	1 KB	μPD78F0413 μPD78F0403	μPD78F0433 μPD78F0423	μPD78F0463 μPD78F0453 μPD78F0443	μPD78F0493 μPD78F0483 μPD78F0473
24 KB	1 KB	μPD78F0412 μPD78F0402	μPD78F0432 μPD78F0422	μPD78F0462 μPD78F0452 μPD78F0442	μPD78F0492 μPD78F0482 μPD78F0472
16 KB	768 B	μPD78F0411 μPD78F0401	μPD78F0431 μPD78F0421	μPD78F0461 μPD78F0451 μPD78F0441	μPD78F0491 μPD78F0481 μPD78F0471
8 KB	512 B	μPD78F0410 μPD78F0400	μPD78F0430 μPD78F0420	–	–

(2/3)

Item \ Part Number			78K0/LE3													
			μPD78F044x					μPD78F045x					μPD78F046x				
			64 Pins													
Flash memory (KB)			16	24	32	48	60	16	24	32	48	60	16	24	32	48	60
RAM (KB)			0.75	1	1	2	2	0.75	1	1	2	2	0.75	1	1	2	2
Power supply voltage			V_{DD} = 1.8 to 5.5 V														
Regulator			Provided														
Minimum instruction execution time			0.2 μs (10 MHz: V_{DD} = 2.7 to 5.5 V)/ 0.4 μs (5 MHz: V_{DD} = 1.8 to 5.5 V)														
Clock	Main	High-speed system clock	10 MHz: V_{DD} = 2.7 to 5.5 V/5 MHz: V_{DD} = 1.8 to 5.5 V														
		Internal high-speed oscillation clock	8 MHz (TYP.): V_{DD} = 1.8 to 5.5 V														
	Subclock		32.768 kHz (TYP.): V_{DD} = 1.8 to 5.5 V														
	Internal low-speed oscillation clock		240 kHz (TYP.): V_{DD} = 1.8 to 5.5 V														
Port	Total		46														
Timer	16 bits (TM0)		1 ch														
	8 bits (TM5)		3 ch														
	8 bits (TMH)		3 ch														
	RTC		1 ch														
	WDT		1 ch														
Serial interface	3-wire CSI/UART[Note 1]		1 ch														
	UART supporting LIN-bus[Note 2]		1 ch														
LCD	Type		External resistance division and internal resistance division are switchable.														
	Segment signal		32 (28) [28 (24)] [Note 3, 4]										24 (20) [20 (16)] [Note 3, 4]				
	Common signal		4 (8)[Note 3]														
10-bit successive approximation type A/D			–					8 ch									
16-bit ΔΣ type A/D			–										3 ch				
Interrupt	External		6														
	Internal		19					20					21				
Segment key source signal output			8 ch														
Key interrupt			5 ch														
Reset	$\overline{\text{RESET}}$ pin		Provided														
	POC		1.59 V ±0.15 V (Time for rising up to 1.8 V : 3.6 ms (MAX.))														
	LVI		The detection level of the supply voltage is selectable in 16 steps.														
	WDT		Provided														
Clock output			–														
Buzzer output			Provided														
Remote controller receiver			Provided														
MCG			Provided														
On-chip debug function			Provided														
Operating ambient temperature			T_A = –40 to +85°C														

Notes 1. Select either of the functions of these alternate-function pins.

2. The LIN-bus supporting UART pins can be changed to the 3-wire CSI/UART pins (pin numbers 62 and 63).

3. The values in parentheses are the number of signal outputs when 8com is used.

<R> **4.** The values in square brackets are the number of signal outputs when using the UART6 pins (RxD6, TxD6) on the bottom side.

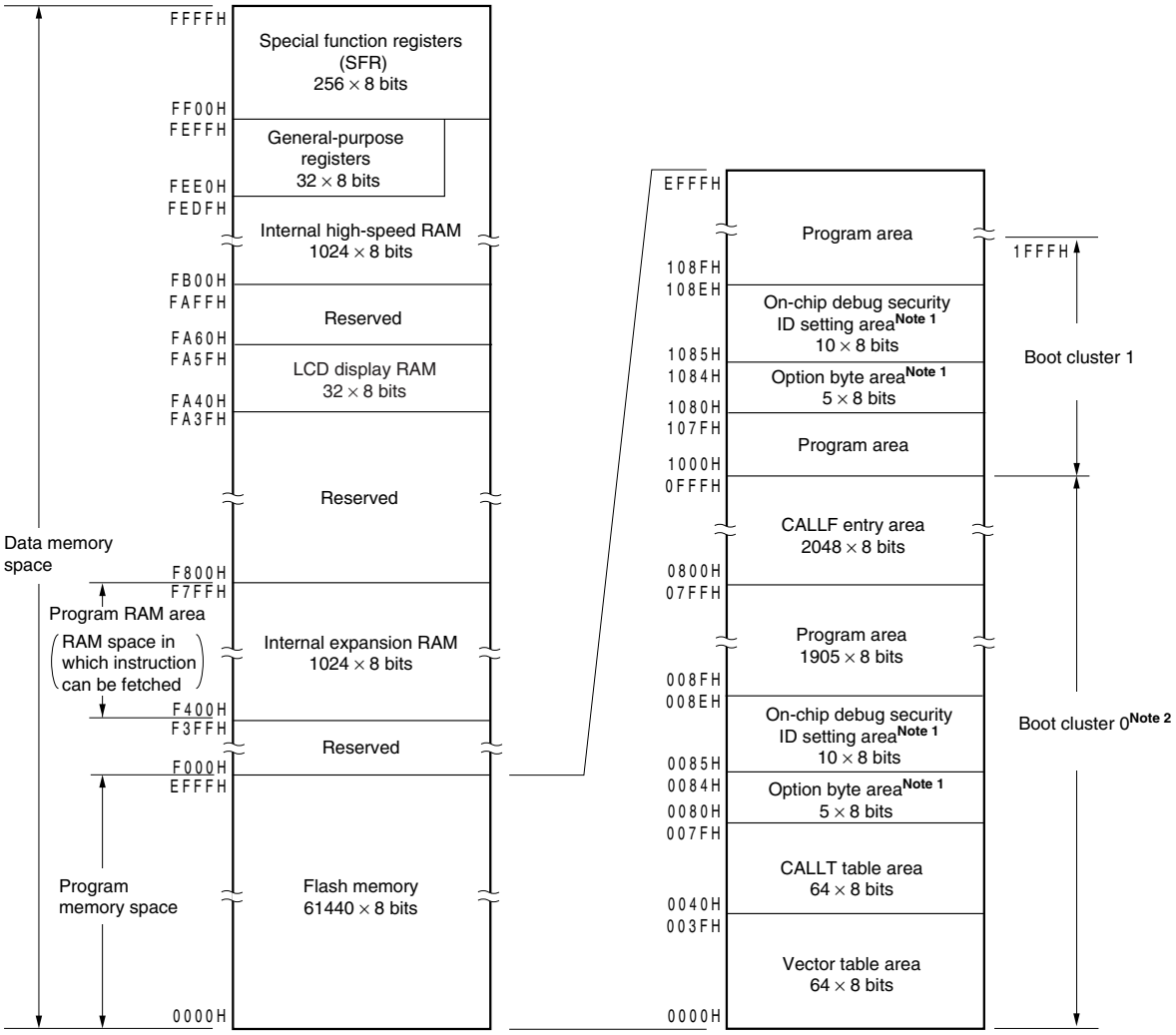
1.7 Outline of Functions (μPD78F044x)

(1/2)

Item		μPD78F0441	μPD78F0442	μPD78F0443	μPD78F0444	μPD78F0445
Internal memory	Flash memory (self-programming supported)[Note]	16 KB	24 KB	32 KB	48 KB	60 KB
	High-speed RAM[Note]	768 bytes	1 KB			
	Expansion RAM[Note]	–			1 KB	
	LCD display RAM	32 × 4 bits (with 4 com) or 28 × 8 bits (with 8 com)				
Memory space		64 KB				
Main system clock (oscillation frequency)	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) 2 to 10 MHz: V_{DD} = 2.7 to 5.5 V, 2 to 5 MHz: V_{DD} = 1.8 to 5.5 V				
	Internal high-speed oscillation clock	Internal oscillation 8 MHz (TYP.): V_{DD} = 1.8 to 5.5 V				
Subsystem clock (oscillation frequency)		XT1 (crystal) oscillation 32.768 kHz (TYP.): V_{DD} = 1.8 to 5.5 V				
Internal low-speed oscillation clock (for TMH1, WDT)		Internal oscillation 240 kHz (TYP.): V_{DD} = 1.8 to 5.5 V				
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)				
Minimum instruction execution time		0.2 μs (high-speed system clock: @ f_{XH} = 10 MHz operation)				
		0.25 μs (internal high-speed oscillation clock: @ f_{RH} = 8 MHz (TYP.) operation)				
		122 μs (subsystem clock: @ f_{SUB} = 32.768 kHz operation)				
Instruction set		• 8-bit operation and 16-bit operation • Bit manipulate (set, reset, test, and Boolean operation) • BCD adjust, etc.				
I/O ports		Total: 46 CMOS I/O: 42 CMOS input: 4				
Timers		• 16-bit timer/event counter: 1 channel • 8-bit timer/event counter: 3 channels (out of which 2 channels can perform PWM output) • 8-bit timer: 3 channels (out of which 2 channels can perform PWM output) • Real-time counter: 1 channel • Watchdog timer: 1 channel				
	Timer outputs	5 (PWM output: 4 and PPG output: 1)				
	RTC outputs	2 • 1 Hz (Subsystem clock: f_{SUB} = 32.768 kHz) • 512 Hz or 16.384 kHz or 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz)				
Buzzer output		• 1.22 kHz, 2.44 kHz, 4.88 kHz, 9.77 MHz (peripheral hardware clock: @ f_{PRS} = 10 MHz operation)				

Note The internal flash memory capacity, internal high-speed RAM capacity, and internal expansion RAM capacity can be changed using the internal memory size switching register (IMS) and the internal expansion RAM size switching register (IXS).

Figure 3-9. Memory Map (μPD78F0445, 78F0455)



Notes 1. When boot swap is not used: Set the option bytes to 0080H to 0084H, and the on-chip debug security IDs to 0085H to 008EH.

When boot swap is used: Set the option bytes to 0080H to 0084H and 1080H to 1084H, and the on-chip debug security IDs to 0085H to 008EH and 1085H to 108EH.

2. Writing boot cluster 0 can be prohibited depending on the setting of security (see **27.8 Security Setting**).

Remark The flash memory is divided into blocks (one block = 1 KB). For the address values and block numbers, see **Table 3-2 Correspondence Between Address Values and Block Numbers in Flash Memory**.

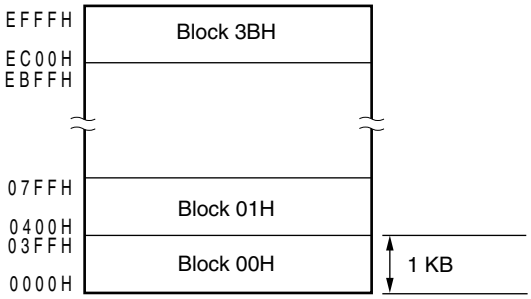
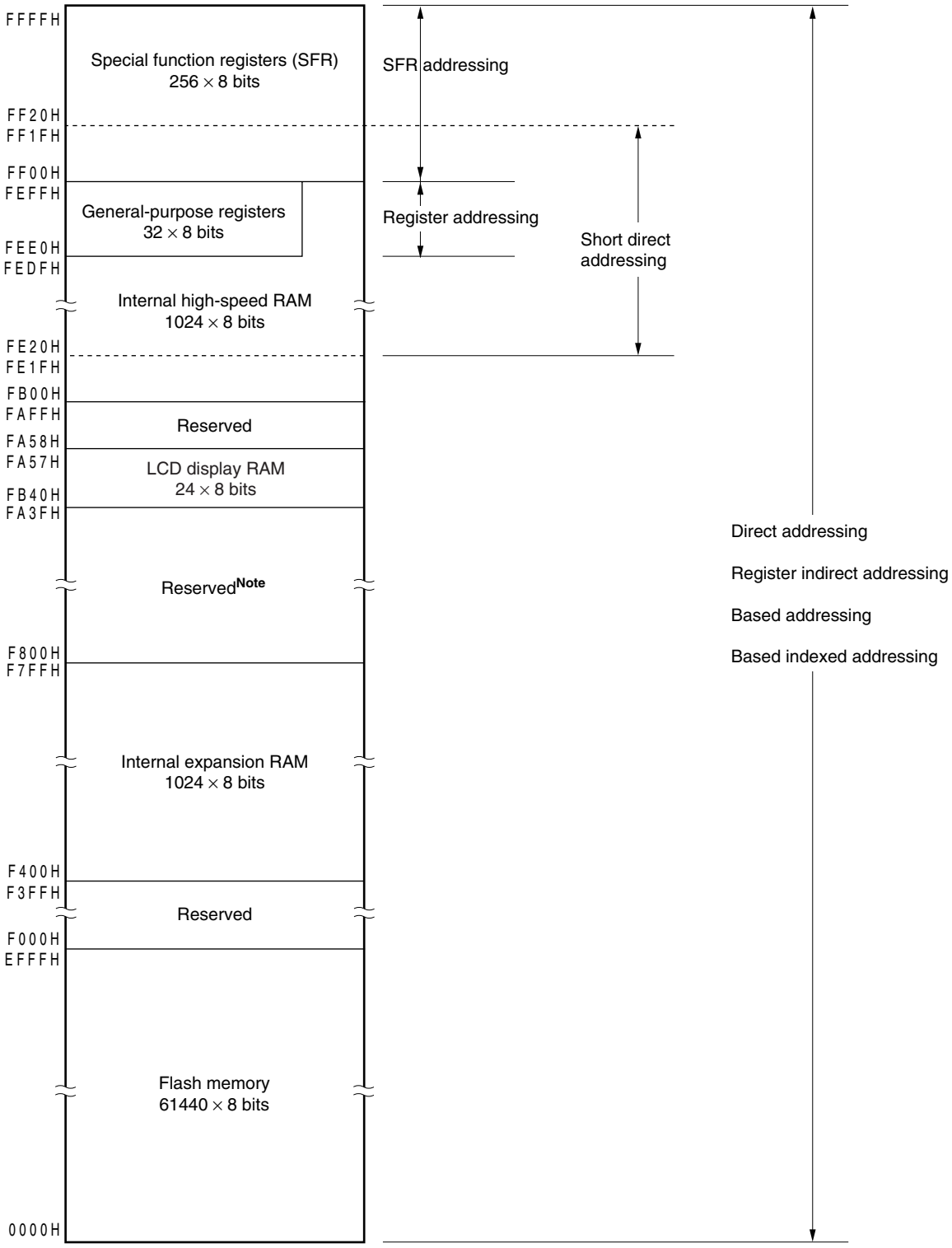


Figure 3-20. Correspondence Between Data Memory and Addressing (μPD78F0465)



<R> **Note** However, FA26H and FA27H can be used (See **13.3 Registers Used in 16-Bit ΔΣ Type A/D Converter**).

Figure 6-9. Format of Prescaler Mode Register 00 (PRM00)

Address: FFBBH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PRM00	ES101	ES100	ES001	ES000	0	PRM002	PRM001	PRM000

ES101	ES100	TI010 pin valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

ES001	ES000	TI000 pin valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

PRM002	PRM001	PRM000	Count clock selection[Note 1]			
				f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 10 MHz
0	0	0	f_{PRS}[Note 2]	2 MHz	5 MHz	10 MHz
0	0	1	$f_{PRS}/2$	1 MHz	2.5 MHz	5 MHz
0	1	0	$f_{PRS}/2^2$	500 kHz	1.25 MHz	2.5 MHz
0	1	1	$f_{PRS}/2^4$	1.25 MHz	2.5 MHz	625 kHz
1	0	0	$f_{PRS}/2^8$	7.81 kHz	19.53 kHz	39.06 kHz
1	0	1	f_{SUB}	32.768 kHz		
1	1	0	TI000 valid edge[Note 3]			
1	1	1	TM52 output			

Notes 1. If the peripheral hardware clock (f_{PRS}) operates on the high-speed system clock (f_{XH}) (XSEL = 1), the f_{PRS} operating frequency varies depending on the supply voltage.
- V_{DD} = 2.7 to 5.5 V: $f_{PRS} \leq$ 10 MHz
- V_{DD} = 1.8 to 2.7 V: $f_{PRS} \leq$ 5 MHz

2. If the peripheral hardware clock (f_{PRS}) operates on the internal high-speed oscillation clock (f_{RH}) (XSEL = 0), when 1.8 V $\leq V_{DD} <$ 2.7 V, the setting of PRM002 = PRM001 = PRM000 = 0 (count clock: f_{PRS}) is prohibited.

3. The external clock from the TI000 pin requires a pulse longer than twice the cycle of the peripheral hardware clock (f_{PRS}).

Caution Do not select the valid edge of TI000 as the count clock during the pulse width measurement.

Remarks 1. 8-bit timer/event counter 52 (TM52) output can be selected as the TM00 count clock by setting PRM002, PRM001, PRM000 = 1, 1, 1. Any frequency can be set as the 16-bit timer (TM00) count clock, depending on the TM52 count clock and compare register setting values.

2. f_{PRS}: Peripheral hardware clock frequency
f_{SUB}: Subsystem clock frequency

(5) Input switch control register (ISC)

The input source to TI000 becomes the input signal from the P33/TI000 pin, by setting ISC1 to 0.

ISC can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets ISC to 00H.

Figure 6-10. Format of Input Switch Control Register (ISC)

Address: FF4FH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ISC	0	0	ICS5	ICS4	ICS3	ICS2	ICS1	ICS0

ICS5	ICS4	TxD6, RxD6 input source selection
0	0	TxD6:P112, RxD6: P113
1	0	TxD6:P13, RxD6: P12
Other than above		Setting prohibited

ISC3	RxD6/P113 input enabled/disabled
0	RxD6/P113 input disabled
1	RxD6/P113 input enabled

ISC2	TI52 input source control
0	No enable control of TI52 input (P34)
1	Enable controlled of TI52 input (P34)Note 1

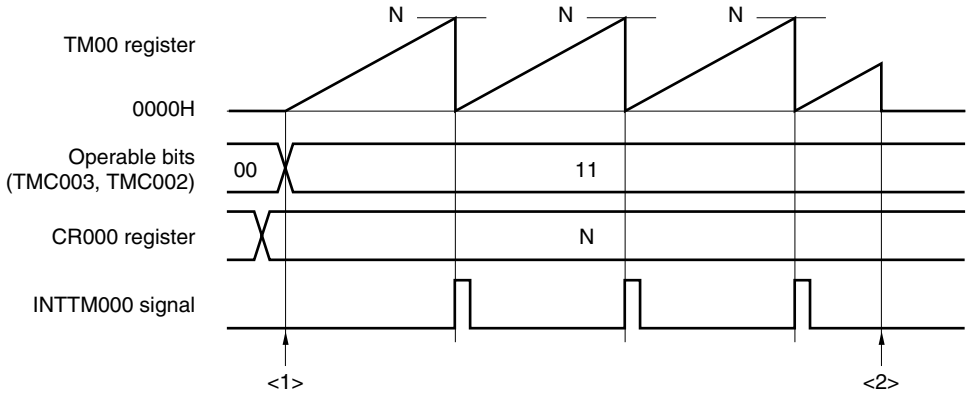
ISC1	TI000 input source selection
0	TI000 (P33)
1	RxD6 (P12 or P113Note 2)

ISC0	INTP0 input source selection
0	INTP0 (P120)
1	RxD6 (P12 or P113Note 2)

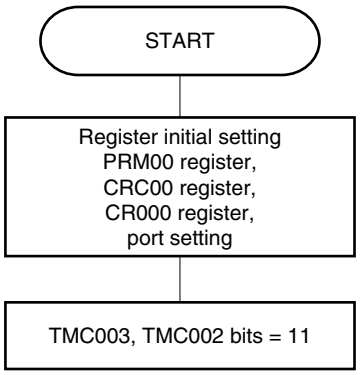
Notes 1. TI52 input is controlled by TOH2 output signal.

<R> **2.** This is selected by ISC5 and ISC4.

Figure 6-15. Example of Software Processing for Interval Timer Function



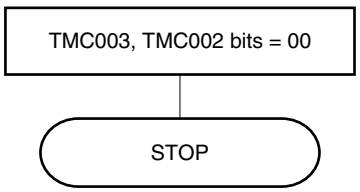
<1> Count operation start flow



Initial setting of these registers is performed before setting the TMC003 and TMC002 bits to 11.

Starts count operation

<2> Count operation stop flow



The counter is initialized and counting is stopped by clearing the TMC003 and TMC002 bits to 00.

Correction example <2>

Example of correcting from 32767.4 Hz to 32768 Hz (32767.4 Hz + 18.3 ppm)

[Measuring the oscillation frequency]

The oscillation frequency[Note] of each product is measured by outputting about 32 kHz from the RTCCL pin or outputting about 1 Hz from the RTC1HZ pin when the watch error correction register is set to its initial value (00H).

Note See **9.4.5 1 Hz output of real-time counter** for the setting procedure of outputting about 1 Hz from the RTC1HZ pin, and **9.4.6 32.768 kHz output of real-time counter** for the setting procedure of outputting about 32 kHz from the RTCCL pin.

[Calculating the correction value]

(When the output frequency from the RTCCL pin is 0.9999817 Hz)

Oscillation frequency = 32768 × 0.9999817 ≈ 32767.4 Hz

Assume the target frequency to be 32768 Hz (32767.4 Hz + 18.3 ppm) and DEV to be 1.

The expression for calculating the correction value when DEV is 1 is applied.

Correction value = Number of correction counts in 1 minute
= (Oscillation frequency ÷ Target frequency − 1) × 32768 × 60
= (32767.4 ÷ 32768 − 1) × 32768 × 60
= −36

[Calculating the values to be set to (F6 to F0)]

(When the correction value is −36)

If the correction value is 0 or less (when speeding up), assume F6 to be 1.

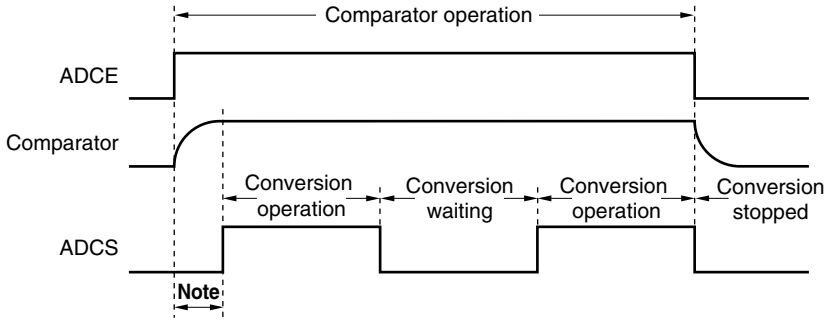
Calculate (F5, F4, F3, F2, F1, F0) from the correction value.

− {(/F5, /F4, /F3, /F2, /F1, /F0) + 1} × 2	= −36
(/F5, /F4, /F3, /F2, /F1, /F0)	= 17
(/F5, /F4, /F3, /F2, /F1, /F0)	= (0, 1, 0, 0, 0, 1)
(F5, F4, F3, F2, F1, F0)	= (1, 0, 1, 1, 1, 0)

Consequently, when correcting from 32767.4 Hz to 32768 Hz (32767.4 Hz + 18.3 ppm), setting the correction register such that DEV is 1 and the correction value is −36 (bits 6 to 0 of SUBCUD: 1101110) results in 32768 Hz (0 ppm).

Figure 9-27 shows the operation when (DEV, F6, F5, F4, F3, F2, F1, F0) is (1, 1, 1, 0, 1, 1, 1, 0).

Figure 12-4. Timing Chart When Comparator Is Used



Note To stabilize the internal circuit, the time from the rising of the ADCE bit to the falling of the ADCS bit must be 1 μs or longer.

Cautions 1. A/D conversion must be stopped before rewriting bits FR0 to FR3, LV1, and LV0 to values other than the identical data.

2. If data is written to ADM, a wait cycle is generated. Do not write data to ADM when the CPU is operating on the subsystem clock and the peripheral hardware clock is stopped. For details, see CHAPTER 33 CAUTIONS FOR WAIT.

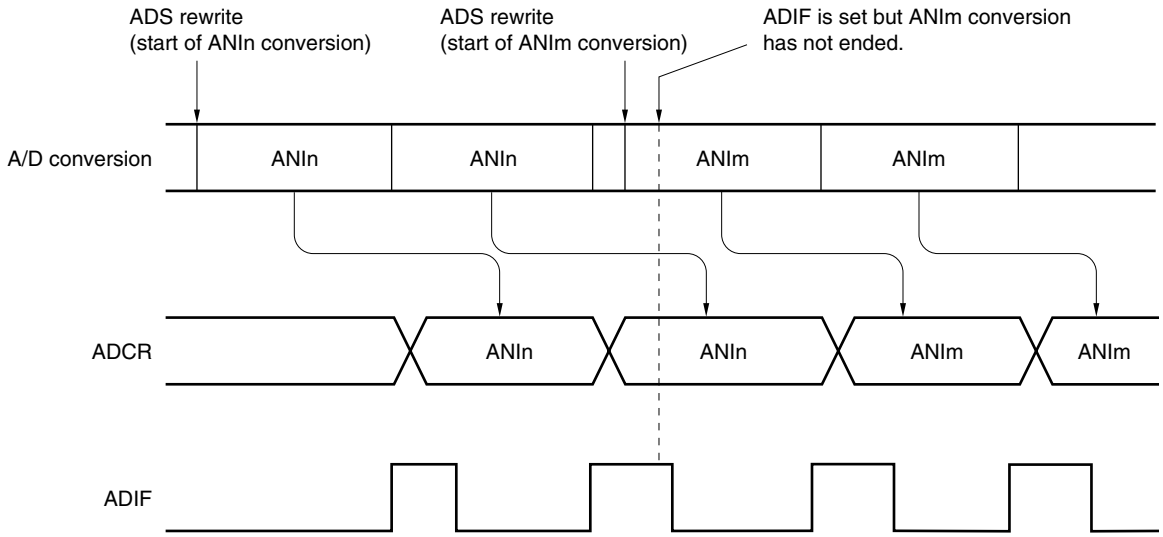
(8) Interrupt request flag (ADIF)

The interrupt request flag (ADIF) is not cleared even if the analog input channel specification register (ADS) is changed.

Therefore, if an analog input pin is changed during A/D conversion, the A/D conversion result and ADIF for the pre-change analog input may be set just before the ADS rewrite. Caution is therefore required since, at this time, when ADIF is read immediately after the ADS rewrite, ADIF is set despite the fact A/D conversion for the post-change analog input has not ended.

When A/D conversion is stopped and then resumed, clear ADIF before the A/D conversion operation is resumed.

Figure 12-21. Timing of A/D Conversion End Interrupt Request Generation



Remarks 1. n = 0 to 7

2. m = 0 to 7

(9) Conversion results just after A/D conversion start

The first A/D conversion value immediately after A/D conversion starts may not fall within the rating range if the ADCS bit is set to 1 within 1 μs after the ADCE bit was set to 1, or if the ADCS bit is set to 1 with the ADCE bit = 0. Take measures such as polling the A/D conversion end interrupt request (INTAD) and removing the first conversion result.

(10) A/D conversion result register (ADCR, ADCRH) read operation

When a write operation is performed to the A/D converter mode register (ADM), analog input channel specification register (ADS), and A/D port configuration register 0 (ADPC0), the contents of ADCR and ADCRH may become undefined. Read the conversion result following conversion completion before writing to ADM, ADS, and ADPC0. Using a timing other than the above may cause an incorrect conversion result to be read.

14.4.2 Asynchronous serial interface (UART) mode

In this mode, 1-byte data is transmitted/received following a start bit, and a full-duplex operation can be performed.

A dedicated UART baud rate generator is incorporated, so that communication can be executed at a wide range of baud rates.

(1) Registers used

- Asynchronous serial interface operation mode register 0 (ASIM0)
- Asynchronous serial interface reception error status register 0 (ASIS0)
- Baud rate generator control register 0 (BRGC0)
- Port mode register 1 (PM1)
- Port register 1 (P1)

The basic procedure of setting an operation in the UART mode is as follows.

<1> Set the BRGC0 register (see **Figure 14-4**).
<2> Set bits 1 to 4 (SL0, CL0, PS00, and PS01) of the ASIM0 register (see **Figure 14-2**).
<3> Set bit 7 (POWER0) of the ASIM0 register to 1.
<4> Set bit 6 (TXE0) of the ASIM0 register to 1. → Transmission is enabled.
Set bit 5 (RXE0) of the ASIM0 register to 1. → Reception is enabled.
<5> Write data to the TXS0 register. → Data transmission is started.

Caution Take relationship with the other party of communication when setting the port mode register and port register.

The relationship between the register settings and pins is shown below.

Table 14-2. Relationship Between Register Settings and Pins

POWER0	TXE0	RXE0	PM13	P13	PM12	P12	UART0 Operation	Pin Function	
								TxD0/SO10 /<TxD6>/P13	RxD0/SI10 /<RxD6>/P12
0	0	0	×Note	×Note	×Note	×Note	Stop	SO10/<TxD6>/P13	SI10/<RxD6>/P12
1	0	1	×Note	×Note	1	×	Reception	SO10/P13	RxD0
	1	0	0	×	×Note	×Note	Transmission	TxD0	SI10/P12
	1	1	0	×	1	×	Transmission/ reception	TxD0	RxD0

Note Can be set as port function, serial interface CSI10, or serial interface UART6 (only when UART0 is stopped).

Remark ×: don't care
POWER0: Bit 7 of asynchronous serial interface operation mode register 0 (ASIM0)
TXE0: Bit 6 of ASIM0
RXE0: Bit 5 of ASIM0
PM1×: Port mode register
P1×: Port output latch

(2) Generation of serial clock

A serial clock to be generated can be specified by using baud rate generator control register 0 (BRGC0).

Select the clock to be input to the 5-bit counter by using bits 7 and 6 (TPS01 and TPS00) of BRGC0.

Bits 4 to 0 (MDL04 to MDL00) of BRGC0 can be used to select the division value ($f_{XCLK0}/8$ to $f_{XCLK0}/31$) of the 5-bit counter.

14.4.4 Calculation of baud rate

(1) Baud rate calculation expression

The baud rate can be calculated by the following expression.

- Baud rate = $\frac{f_{XCLK0}}{2 \times k}$ [bps]

f_{XCLK0}: Frequency of base clock selected by the TPS01 and TPS00 bits of the BRGC0 register

k: Value set by the MDL04 to MDL00 bits of the BRGC0 register (k = 8, 9, 10, ..., 31)

Table 14-4. Set Value of TPS01 and TPS00

TPS01	TPS00	Base clock (f_{XCLK0}) selection[Note 1]				
			f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 8 MHz	f_{PRS} = 10 MHz
0	0	TM50 output[Note 2]				
0	1	$f_{PRS}/2$	1 MHz	2.5 MHz	4 MHz	5 MHz
1	0	$f_{PRS}/2^3$	250 kHz	625 kHz	1 MHz	1.25 MHz
1	1	$f_{PRS}/2^5$	62.5 kHz	156.25 kHz	250 kHz	312.5 kHz

Notes 1. If the peripheral hardware clock (f_{PRS}) operates on the high-speed system clock (f_{XH}) (XSEL = 1), the f_{PRS} operating frequency varies depending on the supply voltage.

- V_{DD} = 2.7 to 5.5 V: $f_{PRS} \leq$ 10 MHz
- V_{DD} = 1.8 to 2.7 V: $f_{PRS} \leq$ 5 MHz

2. Note the following points when selecting the TM50 output as the base clock.

- Mode in which the count clock is cleared and started upon a match of TM50 and CR50 (TMC506 = 0)
  Start the operation of 8-bit timer/event counter 50 first and then enable the timer F/F inversion operation (TMC501 = 1).
- PWM mode (TMC506 = 1)
  Start the operation of 8-bit timer/event counter 50 first and then set the count clock to make the duty = 50%.

It is not necessary to enable (TOE50 = 1) TO50 output in any mode.

(2) Error of baud rate

The baud rate error can be calculated by the following expression.

- Error (%) = $\left(\frac{\text{Actual baud rate (baud rate with error)}}{\text{Desired baud rate (correct baud rate)}} - 1\right) \times 100$ [%]

Cautions 1. Keep the baud rate error during transmission to within the permissible error range at the reception destination.

2. Make sure that the baud rate error during reception satisfies the range shown in (4) Permissible baud rate range during reception.

17.4.2 Setting method when using segment key scan function (KSON = 1)

When using the segment key scan function (KSON = 1), set the LCD controller/driver as follows. Set the LCD controller/driver using the following procedure.

<1> Set (VAON = 1) internal gate voltage boosting (bit 4 of the LCD display mode register (LCDM)).[Note 1]
<2> Set the resistance division method via MDSET0 and MDSET1 (bits 4 and 5 of the LCD mode register (LCDMD)) (MDSET0 = 0: external resistance division method, MDSET0 = 1: internal resistance division method).
Set (KSON = 1) KSON (bit 0 of the LCD mode register (LCDMD)).
<3> Set the pins to be used as segment outputs to the port function registers (PF2m, PFnALL).
<4> Use port mode register 4 (PM4) to set the pin to be used as a key scan input pin[Note 2] to PM4p = 1 (input mode).
<5> Use pull-up resistor option register 4 (PU4) to set the pin to be used as a key scan input pin[Note 2] to PU4p = 0 (connects an on-chip pull-up resistor only during the segment key scan output period).
<6> Use the key return mode register (KRM) to set the pin to be used as a segment key scan input pin to KRMp = 1[Note 3].
<7> Set an initial value to the RAM for LCD display.
<8> Set an initial value of segment key scan output to P14, P15.
<9> Set the number of time slices via LCDM0 to LCDM2 (bits 0 to 2 of the LCD display mode register (LCDM)).
<10> Set the LCD source clock and LCD clock via LCD clock control register 0 (LCDC0).
<11> Set (SCOC = 1) SCOC (bit 6 of the LCD display mode register (LCDM)).
Deselect signals are output from all the segment and common pins, and the non-display status is entered.
<12> Start output corresponding to each data memory by setting (LCDON = 1) LCDON (bit 7 of LCDM).

Hereinafter, set data to the data memory according to the contents displayed, and perform segment key scan output settings for the port registers (P14, P15) according to the contents of the segment key scan output.

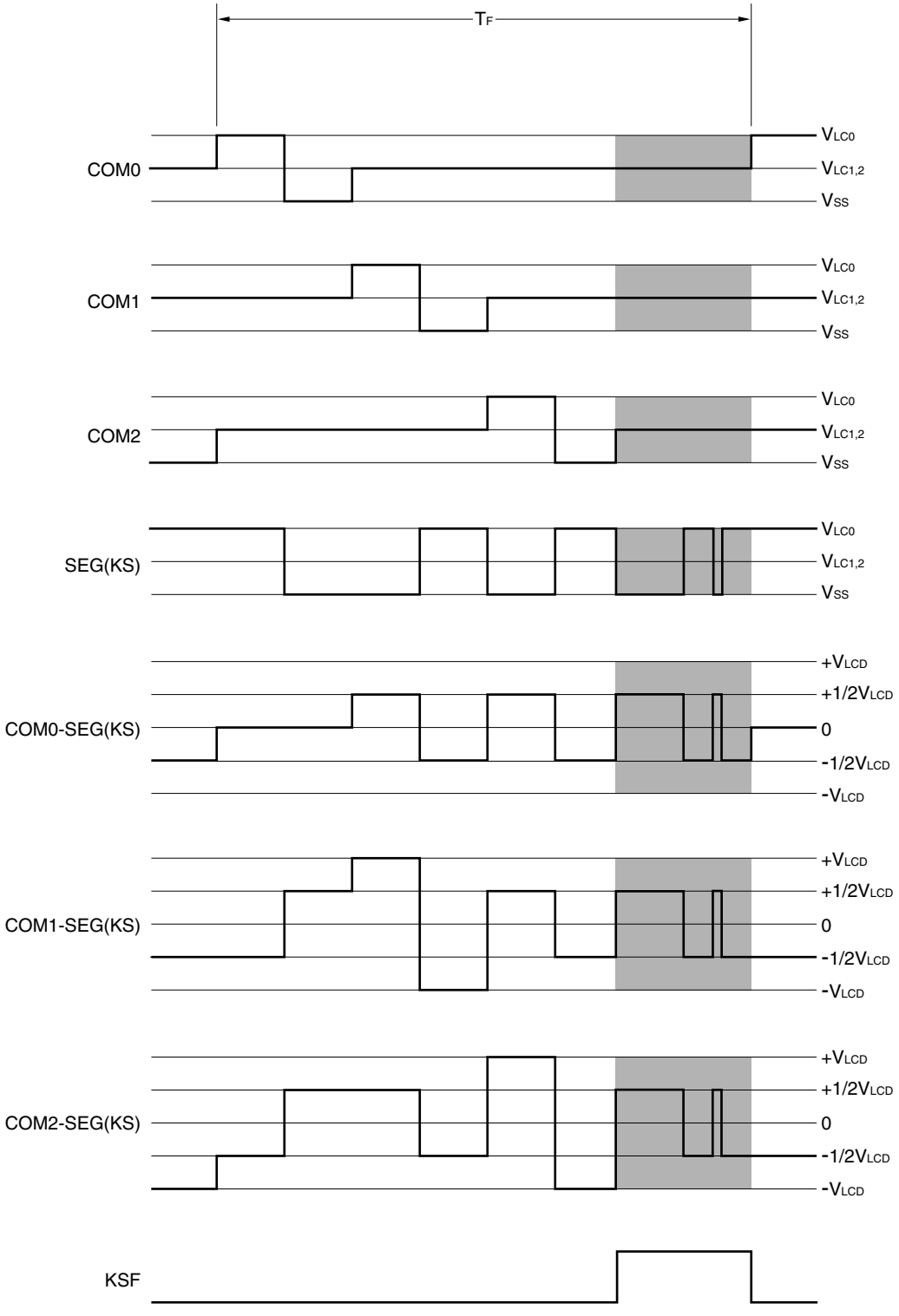
Notes 1. Set VAON based on the following conditions.
<When set to the 1/3 bias method>
- When 2.5 V ≤ V_{LCD} = V_{DD} ≤ 5.5 V: VAON = 0
- When 1.8 V ≤ V_{LCD} = V_{DD} ≤ 3.6 V: VAON = 1

<When set to the 1/2 bias method or 1/4 bias method >
- When 2.7 V ≤ V_{LCD} = V_{DD} ≤ 5.5 V: VAON = 0
- When 1.8 V ≤ V_{LCD} = V_{DD} ≤ 3.6 V: VAON = 1

2. When using the segment key scan function, be sure to set port 4 as a segment key scan input pin and the pull-up resistor option register of the port to be used to PU4p = 0 (connects an on-chip pull-up resistor only during the segment key scan output period).
An external pull-up resistor cannot be used, because it affects the LCD display output.

3. An interrupt request flag may be set when KRM has been changed. Consequently, change the KRM register after having disabled interrupts, and enable interrupts after having cleared the interrupt request flag.

<Key identification>

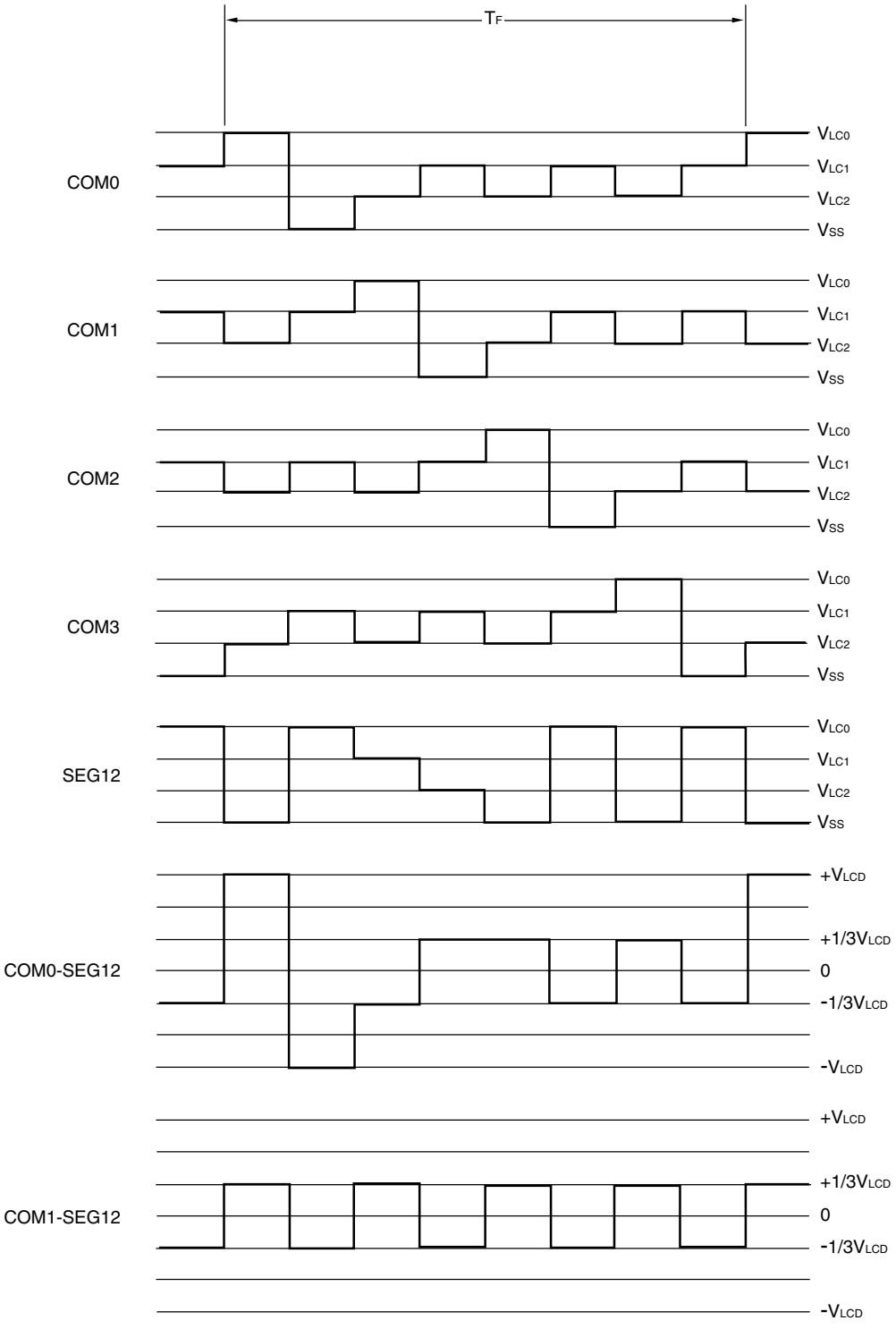


Shaded sections: Segment key scan output period

Remark During key identification, the residual charge of the LCD panel can be eliminated by outputting a signal with an inverted relationship between its first half and latter half.

Figure 17-29. Four-Time-Slice LCD Drive Waveform Examples (1/3 Bias Method)

(a) When segment key scan function is not used (KSON = 0)



Remark The waveforms for COM2 to SEG12 and COM3 to SEG12 are omitted.

(c) MCG control register 2 (MC0CTL2)

This register is used to set the transmit baud rate.

This register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 1FH.

Address: FF4EH After reset: 1FH R/W

Symbol	7	6	5	4	3	2	1	0
MC0CTL2	0	0	0	MC0BRS4	MC0BRS3	MC0BRS2	MC0BRS1	MC0BRS0

MC0BRS4	MC0BRS3	MC0BRS2	MC0BRS1	MC0BRS0	k	Output clock selection of 5-bit counter
0	0	0	×	×	4	$f_{XCLK}/4$
0	0	1	0	0	4	$f_{XCLK}/4$
0	0	1	0	1	5	$f_{XCLK}/5$
0	0	1	1	0	6	$f_{XCLK}/6$
0	0	1	1	1	7	$f_{XCLK}/7$
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
1	1	1	0	0	28	$f_{XCLK}/28$
1	1	1	0	1	29	$f_{XCLK}/29$
1	1	1	1	0	30	$f_{XCLK}/30$
1	1	1	1	1	31	$f_{XCLK}/31$

Cautions 1. Clear bit 7 (MC0PWR) of the MC0CTL0 register to 0 before rewriting the MC0BRS4 to MC0BRS0 bits.

2. The value from further dividing the output clock of the 5-bit counter by 2 is the baud rate value.

Remarks 1. f_{XCLK}: Frequency of the base clock selected by the MC0CKS2 to MC0CKS0 bits of the MC0CTL1 register

2. k: Value set by the MC0BRS4 to MC0BRS0 bits (k = 4, 5, 6, 7, …., 31)

3. ×: Don't care

<1> Baud rate

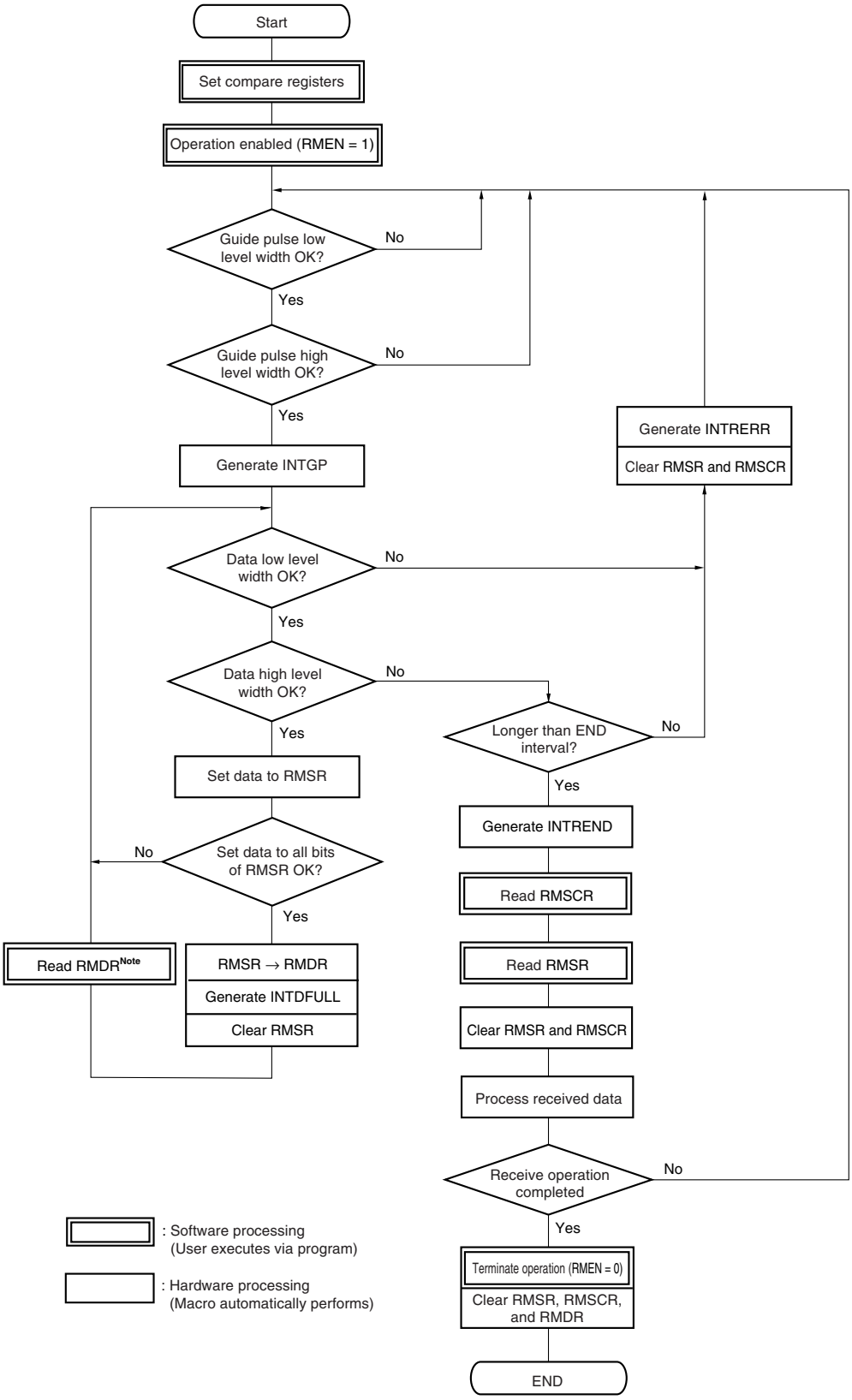
The baud rate can be calculated by the following expression.

- Baud rate = $\frac{f_{XCLK}}{2 \times k}$ [bps]

f_{XCLK}: Frequency of base clock selected by the MC0CKS2 to MC0CKS0 bits of the MC0CTL1 register

k: Value set by the MC0BRS4 to MC0BRS0 bits of the MC0CTL2 register (k = 4, 5, 6, ..., 31)

Figure 19-9. Operation Flow of Type B Reception Mode



Note Read RMDR before data has been set to all the bits of RMSR.

CHAPTER 24 POWER-ON-CLEAR CIRCUIT

24.1 Functions of Power-on-Clear Circuit

The power-on-clear circuit (POC) has the following functions.

- Generates internal reset signal at power on.
  In the 1.59 V POC mode (option byte: POCMODE = 0), the reset signal is released when the supply voltage (V_{DD}) exceeds 1.59 V ±0.15 V.
  In the 2.7 V/1.59 V POC mode (option byte: POCMODE = 1), the reset signal is released when the supply voltage (V_{DD}) exceeds 2.7 V ±0.2 V.

- Compares supply voltage (V_{DD}) and detection voltage (V_{POC} = 1.59 V ±0.15 V), generates internal reset signal when $V_{DD} < V_{POC}$.

Caution If an internal reset signal is generated in the POC circuit, the reset control flag register (RESF) is cleared to 00H.

Remark 78K0/LE3 incorporates multiple hardware functions that generate an internal reset signal. A flag that indicates the reset source is located in the reset control flag register (RESF) for when an internal reset signal is generated by the watchdog timer (WDT) or low-voltage-detector (LVI). RESF is not cleared to 00H and the flag is set to 1 when an internal reset signal is generated by WDT or LVI.
For details of RESF, see **CHAPTER 23 RESET FUNCTION**.

(3) 0084H/1084H

○ On-chip debug operation control

- Disabling on-chip debug operation
- Enabling on-chip debug operation and erasing data of the flash memory in case authentication of the on-chip debug security ID fails
- Enabling on-chip debug operation and not erasing data of the flash memory even in case authentication of the on-chip debug security ID fails

Caution To use the on-chip debug function, set 02H or 03H to 0084H. Set a value that is the same as that of 0084H to 1084H because 0084H and 1084H are switched during the boot operation.