Renesas Electronics America Inc - UPD78F0453GB-GAH-AX Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	3-Wire SIO, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	46
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0453gb-gah-ax

[MEMO]

Other Documents

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE − Products and Packages −	X13769X
Semiconductor Device Mount Manual	**Note**
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

Note See the “Semiconductor Device Mount Manual” website (http://www.necel.com/pkg/en/mount/index.html).

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document when designing.

(3/3)

Item \ Part Number			78K0/LF3													
			μPD78F047x					μPD78F048x					μPD78F049x				
			80 Pins														
Flash memory (KB)			16	24	32	48	60	16	24	32	48	60	16	24	32	48	60
RAM (KB)			0.75	1	1	2	2	0.75	1	1	2	2	0.75	1	1	2	2
Power supply voltage			V_{DD} = 1.8 to 5.5 V														
Regulator			Provided														
Minimum instruction execution time			0.2 μs (10 MHz: V_{DD} = 2.7 to 5.5 V)/ 0.4 μs (5 MHz: V_{DD} = 1.8 to 5.5 V)														
Clock	Main	High-speed system clock	10 MHz: V_{DD} = 2.7 to 5.5 V/5 MHz: V_{DD} = 1.8 to 5.5 V														
		Internal high-speed oscillation clock	8 MHz (TYP.): V_{DD} = 1.8 to 5.5 V														
	Subclock		32.768 kHz (TYP.): V_{DD} = 1.8 to 5.5 V														
	Internal low-speed oscillation clock		240 kHz (TYP.): V_{DD} = 1.8 to 5.5 V														
Port	Total		62														
Timer	16 bits (TM0)		1 ch														
	8 bits (TM5)		3 ch														
	8 bits (TMH)		3 ch														
	RTC		1 ch														
	WDT		1 ch														
Serial interface	3-wire CSI/UART[Note 1]		1 ch														
	Automatic transmit/ receive 3-wire CSI		1 ch														
	UART supporting LIN-bus[Note 2]		1 ch														
LCD	Type		External resistance division and internal resistance division are switchable.														
	Segment signal		40 (36) [36 (32)] [Note 3, 4]										32 (28) [28 (24)] [Note 3, 4]				
	Common signal		4 (8)[Note 3]														
10-bit successive approximation type A/D			–					8 ch									
16-bit ΔΣ type A/D			–										3 ch				
Interrupt	External		7														
	Internal		20					21					22				
Segment key source signal output			8 ch														
Key interrupt			8 ch														
Reset	$\overline{\text{RESET}}$ pin		Provided														
	POC		1.59 V ±0.15 V (Time for rising up to 1.8 V : 3.6 ms (MAX.))														
	LVI		The detection level of the supply voltage is selectable in 16 steps.														
	WDT		Provided														
Clock output/ Buzzer output			Provided														
Remote controller receiver			Provided														
MCG			Provided														
On-chip debug function			Provided														
Operating ambient temperature			T_A = −40 to +85°C														

Notes 1. Select either of the functions of these alternate-function pins.

2. The LIN-bus supporting UART pins can be changed to the Automatic transmit/receive 3-wire CSI/UART pins (pin numbers 75 and 76).

3. The values in parentheses are the number of signal outputs when 8com is used.

<R> **4.** The values in square brackets are the number of signal outputs when using the UART6 pins (RxD6, TxD6) on the bottom side.

Table 3-8. Special Function Register List (1/5)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulatable Bit Unit			After Reset
				1 Bit	8 Bits	16 Bits	
FF00H	Receive buffer register 6	RXB6	R	–	√	–	FFH
FF01H	Port register 1	P1	R/W	√	√	–	00H
FF02H	Port register 2	P2	R/W	√	√	–	00H
FF03H	Port register 3	P3	R/W	√	√	–	00H
FF04H	Port register 4	P4	R/W	√	√	–	00H
FF05H	Transmit buffer register 6	TXB6	R/W	–	√	–	FFH
FF06H	10-bit A/D conversion result register[Note]	ADCR	R	–	–	√	0000H
FF07H	8-bit A/D conversion result register H[Note]	ADCRH	R	–	√	–	00H
FF08H	Port register 8	P8	R/W	√	√	–	00H
FF0AH	Port register 10	P10	R/W	√	√	–	00H
FF0BH	Port register 11	P11	R/W	√	√	–	00H
FF0CH	Port register 12	P12	R/W	√	√	–	00H
FF0EH	Port register 14	P14	R/W	√	√	–	00H
FF0FH	Port register 15	P15	R/W	√	√	–	00H
FF10H	16-bit timer counter 00	TM00	R	–	–	√	0000H
FF11H							
FF12H	16-bit timer capture/compare register 000	CR000	R/W	–	–	√	0000H
FF13H							
FF14H	16-bit timer capture/compare register 010	CR010	R/W	–	–	√	0000H
FF15H							
FF16H	8-bit timer counter 50	TM50	R	–	√	–	00H
FF17H	8-bit timer compare register 50	CR50	R/W	–	√	–	00H
FF18H	8-bit timer H compare register 00	CMP00	R/W	–	√	–	00H
FF19H	8-bit timer H compare register 10	CMP10	R/W	–	√	–	00H
FF1AH	8-bit timer H compare register 01	CMP01	R/W	–	√	–	00H
FF1BH	8-bit timer H compare register 11	CMP11	R/W	–	√	–	00H
FF1FH	Serial I/O shift register 10	SIO10	R	–	√	–	00H
FF20H	Port function register 1	PF1	R/W	√	√	–	00H
FF21H	Port mode register 1	PM1	R/W	√	√	–	FFH
FF22H	Port mode register 2	PM2	R/W	√	√	–	FFH
FF23H	Port mode register 3	PM3	R/W	√	√	–	FFH
FF24H	Port mode register 4	PM4	R/W	√	√	–	FFH
FF28H	Port mode register 8	PM8	R/W	√	√	–	FFH
FF2AH	Port mode register 10	PM10	R/W	√	√	–	FFH
FF2BH	Port mode register 11	PM11	R/W	√	√	–	FFH
FF2CH	Port mode register 12	PM12	R/W	√	√	–	FFH
FF2EH	Port mode register 14	PM14	R/W	√	√	–	FFH
FF2FH	Port mode register 15	PM15	R/W	√	√	–	FFH
FF30H	Internal high-speed oscillation trimming register	HIOTRM	R/W	–	√	–	10H
FF31H	Pull-up resistor option register 1	PU1	R/W	√	√	–	00H
FF33H	Pull-up resistor option register 3	PU3	R/W	√	√	–	00H

Note μPD78F045x and 78F046x only.

Table 5-8. Maximum Time Required for Main System Clock Switchover

Set Value Before Switchover	Set Value After Switchover	
MCM0	MCM0	
	0	1
0		1 + 2f_{RH}/f_{XH} clock
1	1 + 2f_{XH}/f_{RH} clock	

Caution When switching the internal high-speed oscillation clock to the high-speed system clock, bit 2 (XSEL) of MCM must be set to 1 in advance. The value of XSEL can be changed only once after a reset release.

Remarks 1. The number of clocks listed in Table 5-8 is the number of main system clocks before switchover.

2. Calculate the number of clocks in Table 5-8 by removing the decimal portion.

Example When switching the main system clock from the internal high-speed oscillation clock to the high-speed system clock (@ oscillation with f_{RH} = 8 MHz, f_{XH} = 10 MHz)

$1 + 2f_{RH}/f_{XH} = 1 + 2 \times 8/10 = 1 + 2 \times 0.8 = 1 + 1.6 = 2.6 \rightarrow 2$ clocks

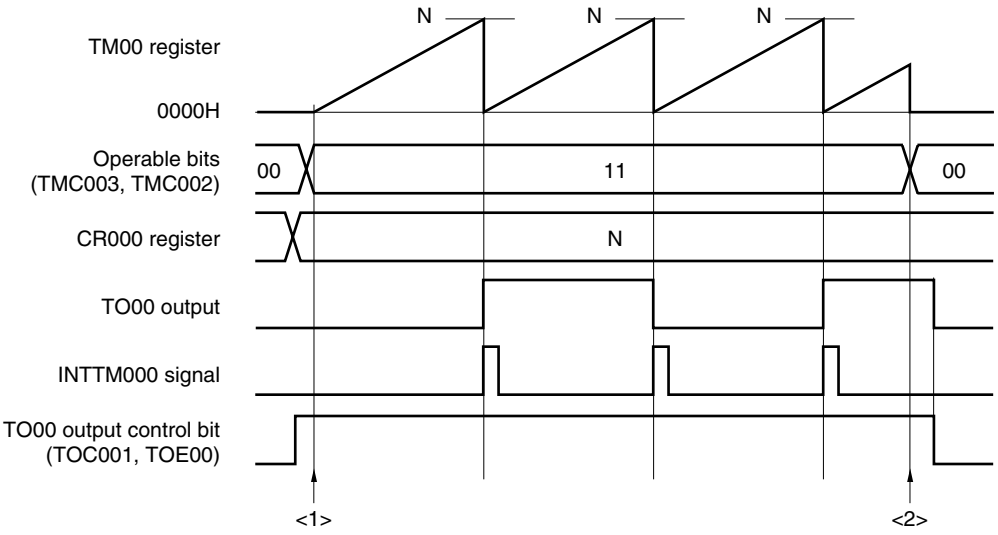
5.6.9 Conditions before clock oscillation is stopped

The following lists the register flag settings for stopping the clock oscillation (disabling external clock input) and conditions before the clock oscillation is stopped.

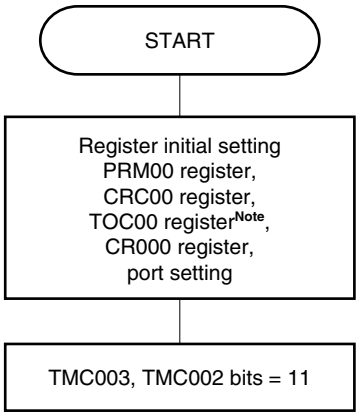
Table 5-9. Conditions Before the Clock Oscillation Is Stopped and Flag Settings

Clock	Conditions Before Clock Oscillation Is Stopped (External Clock Input Disabled)	Flag Settings of SFR Register
Internal high-speed oscillation clock	MCS = 1 or CLS = 1 (The CPU is operating on a clock other than the internal high-speed oscillation clock)	RSTOP = 1
X1 clock	MCS = 0 or CLS = 1 (The CPU is operating on a clock other than the high-speed system clock)	MSTOP = 1
External main system clock		
XT1 clock	CLS = 0 (The CPU is operating on a clock other than the subsystem clock)	OSCSELS = 0

Figure 6-19. Example of Software Processing for Square Wave Output Function



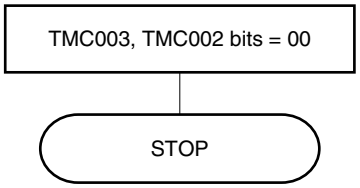
<1> Count operation start flow



Initial setting of these registers is performed before setting the TMC003 and TMC002 bits to 11.

Starts count operation

<2> Count operation stop flow



The counter is initialized and counting is stopped by clearing the TMC003 and TMC002 bits to 00.

Note Care must be exercised when setting TOC00. For details, see **6.3 (3) 16-bit timer output control register 00 (TOC00)**.

6.4.5 Free-running timer operation

When bits 3 and 2 (TMC003 and TMC002) of 16-bit timer mode control register 00 (TMC00) are set to 01 (free-running timer mode), 16-bit timer/event counter 00 continues counting up in synchronization with the count clock. When it has counted up to FFFFH, the overflow flag (OVF00) is set to 1 at the next clock, and TM00 is cleared (to 0000H) and continues counting. Clear OVF00 to 0 by executing the CLR instruction via software.

The following three types of free-running timer operations are available.

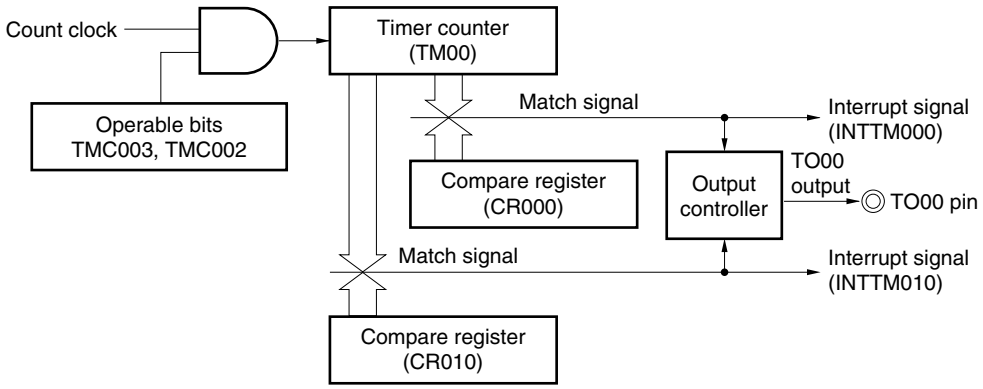
- Both CR000 and CR010 are used as compare registers.
- One of CR000 or CR010 is used as a compare register and the other is used as a capture register.
- Both CR000 and CR010 are used as capture registers.

Remarks 1. For the setting of the I/O pins, see **6.3 (6) Port mode register 3 (PM3)**.

2. For how to enable the INTTM000 signal interrupt, see **CHAPTER 20 INTERRUPT FUNCTIONS**.

(1) Free-running timer mode operation
(CR000: compare register, CR010: compare register)

Figure 6-33. Block Diagram of Free-Running Timer Mode (CR000: Compare Register, CR010: Compare Register)



12.6 Cautions for 10-bit successive approximation type A/D Converter

(1) Operating current in STOP mode

The A/D converter stops operating in the STOP mode. At this time, the operating current can be reduced by clearing bit 7 (ADCS) and bit 0 (ADCE) of the A/D converter mode register (ADM) to 0.

To restart from the standby status, clear bit 0 (ADIF) of interrupt request flag register 1L (IF1L) to 0 and start operation.

(2) Input range of ANI0 to ANI7

Observe the rated range of the ANI0 to ANI7 input voltage. If a voltage of AV_{REF} or higher and AV_{SS} or lower (even in the range of absolute maximum ratings) is input to an analog input channel, the converted value of that channel becomes undefined. In addition, the converted values of the other channels may also be affected.

(3) Conflicting operations

<1> Conflict between A/D conversion result register (ADCR, ADCRH) write and ADCR or ADCRH read by instruction upon the end of conversion

ADCR or ADCRH read has priority. After the read operation, the new conversion result is written to ADCR or ADCRH.

<2> Conflict between ADCR or ADCRH write and A/D converter mode register (ADM) write, analog input channel specification register (ADS), or A/D port configuration register 0 (ADPC0) write upon the end of conversion

ADM, ADS, or ADPC0 write has priority. ADCR or ADCRH write is not performed, nor is the conversion end interrupt signal (INTAD) generated.

(4) Noise countermeasures

To maintain the 10-bit resolution, attention must be paid to noise input to the AV_{REF} pin and pins ANI0 to ANI7.

<1> Connect a capacitor with a low equivalent resistance and a good frequency response to the power supply.

<2> The higher the output impedance of the analog input source, the greater the influence. To reduce the noise, connecting external C as shown in Figure 12-20 is recommended.

<3> Do not switch these pins with other pins during conversion.

<4> The accuracy is improved if the HALT mode is set immediately after the start of conversion.

14.3 Registers Controlling Serial Interface UART0

Serial interface UART0 is controlled by the following six registers.

- Asynchronous serial interface operation mode register 0 (ASIM0)
- Asynchronous serial interface reception error status register 0 (ASIS0)
- Baud rate generator control register 0 (BRGC0)
- Port function register 1 (PF1)
- Port mode register 1 (PM1)
- Port register 1 (P1)

(1) Asynchronous serial interface operation mode register 0 (ASIM0)

This 8-bit register controls the serial communication operations of serial interface UART0.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 01H.

Figure 14-2. Format of Asynchronous Serial Interface Operation Mode Register 0 (ASIM0) (1/2)

Address: FF70H After reset: 01H R/W

Symbol	<7>	<6>	<5>	4	3	2	1	0
ASIM0	POWER0	TXE0	RXE0	PS01	PS00	CL0	SL0	1

POWER0	Enables/disables operation of internal operation clock
0[Note 1]	Disables operation of the internal operation clock (fixes the clock to low level) and asynchronously resets the internal circuit[Note 2].
1	Enables operation of the internal operation clock.

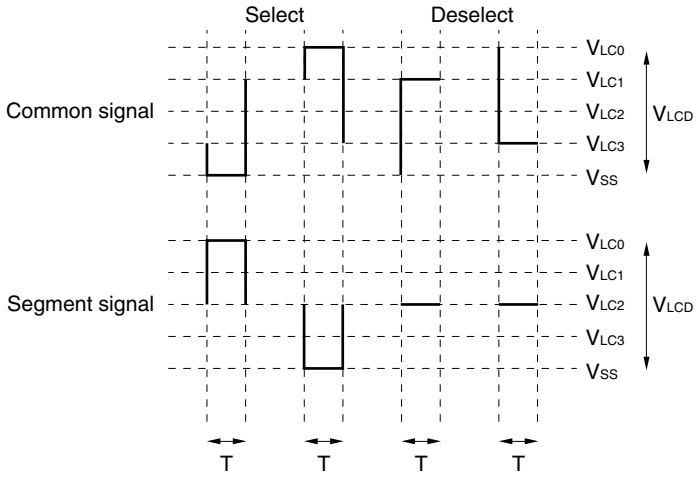
TXE0	Enables/disables transmission
0	Disables transmission (synchronously resets the transmission circuit).
1	Enables transmission.

RXE0	Enables/disables reception
0	Disables reception (synchronously resets the reception circuit).
1	Enables reception.

Notes 1. The input from the RxD0 pin is fixed to high level when POWER0 = 0.

2. Asynchronous serial interface reception error status register 0 (ASIS0), transmit shift register 0 (TXS0), and receive buffer register 0 (RXB0) are reset.

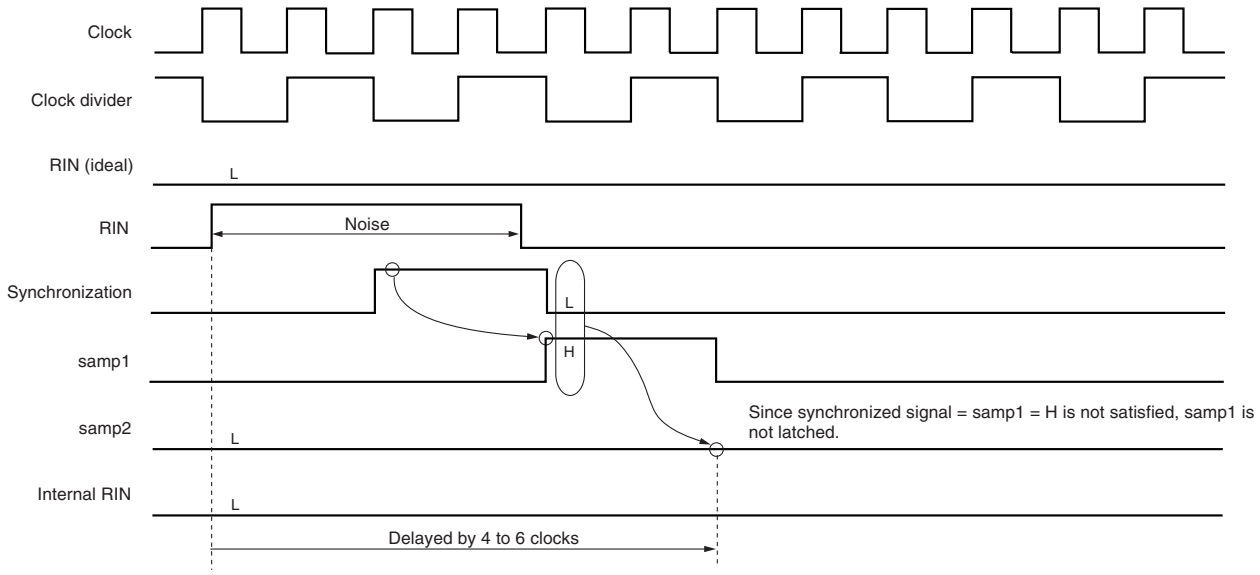
(d) 1/4 bias method



T: One LCD clock period

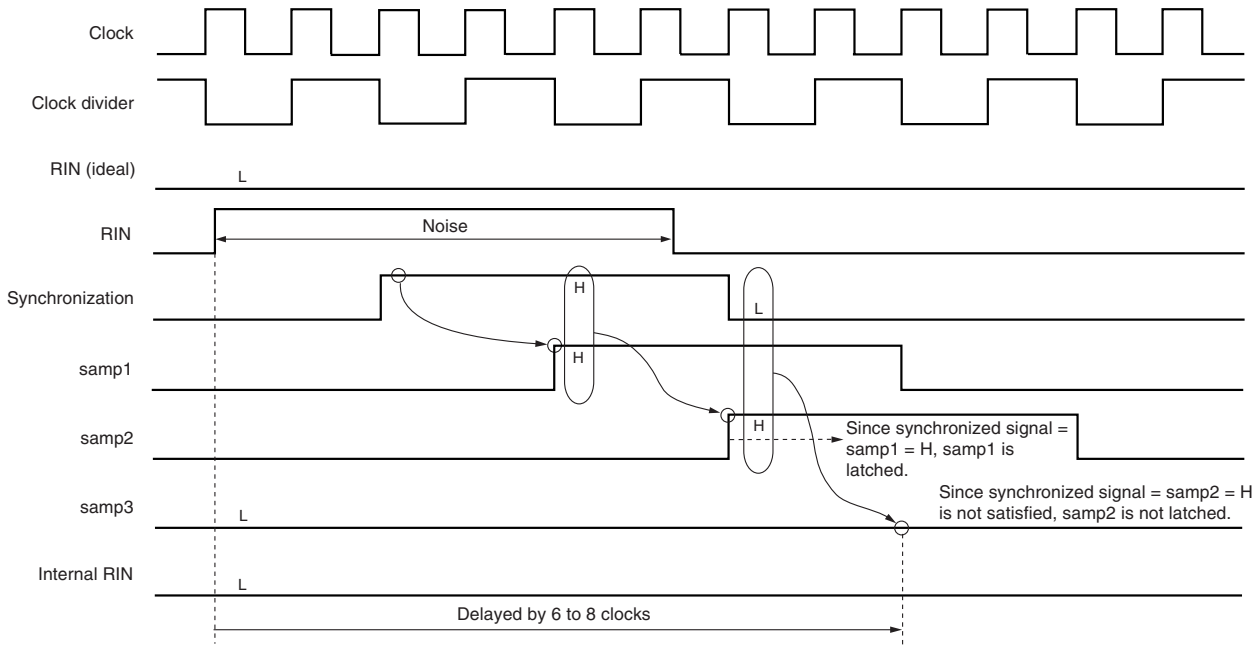
Figure 19-16. Noise Elimination Operation Example (2/2)

(c) 2-clock noise elimination (PRSEN = 1, NCW = 0)



Remark Internal RIN is a signal after synchronization and sampling are performed twice, and is therefore later than the actual signal input from the outside to the RIN pin by 4 to 6 clocks.

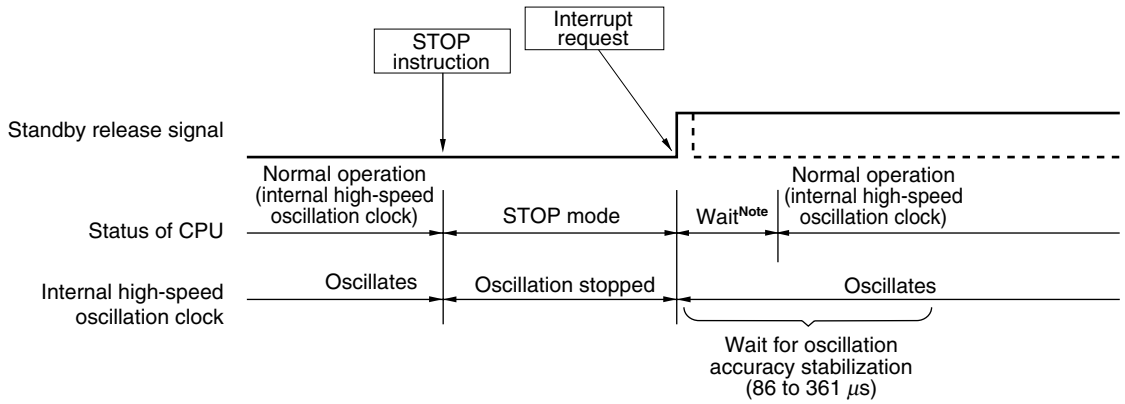
(d) 4-clock noise elimination (PRSEN = 1, NCW = 1)



Remark Internal RIN is a signal after synchronization and sampling are performed three times, and is therefore later than the actual signal input from the outside to the RIN pin by 6 to 8 clocks.

Figure 22-6. STOP Mode Release by Interrupt Request Generation (2/2)

(3) When internal high-speed oscillation clock is used as CPU clock



Note The wait time is as follows:

- When vectored interrupt servicing is carried out: 8 or 9 clocks
- When vectored interrupt servicing is not carried out: 2 or 3 clocks

Remark The broken lines indicate the case when the interrupt request that has released the standby mode is acknowledged.

Table 23-1. Operation Statuses During Reset Period

Item		During Reset Period
System clock		Clock supply to the CPU is stopped.
Main system clock	f_{RH}	Operation stopped
	f_X	Operation stopped (pin is I/O port mode)
	f_{EXCLK}	Clock input invalid (pin is I/O port mode)
Subsystem clock	f_{XT}	Operation stopped (pin is I/O port mode)
f_{RL}		Operation stopped
CPU		
Flash memory		
RAM		
Port (latch)		
16-bit timer/event counter 00		
8-bit timer/event counter	50	
	51	
	52	
8-bit timer	H0	
	H1	
	H2	
Real-time counter		
Watchdog timer		
Buzzer output		
10-bit successive approximation type A/D converter		
16-bit ΔΣ type A/D converter		
Serial interface	UART0	
	UART6	
	CSI10	
LCD controller/driver		
Manchester code generator		
Remote controller receiver		
Power-on-clear function		Operable
Low-voltage detection function		Operation stopped
External interrupt		

Remark f_{RH}: Internal high-speed oscillation clock
f_X: X1 oscillation clock
f_{EXCLK}: External main system clock
f_{XT}: XT1 oscillation clock
f_{RL}: Internal low-speed oscillation clock

(2) Low-voltage detection level selection register (LVIS)

This register selects the low-voltage detection level.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

The generation of a reset signal other than an LVI reset clears this register to 00H.

Figure 25-3. Format of Low-Voltage Detection Level Selection Register (LVIS)

Address: FFBFH After reset: 00H[Note] R/W

Symbol	7	6	5	4	3	2	1	0
LVIS	0	0	0	0	LVIS3	LVIS2	LVIS1	LVIS0

LVIS3	LVIS2	LVIS1	LVIS0	Detection level
0	0	0	0	V_{LVI0} (4.24 V ±0.1 V)
0	0	0	1	V_{LVI1} (4.09 V ±0.1 V)
0	0	1	0	V_{LVI2} (3.93 V ±0.1 V)
0	0	1	1	V_{LVI3} (3.78 V ±0.1 V)
0	1	0	0	V_{LVI4} (3.62 V ±0.1 V)
0	1	0	1	V_{LVI5} (3.47 V ±0.1 V)
0	1	1	0	V_{LVI6} (3.32 V ±0.1 V)
0	1	1	1	V_{LVI7} (3.16 V ±0.1 V)
1	0	0	0	V_{LVI8} (3.01 V ±0.1 V)
1	0	0	1	V_{LVI9} (2.85 V ±0.1 V)
1	0	1	0	V_{LVI10} (2.70 V ±0.1 V)
1	0	1	1	V_{LVI11} (2.55 V ±0.1 V)
1	1	0	0	V_{LVI12} (2.39 V ±0.1 V)
1	1	0	1	V_{LVI13} (2.24 V ±0.1 V)
1	1	1	0	V_{LVI14} (2.08 V ±0.1 V)
1	1	1	1	V_{LVI15} (1.93 V ±0.1 V)

Note The value of LVIS is not reset but retained as is, upon a reset by LVI. It is cleared to 00H upon other resets.

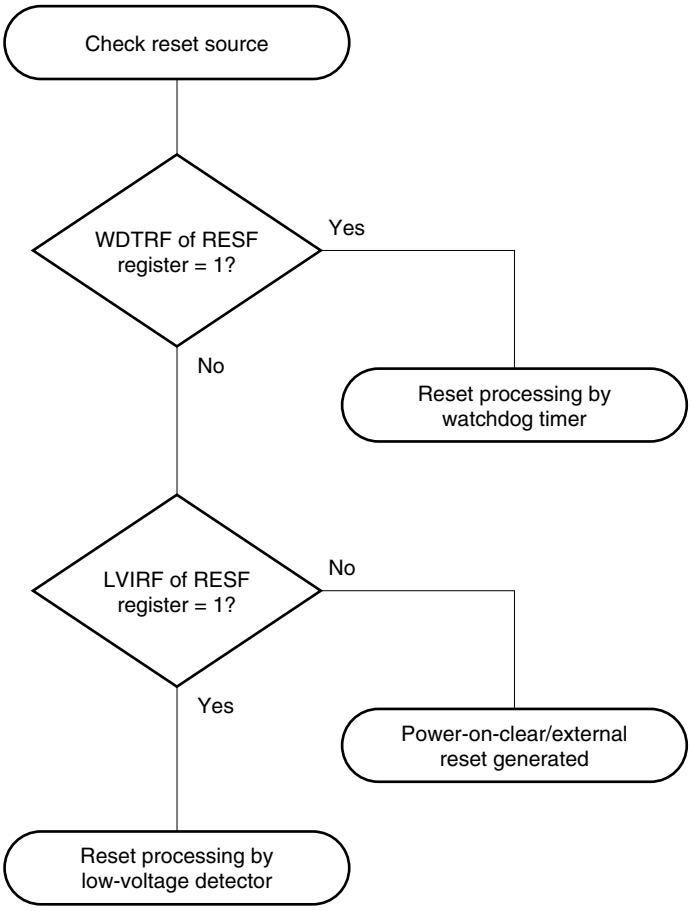
Cautions 1. Be sure to clear bits 4 to 7 to "0".

2. Do not change the value of LVIS during LVI operation.

3. When an input voltage from the external input pin (EXLVI) is detected, the detection voltage (V_{EXLVI} = 1.21 V (TYP.)) is fixed. Therefore, setting of LVIS is not necessary.

Figure 25-9. Example of Software Processing After Reset Release (2/2)

• Checking reset source



27.7.3 Selecting communication mode

In the 78K0/LE3, a communication mode is selected by inputting pulses to the FLMD0 pin after the dedicated flash memory programming mode is entered. These FLMD0 pulses are generated by the flash memory programmer.

The following table shows the relationship between the number of pulses and communication modes.

Table 27-7. Communication Modes

Communication Mode	Standard Setting[Note 1]				Pins Used	Peripheral Clock	Number of FLMD0 Pulses
	Port	Speed	Frequency	Multiply Rate			
UART (UART6)	UART-Ext-OSC	115,200 bps[Note 3]	2 M to 10 MHz[Note 2]	1.0	TxD6, RxD6	f_X	0
	UART-Ext-FP5CLK					f_{EXCLK}	3
<R>	UART-Internal-OSC		–			f_{RH}	5
3-wire serial I/O (CSI10)	CSI-Internal-OSC	2.4 kHz to 2.5 MHz	–		SO10, SI10, $\overline{SCK10}$	f_{RH}	8

Notes 1. Selection items for Standard settings on GUI of the flash memory programmer.

2. The possible setting range differs depending on the voltage. For details, see **CHAPTER 30 ELECTRICAL SPECIFICATIONS (STANDARD PRODUCTS)**.

3. Because factors other than the baud rate error, such as the signal waveform slew, also affect UART communication, thoroughly evaluate the slew as well as the baud rate error.

Caution When UART6 is selected, the receive clock is calculated based on the reset command sent from the dedicated flash memory programmer after the FLMD0 pulse has been received.

Remark f_X: X1 clock
f_{EXCLK}: External main system clock
f_{RH}: Internal high-speed oscillation clock

Table 27-10. Relationship Between Enabling Security Function and Command

(1) During on-board/off-board programming

Valid Security	Executed Command		
	Batch Erase (Chip Erase)	Block Erase	Write
Prohibition of batch erase (chip erase)	Cannot be erased in batch	Blocks cannot be erased.	Can be performed[Note].
Prohibition of block erase	Can be erased in batch.		Can be performed.
Prohibition of writing			Cannot be performed.
Prohibition of rewriting boot cluster 0	Cannot be erased in batch	Boot cluster 0 cannot be erased.	Boot cluster 0 cannot be written.

Note Confirm that no data has been written to the write area. Because data cannot be erased after batch erase (chip erase) is prohibited, do not write data if the data has not been erased.

(2) During self programming

Valid Security	Executed Command	
	Block Erase	Write
Prohibition of batch erase (chip erase)	Blocks can be erased.	Can be performed.
Prohibition of block erase		
Prohibition of writing		
Prohibition of rewriting boot cluster 0	Boot cluster 0 cannot be erased.	Boot cluster 0 cannot be written.

Table 27-11 shows how to perform security settings in each programming mode.

Table 27-11. Setting Security in Each Programming Mode

(1) On-board/off-board programming

Security	Security Setting	How to Disable Security Setting
Prohibition of batch erase (chip erase)	Set via GUI of dedicated flash memory programmer, etc.	Cannot be disabled after set.
Prohibition of block erase		Execute batch erase (chip erase) command
Prohibition of writing		
Prohibition of rewriting boot cluster 0		Cannot be disabled after set.

(2) Self programming

Security	Security Setting	How to Disable Security Setting
Prohibition of batch erase (chip erase)	Set by using information library.	Cannot be disabled after set.
Prohibition of block erase		Execute batch erase (chip erase) command during on-board/off-board programming (cannot be disabled during self programming)
Prohibition of writing		
Prohibition of rewriting boot cluster 0		Cannot be disabled after set.

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag
				Note 1	Note 2		Z AC CY
16-bit data transfer	**MOVW**	rp, #word	3	6	–	rp ← word	
		saddrp, #word	4	8	10	(saddrp) ← word	
		sfrp, #word	4	–	10	sfrp ← word	
		AX, saddrp	2	6	8	AX ← (saddrp)	
		saddrp, AX	2	6	8	(saddrp) ← AX	
		AX, sfrp	2	–	8	AX ← sfrp	
		sfrp, AX	2	–	8	sfrp ← AX	
		AX, rp Note 3	1	4	–	AX ← rp	
		rp, AX Note 3	1	4	–	rp ← AX	
		AX, !addr16	3	10	12	AX ← (addr16)	
		!addr16, AX	3	10	12	(addr16) ← AX	
	XCHW	AX, rp Note 3	1	4	–	AX ↔ rp	
8-bit operation	**ADD**	A, #byte	2	4	–	A, CY ← A + byte	× × ×
		saddr, #byte	3	6	8	(saddr), CY ← (saddr) + byte	× × ×
		A, r Note 4	2	4	–	A, CY ← A + r	× × ×
		r, A	2	4	–	r, CY ← r + A	× × ×
		A, saddr	2	4	5	A, CY ← A + (saddr)	× × ×
		A, !addr16	3	8	9	A, CY ← A + (addr16)	× × ×
		A, [HL]	1	4	5	A, CY ← A + (HL)	× × ×
		A, [HL + byte]	2	8	9	A, CY ← A + (HL + byte)	× × ×
		A, [HL + B]	2	8	9	A, CY ← A + (HL + B)	× × ×
		A, [HL + C]	2	8	9	A, CY ← A + (HL + C)	× × ×
	ADDC	A, #byte	2	4	–	A, CY ← A + byte + CY	× × ×
		saddr, #byte	3	6	8	(saddr), CY ← (saddr) + byte + CY	× × ×
		A, r Note 4	2	4	–	A, CY ← A + r + CY	× × ×
		r, A	2	4	–	r, CY ← r + A + CY	× × ×
		A, saddr	2	4	5	A, CY ← A + (saddr) + CY	× × ×
		A, !addr16	3	8	9	A, CY ← A + (addr16) + C	× × ×
		A, [HL]	1	4	5	A, CY ← A + (HL) + CY	× × ×
		A, [HL + byte]	2	8	9	A, CY ← A + (HL + byte) + CY	× × ×
		A, [HL + B]	2	8	9	A, CY ← A + (HL + B) + CY	× × ×
		A, [HL + C]	2	8	9	A, CY ← A + (HL + C) + CY	× × ×

Notes 1. When the internal high-speed RAM area is accessed or for an instruction with no data access

2. When an area except the internal high-speed RAM area is accessed

3. Only when rp = BC, DE or HL

4. Except “r = A”

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

2. This clock cycle applies to the internal ROM program.

CHAPTER 30 ELECTRICAL SPECIFICATIONS (STANDARD PRODUCTS)

<R> **Caution The 78K0/LE3 has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. NEC Electronics is not liable for problems occurring when the on-chip debug function is used.**

Absolute Maximum Ratings (T_A = 25°C) (1/2)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		−0.5 to +6.5	V
	V_{SS}		−0.5 to +0.3	V
	AV_{REF} Note 2		−0.5 to V_{DD} + 0.3 Note 1	V
	AV_{SS} Note 2		−0.5 to +0.3	V
REGC pin input voltage	V_{IREGC}		−0.5 to + 3.6 and −0.5 to V_{DD}	V
Input voltage	V_I	P11 to P14, P20 to P27, P31 to P34, P40 to P44, P80 to P83, P100 to P103, P110 to P113, P120 to P124, P140 to P143, P150 to P153, X1, X2, XT1, XT2, FLMD0, $\overline{\text{RESET}}$	−0.3 to V_{DD} + 0.3 Note 1	V
Output voltage	V_O		−0.3 to V_{DD} + 0.3 Note 1	V
Analog input voltage	V_{AN}	ANI0 to ANI7 Note 2, DS0− to DS2− Note 3, DS0+ to DS2+ Note 3	−0.3 to AV_{REF} + 0.3 Note 1 and −0.3 to V_{DD} + 0.3 Note 1	V
	REF+ Note 3		−0.5 to AV_{REF} + 0.3 Note 1	V
	REF− Note 3		−0.5 to + 0.3	V

Notes 1. Must be 6.5 V or lower.

2. μPD78F045x and 78F046x only.

3. μPD78F046x only.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (3/5)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P11 to P14, P31 to P34, P40 to P44, P80 to P83, P100 to P103, P110 to P113, P120, P140 to P143, P150 to P153, FLMD0, $\overline{\text{RESET}}$	$V_I = V_{DD}$				1	μA
	I_{LIH2}	P20 to P27	$V_I = AV_{REF} = V_{DD}$				1	μA
	I_{LIH3}	P121 to 124 (X1, X2, XT1, XT2)	$V_I = V_{DD}$	I/O port mode			1	μA
				OSC mode			20	μA
Input leakage current, low	I_{LIL1}	P11 to P14, P31 to P34, P40 to P44, P80 to P83, P100 to P103, P110 to P113, P120, P140 to P143, P150 to P153, FLMD0, $\overline{\text{RESET}}$	$V_I = V_{SS}$				–1	μA
	I_{LIL2}	P20 to P27	$V_I = V_{SS}$, $AV_{REF} = V_{DD}$				–1	μA
	I_{LIL3}	P121 to 124 (X1, X2, XT1, XT2)	$V_I = V_{SS}$	I/O port mode			–1	μA
				OSC mode			–20	μA
Pull-up resistor	R_U	$V_I = V_{SS}$			10	20	100	kΩ
FLMD0 supply voltage	V_{IL}	In normal operation mode			0		$0.2V_{DD}$	V
	V_{IH}	In self-programming mode			$0.8V_{DD}$		V_{DD}	V

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.