Renesas Electronics America Inc - UPD78F0454GB-GAH-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	3-Wire SIO, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	46
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0454gb-gah-ax

(3/3)

Item \ Part Number			78K0/LF3													
			μPD78F047x					μPD78F048x					μPD78F049x				
			80 Pins														
Flash memory (KB)			16	24	32	48	60	16	24	32	48	60	16	24	32	48	60
RAM (KB)			0.75	1	1	2	2	0.75	1	1	2	2	0.75	1	1	2	2
Power supply voltage			V_{DD} = 1.8 to 5.5 V														
Regulator			Provided														
Minimum instruction execution time			0.2 μs (10 MHz: V_{DD} = 2.7 to 5.5 V)/ 0.4 μs (5 MHz: V_{DD} = 1.8 to 5.5 V)														
Clock	Main	High-speed system clock	10 MHz: V_{DD} = 2.7 to 5.5 V/5 MHz: V_{DD} = 1.8 to 5.5 V														
		Internal high-speed oscillation clock	8 MHz (TYP.): V_{DD} = 1.8 to 5.5 V														
	Subclock		32.768 kHz (TYP.): V_{DD} = 1.8 to 5.5 V														
	Internal low-speed oscillation clock		240 kHz (TYP.): V_{DD} = 1.8 to 5.5 V														
Port	Total		62														
Timer	16 bits (TM0)		1 ch														
	8 bits (TM5)		3 ch														
	8 bits (TMH)		3 ch														
	RTC		1 ch														
	WDT		1 ch														
Serial interface	3-wire CSI/UART[Note 1]		1 ch														
	Automatic transmit/ receive 3-wire CSI		1 ch														
	UART supporting LIN-bus[Note 2]		1 ch														
LCD	Type		External resistance division and internal resistance division are switchable.														
	Segment signal		40 (36) [36 (32)] [Note 3, 4]										32 (28) [28 (24)] [Note 3, 4]				
	Common signal		4 (8)[Note 3]														
10-bit successive approximation type A/D			–					8 ch									
16-bit ΔΣ type A/D			–										3 ch				
Interrupt	External		7														
	Internal		20					21					22				
Segment key source signal output			8 ch														
Key interrupt			8 ch														
Reset	$\overline{\text{RESET}}$ pin		Provided														
	POC		1.59 V ±0.15 V (Time for rising up to 1.8 V : 3.6 ms (MAX.))														
	LVI		The detection level of the supply voltage is selectable in 16 steps.														
	WDT		Provided														
Clock output/ Buzzer output			Provided														
Remote controller receiver			Provided														
MCG			Provided														
On-chip debug function			Provided														
Operating ambient temperature			T_A = −40 to +85°C														

Notes 1. Select either of the functions of these alternate-function pins.

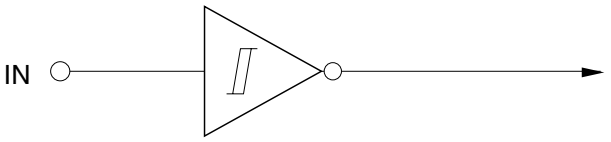
2. The LIN-bus supporting UART pins can be changed to the Automatic transmit/receive 3-wire CSI/UART pins (pin numbers 75 and 76).

3. The values in parentheses are the number of signal outputs when 8com is used.

<R> **4.** The values in square brackets are the number of signal outputs when using the UART6 pins (RxD6, TxD6) on the bottom side.

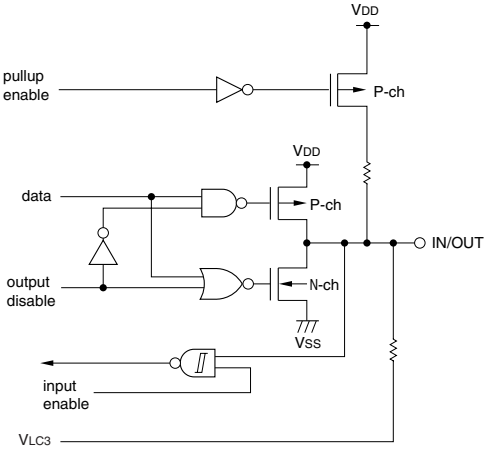
Figure 2-1. Pin I/O Circuit List (1/2)

Type 2

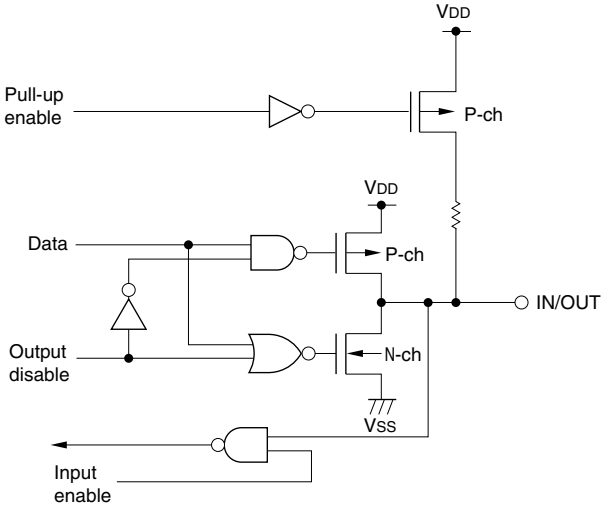


Schmitt-triggered input with hysteresis characteristics

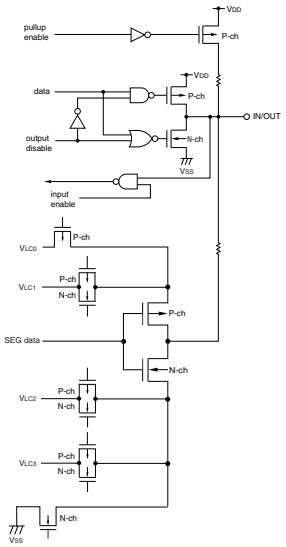
Type 5-AO



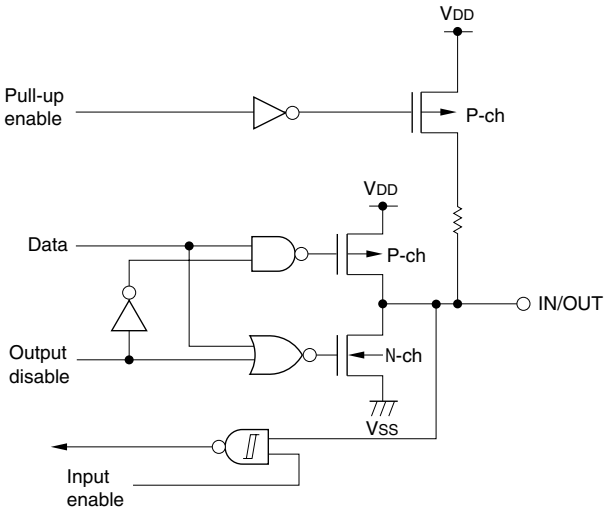
Type 5-AG



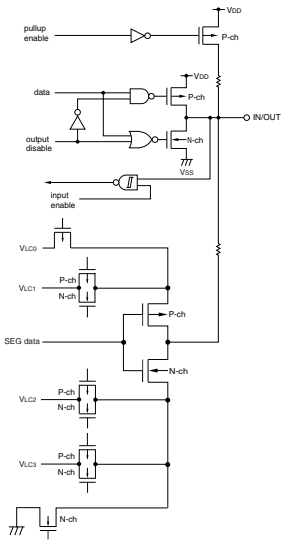
Type 17-P



Type 5-AH



Type 17-Q



(2) CALLT instruction table area

The 64-byte area 0040H to 007FH can store the subroutine entry address of a 1-byte call instruction (CALLT).

(3) Option byte area

A 5-byte area of 0080H to 0084H and 1080H to 1084H can be used as an option byte area. Set the option byte at 0080H to 0084H when the boot swap is not used, and at 0080H to 0084H and 1080H to 1084H when the boot swap is used. For details, see **CHAPTER 26 OPTION BYTE**.

(4) CALLF instruction entry area

The area 0800H to 0FFFH can perform a direct subroutine call with a 2-byte call instruction (CALLF).

(5) On-chip debug security ID setting area

A 10-byte area of 0085H to 008EH and 1085H to 108EH can be used as an on-chip debug security ID setting area. Set the on-chip debug security ID of 10 bytes at 0085H to 008EH when the boot swap is not used and at 0085H to 008EH and 1085H to 108EH when the boot swap is used. For details, see **CHAPTER 28 ON-CHIP DEBUG FUNCTION**.

Figure 3-19. Correspondence Between Data Memory and Addressing (μPD78F0445, 78F0455)

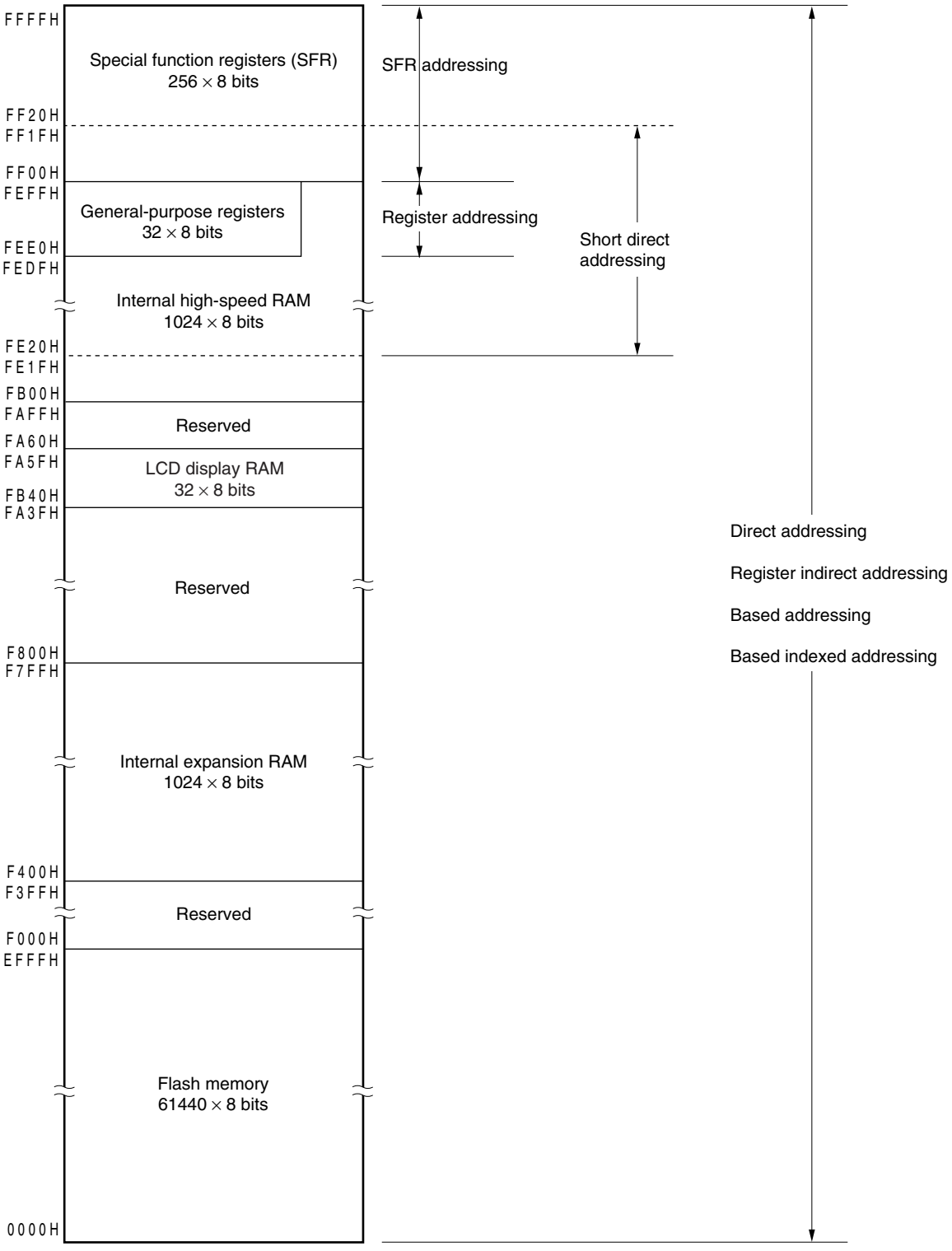
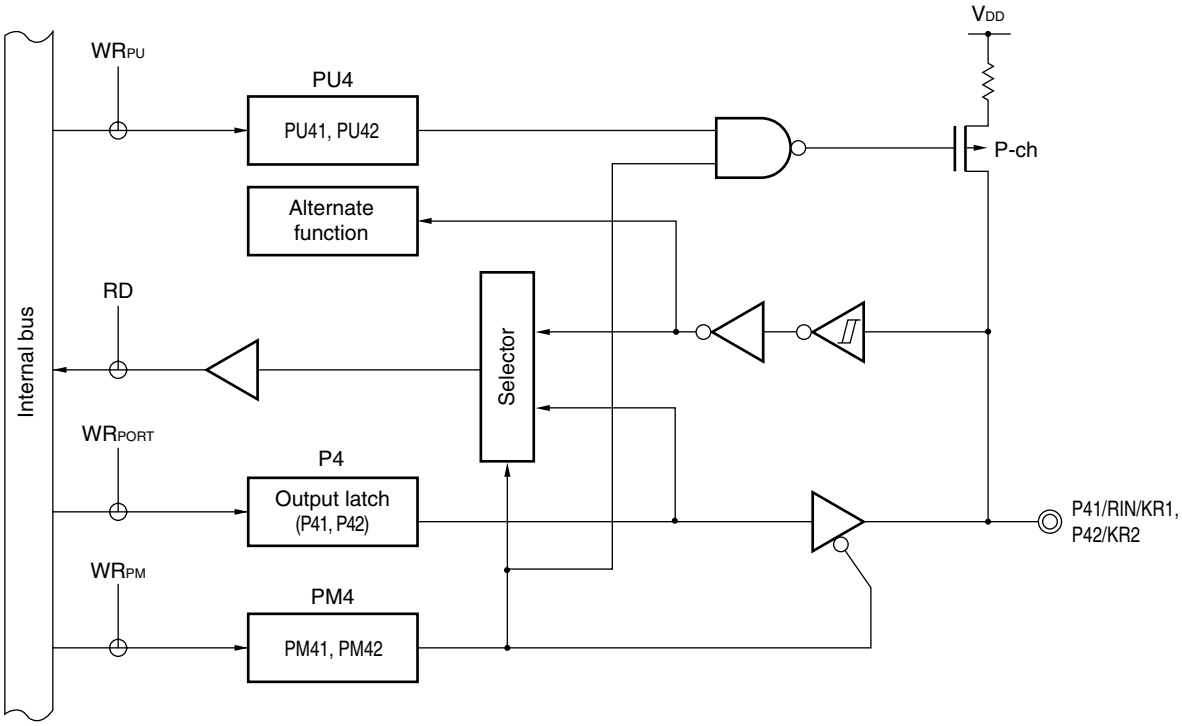


Figure 4-9. Block Diagram of P41 and P42



P4: Port register 4
PU4: Pull-up resistor option register 4
PM4: Port mode register 4
RD: Read signal
WR××: Write signal

Figure 6-21. Example of Register Settings in External Event Counter Mode (2/2)

(e) 16-bit timer counter 00 (TM00)

By reading TM00, the count value can be read.

(f) 16-bit capture/compare register 000 (CR000)

If M is set to CR000, the interrupt signal (INTTM000) is generated when the number of external events reaches (M + 1).

Setting CR000 to 0000H is prohibited.

(g) 16-bit capture/compare register 010 (CR010)

Usually, CR010 is not used in the external event counter mode. However, a compare match interrupt (INTTM010) is generated when the set value of CR010 matches the value of TM00.

Therefore, mask the interrupt request by using the interrupt mask flag (TMMK010).

6.6 Cautions for 16-Bit Timer/Event Counter 00

(1) Restrictions for each channel of 16-bit timer/event counter 00

Table 6-3 shows the restrictions for each channel.

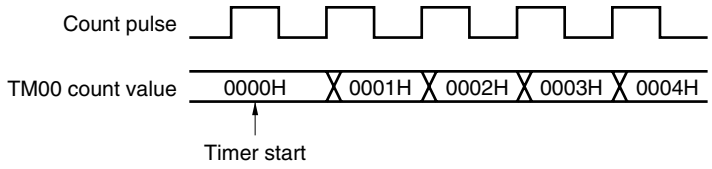
Table 6-3. Restrictions for Each Channel of 16-Bit Timer/Event Counter 00

Operation	Restriction
As interval timer	–
As square wave output	
As external event counter	
As clear & start mode entered by TI000 pin valid edge input	Using timer output (TO00) is prohibited when detection of the valid edge of the TI010 pin is used. (TOC00 = 00H)
As free-running timer	–
As PPG output	0000H ≤ CR010 < CR000 ≤ FFFFH
As one-shot pulse output	Setting the same value to CR000 and CR010 is prohibited.
As pulse width measurement	Using timer output (TO00) is prohibited (TOC00 = 00H)

(2) Timer start errors

An error of up to one clock may occur in the time required for a match signal to be generated after timer start. This is because counting TM00 is started asynchronously to the count pulse.

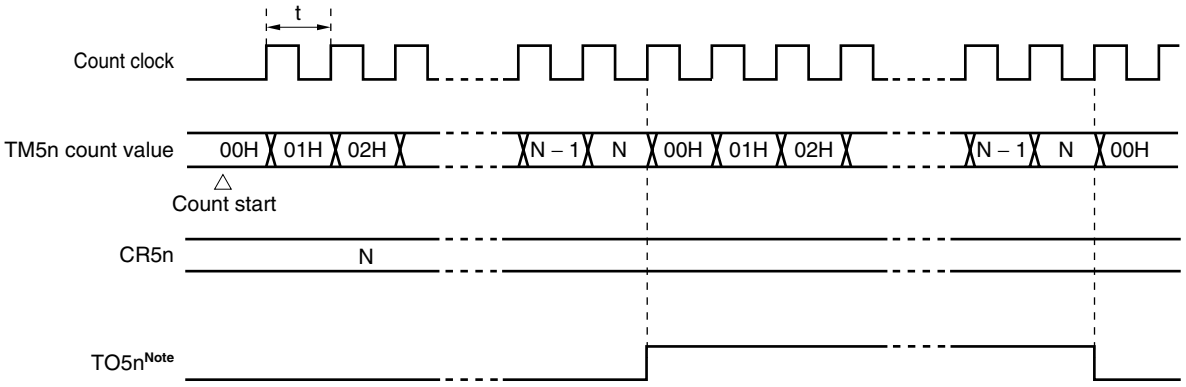
Figure 6-59. Start Timing of TM00 Count



(3) Setting of CR000 and CR010 (clear & start mode entered upon a match between TM00 and CR000)

Set a value other than 0000H to CR000 and CR010 (TM00 cannot count one pulse when it is used as an external event counter).

Figure 7-17. Square-Wave Output Operation Timing



Note The initial value of TO5n output can be set by bits 2 and 3 (LVR5n, LVS5n) of 8-bit timer mode control register 5n (TMC5n).

7.4.4 PWM output operation

8-bit timer/event counter 5n operates as a PWM output when bit 6 (TMC5n6) of 8-bit timer mode control register 5n (TMC5n) is set to 1.

The duty pulse determined by the value set to 8-bit timer compare register 5n (CR5n) is output from TO5n.

Set the active level width of the PWM pulse to CR5n; the active level can be selected with bit 1 (TMC5n1) of TMC5n.

The count clock can be selected with bits 0 to 2 (TCL5n0 to TCL5n2) of timer clock selection register 5n (TCL5n).

PWM output can be enabled/disabled with bit 0 (TOE5n) of TMC5n.

Caution In PWM mode, make the CR5n rewrite period 3 count clocks of the count clock (clock selected by TCL5n) or more.

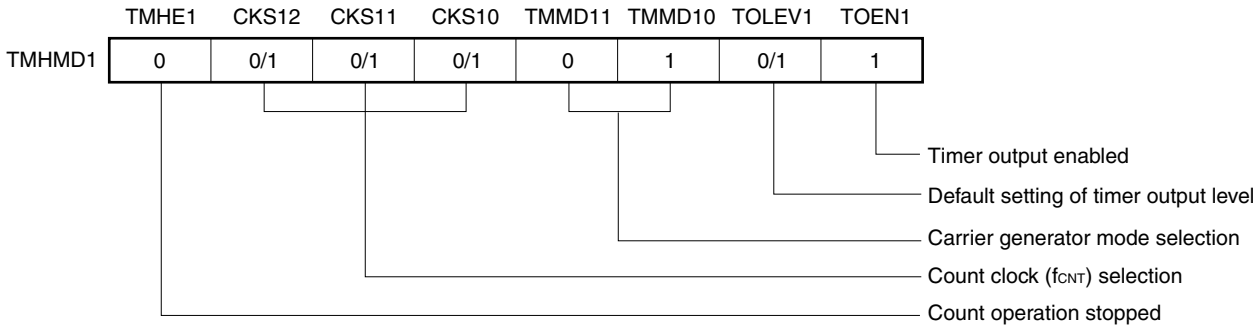
Remark n = 0, 1

Setting

<1> Set each register.

Figure 8-16. Register Setting in Carrier Generator Mode

(i) Setting 8-bit timer H mode register 1 (TMHMD1)



(ii) CMP01 register setting

- Compare value

(iii) CMP11 register setting

- Compare value

(iv) TMCYC1 register setting

- RMC1 = 1 ... Remote control output enable bit
- NRZB1 = 0/1 ... carrier output enable bit

(v) TCL51 and TMC51 register setting

- See **7.3 Registers Controlling 8-Bit Timer/Event Counters 50, 51, and 52**.

<2> When TMHE1 = 1, the 8-bit timer H1 starts counting.

<3> When TCE51 of the 8-bit timer mode control register 51 (TMC51) is set to 1, the 8-bit timer/event counter 51 starts counting.

<4> After the count operation is enabled, the first compare register to be compared is the CMP01 register. When the count value of the 8-bit timer counter H1 and the CMP01 register value match, the INTTMH1 signal is generated, the 8-bit timer counter H1 is cleared. At the same time, the compare register to be compared with the 8-bit timer counter H1 is switched from the CMP01 register to the CMP11 register.

<5> When the count value of the 8-bit timer counter H1 and the CMP11 register value match, the INTTMH1 signal is generated, the 8-bit timer counter H1 is cleared. At the same time, the compare register to be compared with the 8-bit timer counter H1 is switched from the CMP11 register to the CMP01 register.

<6> By performing procedures <4> and <5> repeatedly, a carrier clock is generated.

<7> The INTTM51 signal is synchronized with count clock of the 8-bit timer H1 and output as the INTTM5H1 signal. The INTTM5H1 signal becomes the data transfer signal for the NRZB1 bit, and the NRZB1 bit value is transferred to the NRZ1 bit.

<8> Write the next value to the NRZB1 bit in the interrupt servicing program that has been started by the INTTM5H1 interrupt or after timing has been checked by polling the interrupt request flag. Write data to count the next time to the CR51 register.

<9> When the NRZ1 bit is high level, a carrier clock is output by TOH1 output.

(6) Port mode register 2 (PM2)

When using the ANI0/P20 to ANI7/P27 pins for analog input port, set PM20 to PM27 to 1. The output latches of P20 to P27 at this time may be 0 or 1.

If PM20 to PM27 are set to 0, they cannot be used as analog input port pins.

PM2 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

Figure 12-10. Format of Port Mode Register 2 (PM2)

Address: FF22H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20

PM2n	P2n pin I/O mode selection (n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

ANI0/P20 to ANI7/P27 pins are as shown below depending on the settings of PF2, ADPC0, PM2, ADS, and ADDCTL0.

Table 12-3. Setting Functions of P20/ANI0 to P27/ANI7 Pins

(a) μPD78F045x

PF2	ADPC0	PM2	ADS	P20/SEG31/ANI0 to P27/SEG24/ANI7 Pins
Digital/Analog selection	Analog input selection	Input mode	Does not select ANI.	Analog input (not to be converted)
			Selects ANI.	Analog input (to be converted by successive approximation type A/D converter)
		Output mode	–	Setting prohibited
	Digital I/O selection	Input mode	–	Digital input
		Output mode	–	Digital output
SEG output selection	–	–	–	Segment output

(b) μPD78F046x

ADPC0	PM2	ADS	ADDCTL0	P20/ANI0/DS0- to P27/ANI7/REF+ Pins
Analog input selection	Input mode	Does not select ANI.	Does not select DSn±.	Analog input (not to be converted)
		Selects ANI.	Does not select DSn±.	Analog input (to be converted by successive approximation type A/D converter)
		Does not select ANI.	Selects DSn±.	Analog input (to be converted by ΔΣ type A/D converter)
		Selects ANI.	Selects DSn±.	Setting prohibited
	Output mode	–		Setting prohibited
Digital I/O selection	Input mode	–		Digital input
	Output mode	–		Digital output

15.4.2 Asynchronous serial interface (UART) mode

In this mode, data of 1 byte is transmitted/received following a start bit, and a full-duplex operation can be performed.

A dedicated UART baud rate generator is incorporated, so that communication can be executed at a wide range of baud rates.

(1) Registers used

- Asynchronous serial interface operation mode register 6 (ASIM6)
- Asynchronous serial interface reception error status register 6 (ASIS6)
- Asynchronous serial interface transmission status register 6 (ASIF6)
- Clock selection register 6 (CKSR6)
- Baud rate generator control register 6 (BRGC6)
- Asynchronous serial interface control register 6 (ASICL6)
- Input switch control register (ISC)
- Port mode register 1 (PM1)
- Port register 1 (P1)
- Port mode register 11 (PM11)
- Port register 11 (P11)

The basic procedure of setting an operation in the UART mode is as follows.

<1> Set the CKSR6 register (see **Figure 15-8**).
<2> Set the BRGC6 register (see **Figure 15-9**).
<3> Set bits 0 to 4 (ISRM6, SL6, CL6, PS60, PS61) of the ASIM6 register (see **Figure 15-5**).
<4> Set bits 0 and 1 (TXDLV6, DIR6) of the ASICL6 register (see **Figure 15-10**).
<5> Set bit 7 (POWER6) of the ASIM6 register to 1.
<6> Set bit 6 (TXE6) of the ASIM6 register to 1. → Transmission is enabled.
Set bit 5 (RXE6) of the ASIM6 register to 1. → Reception is enabled.
<7> Write data to transmit buffer register 6 (TXB6). → Data transmission is started.

Caution Take relationship with the other party of communication when setting the port mode register and port register.

17.6 Common and Segment Signals

Each pixel of the LCD panel turns on when the potential difference between the corresponding common and segment signals becomes higher than a specific voltage (LCD drive voltage, V_{LCD}). The pixels turn off when the potential difference becomes lower than V_{LCD}.

Applying DC voltage to the common and segment signals of an LCD panel causes deterioration. To avoid this problem, this LCD panel is driven by AC voltage.

(1) Common signals

Each common signal is selected sequentially according to a specified number of time slices at the timing listed in Table 17-3. In the static display mode, the same signal is output to COM0 to COM3.

When using the segment key scan output function (KSON = 1), segment key scan output will be performed for a period of one time slice after one LCD output cycle. The common signal generated at that time will not be displayed when output.

In the two-time-slice mode, leave the COM2 and COM3 pins open. In the three-time-slice mode, leave the COM3 pin open.

Use the COM4 to COM7 pins other than in the eight-time-slice mode as open or segment pins.

Table 17-3. COM Signals

Number of Time Slices \ COM Signal	COM0	COM1	COM2	COM3	COM4	COM5	COM6	COM7
Static display mode					**Note 2**	**Note 2**	**Note 2**	**Note 2**
Two-time-slice mode[Note 1]			Open	Open	**Note 2**	**Note 2**	**Note 2**	**Note 2**
Three-time-slice mode[Note 1]				Open	**Note 2**	**Note 2**	**Note 2**	**Note 2**
Four-time-slice mode[Note 1]					**Note 2**	**Note 2**	**Note 2**	**Note 2**
eight-time-slice mode[Note 1]								

Notes 1. When using the segment key scan output function (KSON = 1), non-display output will be performed for a period of one time slice after one LCD output cycle.

2. Use the pins as open or segment pins.

(2) Segment signals

(a) μPD78F044x, 78F045x

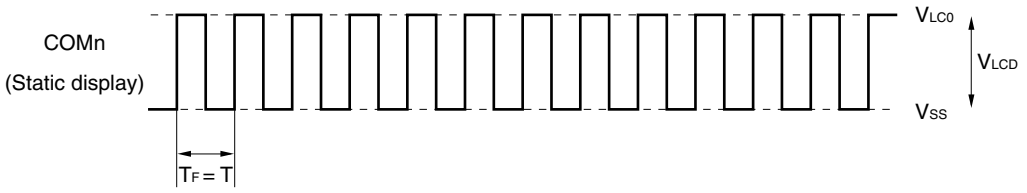
The segment signals correspond to 32 bytes of the LCD display data memory (FA40H to FA5FH) during an LCD display period, bits 0, 1, 2, and 3 of each byte are read in synchronization with COM0, COM1, COM2, and COM3, respectively. If a bit is 1, it is converted to the select voltage, and if it is 0, it is converted to the deselect voltage. The conversion results are output to the segment pins (SEG0 to SEG31).

Furthermore, segment signals correspond to the setting values of port registers 14 and 15 during a segment key scan output period. Bits 0 to 3 and bits 4 to 7 of each port register will be read in synchronization with the first half and latter half of the segment key scan output period, respectively, and if the content of each bit is 1 or 0, high levels or low levels will be output to the segment pins (SEG16 to SEG23), respectively.

Figure 17-13 shows the common signal waveforms, and Figure 17-14 shows the voltages and phases of the common and segment signals.

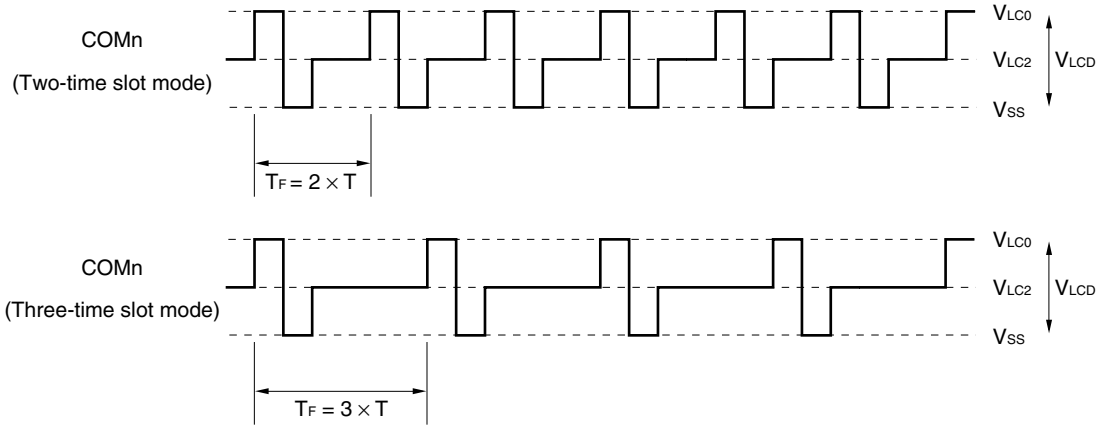
Figure 17-13. Common Signal Waveforms

(a) Static display mode



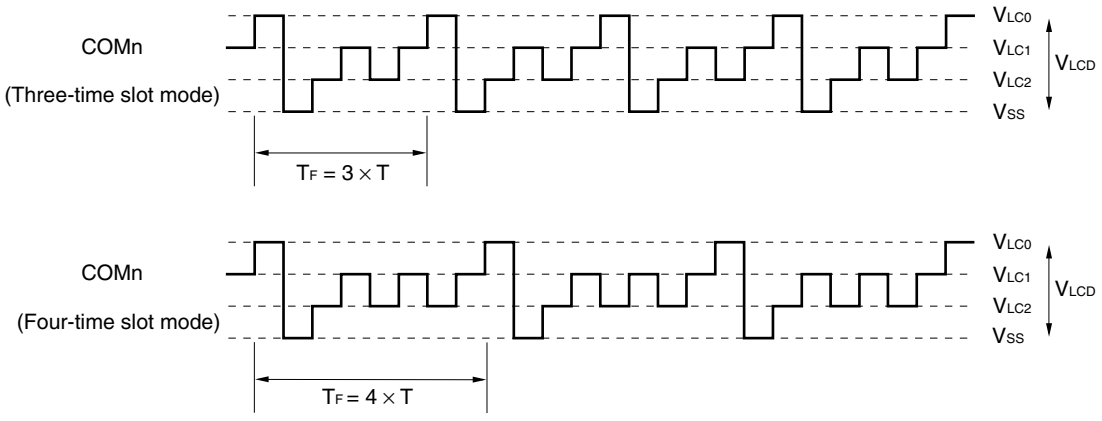
T: One LCD clock period T_F: Frame frequency

(b) 1/2 bias method



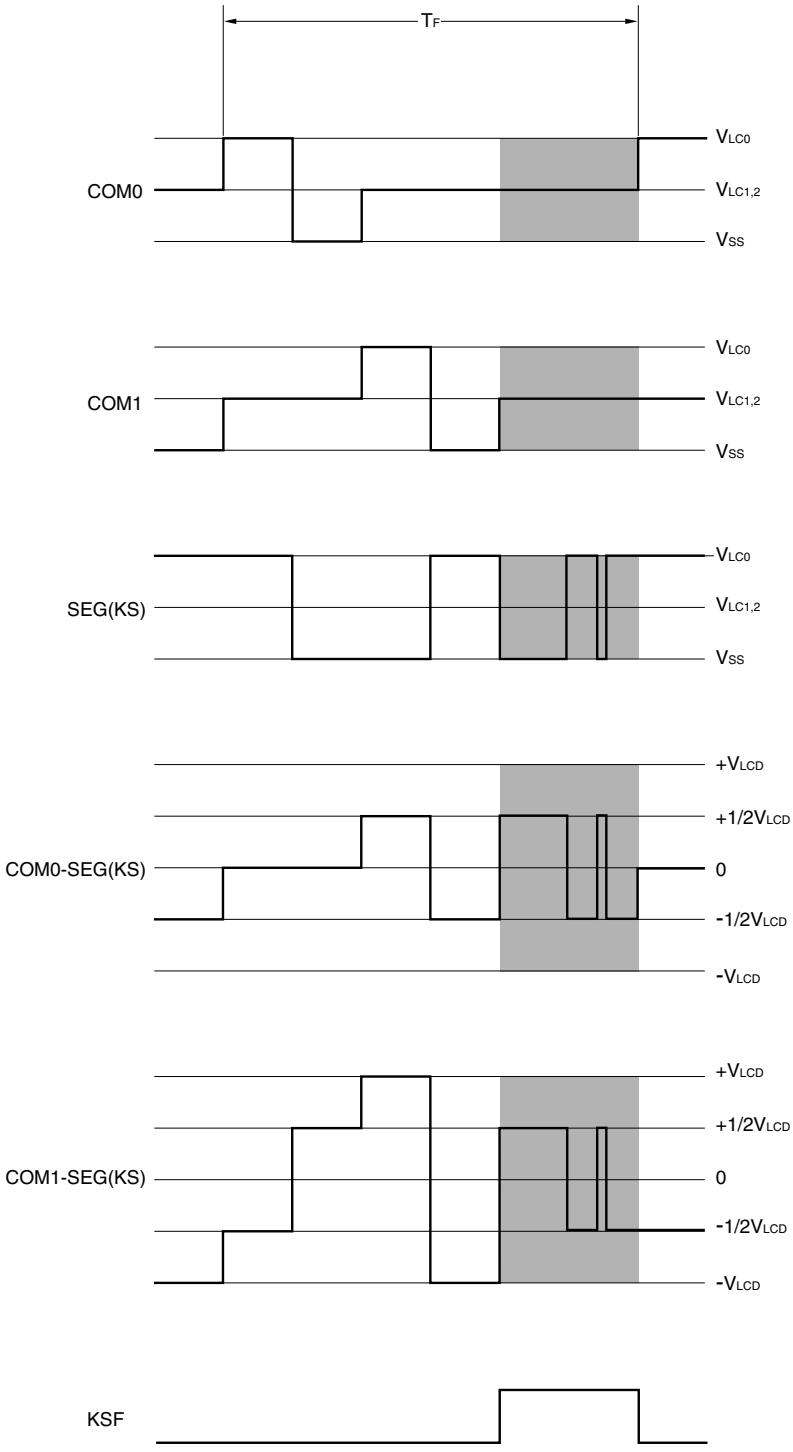
T: One LCD clock period T_F: Frame frequency

(c) 1/3 bias method



T: One LCD clock period T_F: Frame frequency

<Key identification>



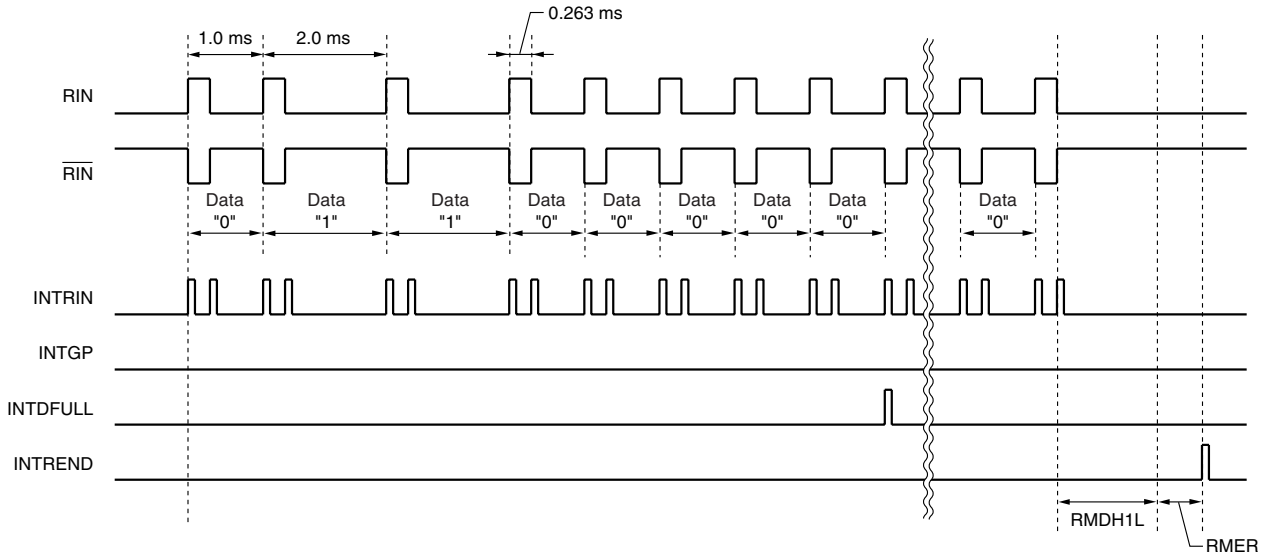
Shaded sections: Segment key scan output period

Remark During key identification, the residual charge of the LCD panel can be eliminated by outputting a signal with an inverted relationship between its first half and latter half.

19.4.5 Format of type C reception mode

Figure 19-10 shows the data format for type C.

Figure 19-10. Example of Type C Data Format



Remark $\overline{\text{RIN}}$ is the internally inverted signal of RIN.

19.4.6 Operation flow of type C reception mode

Figure 19-11 shows the operation flow.

Cautions 1. When INTRERR is generated, RMSR and RMSCR are automatically cleared immediately.

2. When data has been set to all the bits of RMSR, the following processing is automatically performed.

- **The value of RMSR is transferred to RMDR.**
- **INTDFULL is generated.**
- **RMSR is cleared.**

RMDR must then be read before the next data is set to all the bits of RMSR.

3. When INTREND has been generated, read RMSCR first followed by RMSR.
When RMSR has been read, RMSCR and RMSR are automatically cleared.
If INTREND is generated, the next data cannot be received until RMSR is read.

4. RMSR, RMSCR, and RMDR are cleared simultaneously to operation termination (RMEN = 0).

5. In type C reception mode, if the conditions for receiving a data low-/high-level width are not met before the first INTDFULL interrupt is generated, INTRERR and INTREND will not be generated. However, RMSR and RMSCR will be cleared.

CHAPTER 21 KEY INTERRUPT FUNCTION

21.1 Functions of Key Interrupt

A key interrupt (INTKR) can be generated by setting the key return mode register (KRM) and inputting a falling edge to the key interrupt input pins (KR0 to KR4).

Table 21-1. Assignment of Key Interrupt Detection Pins

Flag	Description
KRM0	Controls KR0 signal in 1-bit units.
KRM1	Controls KR1 signal in 1-bit units.
KRM2	Controls KR2 signal in 1-bit units.
KRM3	Controls KR3 signal in 1-bit units.
KRM4	Controls KR4 signal in 1-bit units.

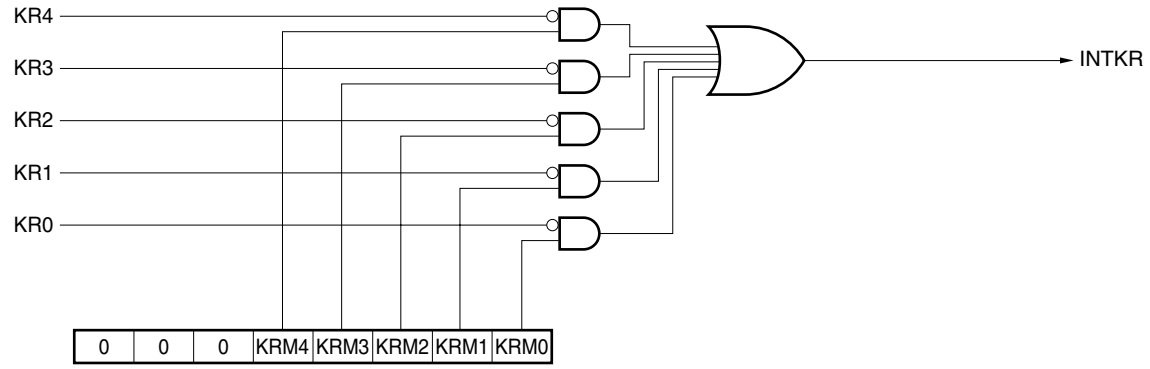
21.2 Configuration of Key Interrupt

The key interrupt includes the following hardware.

Table 21-2. Configuration of Key Interrupt

Item	Configuration
Control register	Key return mode register (KRM)

Figure 21-1. Block Diagram of Key Interrupt



25.5 Cautions for Low-Voltage Detector

In a system where the supply voltage (V_{DD}) fluctuates for a certain period in the vicinity of the LVI detection voltage (V_{LVI}), the operation is as follows depending on how the low-voltage detector is used.

(1) When used as reset

The system may be repeatedly reset and released from the reset status.

In this case, the time from release of reset to the start of the operation of the microcontroller can be arbitrarily set by taking action (1) below.

(2) When used as interrupt

Interrupt requests may be frequently generated. Take (b) of action (2) below.

<Action>

(1) When used as reset

After releasing the reset signal, wait for the supply voltage fluctuation period of each system by means of a software counter that uses a timer, and then initialize the ports (see **Figure 25-9**).

(2) When used as interrupt

(a) Confirm that "supply voltage (V_{DD}) ≥ detection voltage (V_{LVI})" when detecting the falling edge of V_{DD}, or "supply voltage (V_{DD}) < detection voltage (V_{LVI})" when detecting the rising edge of V_{DD}, in the servicing routine of the LVI interrupt by using bit 0 (LVIF) of the low-voltage detection register (LVIM). Clear bit 0 (LVIIF) of interrupt request flag register 0L (IF0L) to 0.

(b) In a system where the supply voltage fluctuation period is long in the vicinity of the LVI detection voltage, wait for the supply voltage fluctuation period, confirm that "supply voltage (V_{DD}) ≥ detection voltage (V_{LVI})" when detecting the falling edge of V_{DD}, or "supply voltage (V_{DD}) < detection voltage (V_{LVI})" when detecting the rising edge of V_{DD}, using the LVIF flag, and clear the LVIIF flag to 0.

Remark If bit 2 (LVISEL) of the low voltage detection register (LVIM) is set to "1", the meanings of the above words change as follows.

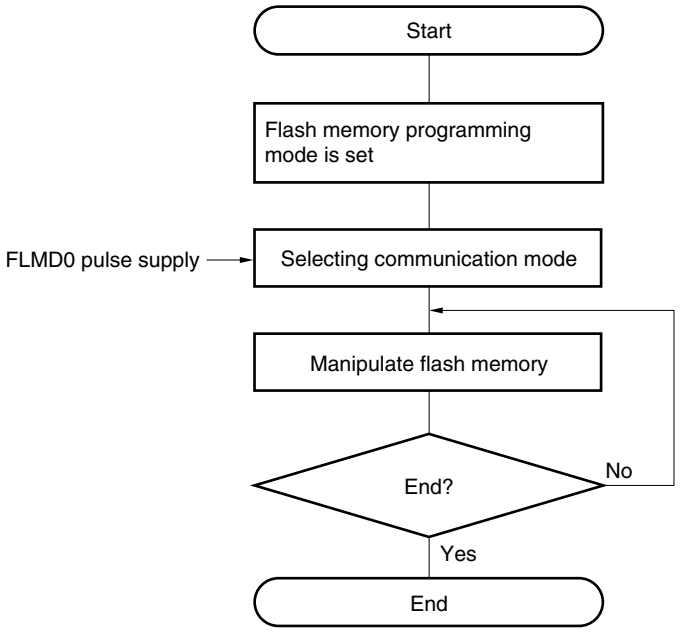
- Supply voltage (V_{DD}) → Input voltage from external input pin (EXLVI)
- Detection voltage (V_{LVI}) → Detection voltage (V_{EXLVI} = 1.21 V)

27.7 Programming Method

27.7.1 Controlling flash memory

The following figure illustrates the procedure to manipulate the flash memory.

<R> **Figure 27-12. Flash Memory Manipulation Procedure**



27.7.2 Flash memory programming mode

To rewrite the contents of the flash memory by using the dedicated flash memory programmer, set the 78K0/LE3 in the flash memory programming mode. To set the mode, set the FLMD0 pin to V_{DD} and clear the reset signal.

Change the mode by using a jumper when writing the flash memory on-board.

Figure 27-13. Flash Memory Programming Mode

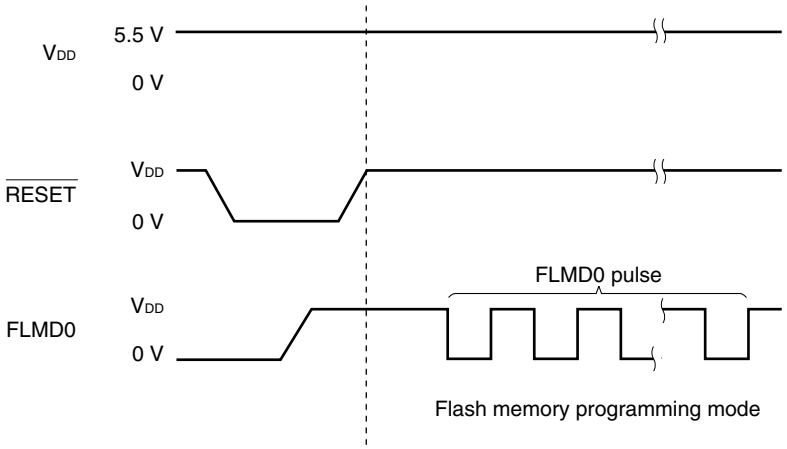


Table 27-6. Relationship Between FLMD0 Pin and Operation Mode After Reset Release

FLMD0	Operation Mode
0	Normal operation mode
V_{DD}	Flash memory programming mode

DC Characteristics (4/5)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply current	I_{DD1} Note 1	Operating mode	f_{XH} = 10 MHz Note 2, V_{DD} = 5.0 V	Square wave input		1.6	3.0	mA
				Resonator connection		2.3	3.4	
			f_{XH} = 10 MHz Note 2, V_{DD} = 3.0 V	Square wave input		1.5	2.9	mA
				Resonator connection		2.2	3.3	
			f_{XH} = 5 MHz Note 2, V_{DD} = 3.0 V	Square wave input		0.9	1.7	mA
				Resonator connection		1.3	2.0	
			f_{XH} = 5 MHz Note 2, V_{DD} = 2.0 V	Square wave input		0.7	1.4	mA
				Resonator connection		1.0	1.6	
			f_{RH} = 8 MHz, V_{DD} = 5.0 V Note 3			1.4	2.3	mA
			f_{SUB} = 32.768 kHz Note 4, V_{DD} = 5.0 V	Resonator connection		6.7	26	μA
	I_{DD2} Note 1	HALT mode	f_{XH} = 10 MHz Note 2, V_{DD} = 5.0 V	Square wave input		0.4	1.4	mA
				Resonator connection		1.0	1.7	
			f_{XH} = 5 MHz Note 2, V_{DD} = 3.0 V	Square wave input		0.2	0.7	mA
				Resonator connection		0.5	1.0	
			f_{RH} = 8 MHz, V_{DD} = 5.0 V Note 3			0.4	1.2	mA
			f_{SUB} = 32.768 kHz Note 5, V_{DD} = 5.0 V	Resonator connection		2.4	22	μA
	I_{DD3} Note 6	STOP mode	V_{DD} = 5.0 V			1	20	μA
			V_{DD} = 5.0 V, T_A = –40 to +70°C			1	10	μA

<R> **Notes 1.** Total current flowing into the internal power supply (V_{DD}), including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The MAX. values include the peripheral operation current. However, the current flowing into the pull-up resistors and the output current of the port are not included.

2. Not including the operating current of the 8 MHz internal oscillator, 240 kHz internal oscillator and XT1 oscillation, and the current flowing into the A/D converter, watchdog timer, LVI circuit and LCD controller/driver.

3. Not including the operating current of the X1 oscillation, XT1 oscillation and 240 kHz internal oscillator, and the current flowing into the A/D converter, watchdog timer, LVI circuit and LCD controller/driver.

4. Not including the operating current of the X1 oscillation, 8 MHz internal oscillator and 240 kHz internal oscillator, and the current flowing into the A/D converter, watchdog timer, LVI circuit and LCD controller/driver.

<R> **5.** Not including the operating current of the X1 oscillation, 8 MHz internal oscillator and 240 kHz internal oscillator, and the current flowing into the A/D converter, watchdog timer, LVI circuit, LCD controller/driver and real-time counter.

<R> **6.** Total current flowing into the internal power supply (V_{DD}), including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. However, the current flowing into the pull-up resistors and the output current of the port, the operating current of the 240 kHz internal oscillator and XT1 oscillation, and the current flowing into the A/D converter, watchdog timer, LVI circuit, LCD controller/driver and real-time counter are not included.

Remarks 1. f_{XH}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{RH}: Internal high-speed oscillation clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

A.5 Debugging Tools (Hardware)

A.5.1 When using in-circuit emulator QB-78K0LX3

QB-78K0/Lx3 In-circuit emulator	This in-circuit emulator serves to debug hardware and software when developing application systems using the 78K0/Lx3. It supports to the integrated debugger (ID78K0-QB). This emulator should be used in combination with a power supply unit and emulation probe, and the USB is used to connect this emulator to the host machine.
QB-144-CA-01 Check pin adapter	This check pin adapter is used in waveform monitoring using the oscilloscope, etc.
QB-80-EP-01T Emulation probe	This emulation probe is flexible type and used to connect the in-circuit emulator and target system.
QB-64GB-EA-09T, QB-64GK-EA-07T Exchange adapter	This exchange adapter is used to perform pin conversion from the in-circuit emulator to target connector. • QB-64GB-EA-09T: For 64-pin plastic LQFP (GB-GAH type) • QB-64GK-EA-07T: For 64-pin plastic LQFP (GK-GAJ type)
QB-64GB-YS-01T, QB-64GK-YS-01T Space adapter	This space adapter is used to adjust the height between the target system and in-circuit emulator. • QB-64GB-YS-01T: For 64-pin plastic LQFP (GB-GAH type) • QB-64GK-YS-01T: For 64-pin plastic LQFP (GK-GAJ type)
QB-64GB-YQ-01T, QB-64GK-YQ-01T YQ connector	This YQ connector is used to connect the target connector and exchange adapter. • QB-64GB-YQ-01T: For 64-pin plastic LQFP (GB-GAH type) • QB-64GK-YQ-01T: For 64-pin plastic LQFP (GK-GAJ type)
QB-64GB-HQ-01T, QB-64GK-HQ-01T Mount adapter	This mount adapter is used to mount the target device with socket. • QB-64GB-HQ-01T: For 64-pin plastic LQFP (GB-GAH type) • QB-64GK-HQ-01T: For 64-pin plastic LQFP (GK-GAJ type)
QB-64GB-NQ-01T, QB-64GK-NQ-01T Target connector	This target connector is used to mount on the target system. • QB-64GB-NQ-01T: For 64-pin plastic LQFP (GB-GAH type) • QB-64GK-NQ-01T: For 64-pin plastic LQFP (GK-GAJ type)

Remarks 1. The QB-78K0LX3 is supplied with the integrated debugger ID78K0-QB, a USB interface cable, a power supply unit, the on-chip debug emulator QB-MINI2, connection cables (10-pin and 16-pin cables), and the 78K0-OCD board.

Download the software for operating the QB-MINI2 from the download site for development tools (http://www.necel.com/micro/ods/eng/index.html) when using the QB-MINI2.

2. The packed contents differ depending on the part number, as follows.

Packed Contents / Part Number	In-Circuit Emulator	Emulation Probe	Exchange Adapter	YQ Connector	Target Connector
QB-78K0LX3 -ZZZ	QB-78K0LX3	None			
QB-78K0LX3-T64GB		QB-80-EP-01T	QB-64GB-EA-09T	QB-64GB-YQ-01T	QB-64GB-NQ-01T
QB-78K0LX3-T64GK			QB-64GK-EA-07T	QB-64GK-YQ-01T	QB-64GK-NQ-01T