Renesas Electronics America Inc - UPD78F0454GK-GAJ-AX Datasheet

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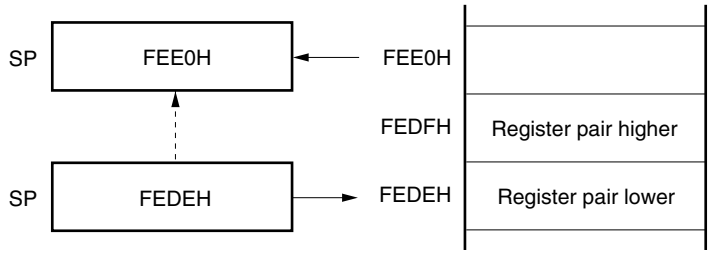
Applications of "Embedded - Microcontrollers"

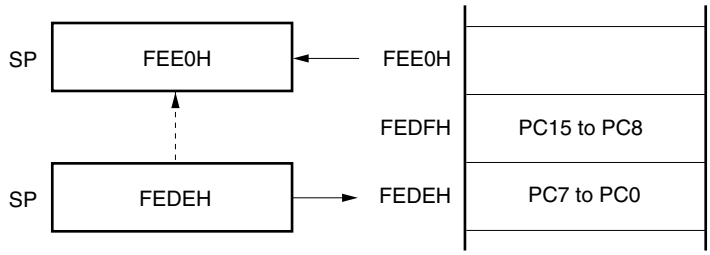
Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	3-Wire SIO, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	46
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0454gk-gaj-ax

Figure 3-25. Data to Be Restored from Stack Memory

(a) POP rp instruction (when SP = FEDEH)



(b) RET instruction (when SP = FEDEH)



(c) RETI, RETB instructions (when SP = FEDDH)

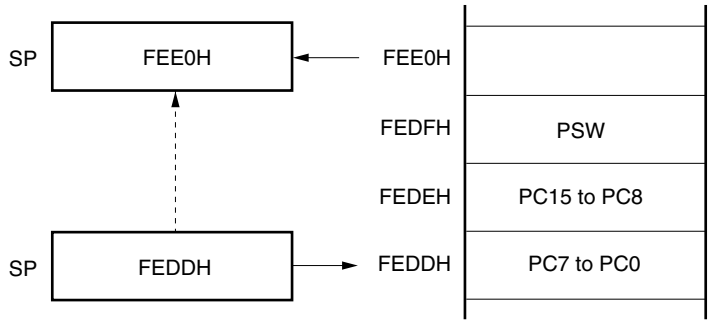
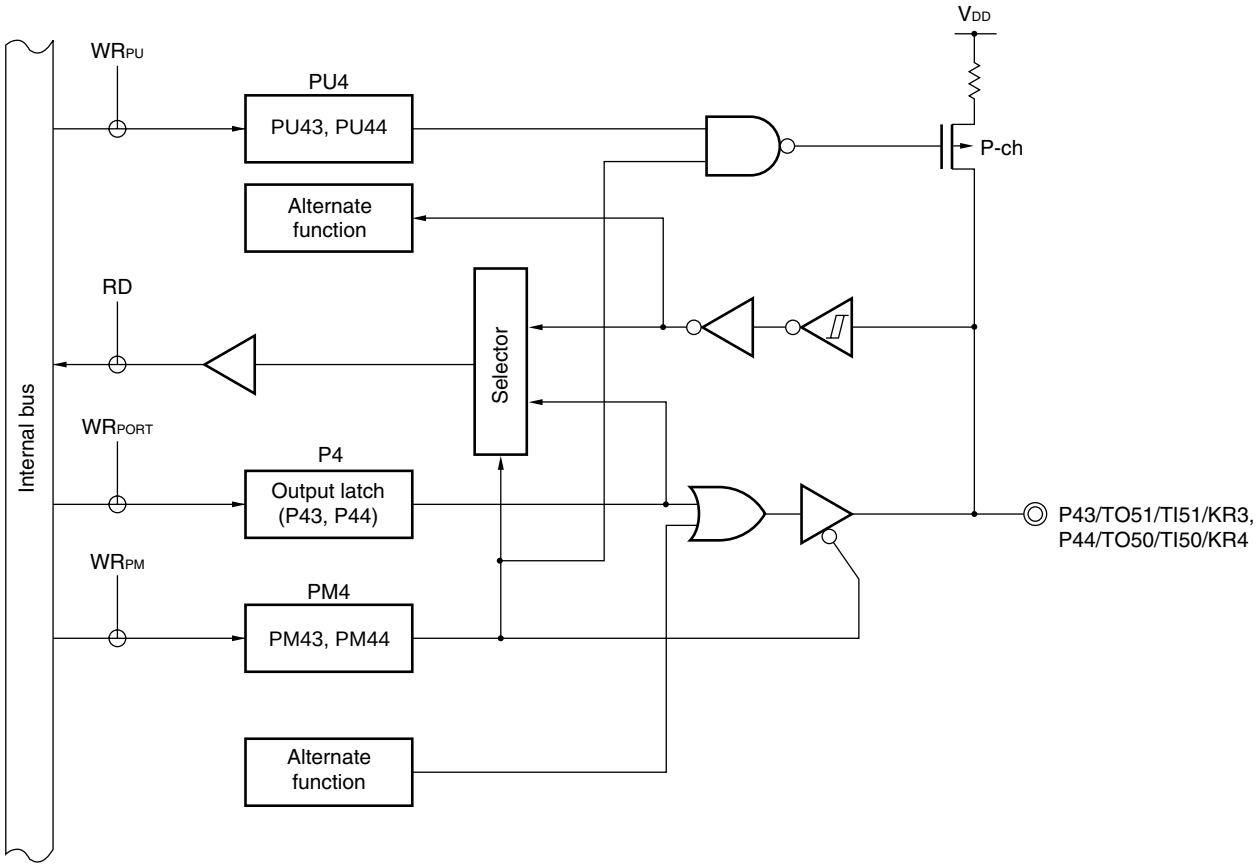


Table 3-8. Special Function Register List (1/5)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulatable Bit Unit			After Reset
				1 Bit	8 Bits	16 Bits	
FF00H	Receive buffer register 6	RXB6	R	–	√	–	FFH
FF01H	Port register 1	P1	R/W	√	√	–	00H
FF02H	Port register 2	P2	R/W	√	√	–	00H
FF03H	Port register 3	P3	R/W	√	√	–	00H
FF04H	Port register 4	P4	R/W	√	√	–	00H
FF05H	Transmit buffer register 6	TXB6	R/W	–	√	–	FFH
FF06H	10-bit A/D conversion result register[Note]	ADCR	R	–	–	√	0000H
FF07H	8-bit A/D conversion result register H[Note]	ADCRH	R	–	√	–	00H
FF08H	Port register 8	P8	R/W	√	√	–	00H
FF0AH	Port register 10	P10	R/W	√	√	–	00H
FF0BH	Port register 11	P11	R/W	√	√	–	00H
FF0CH	Port register 12	P12	R/W	√	√	–	00H
FF0EH	Port register 14	P14	R/W	√	√	–	00H
FF0FH	Port register 15	P15	R/W	√	√	–	00H
FF10H	16-bit timer counter 00	TM00	R	–	–	√	0000H
FF11H							
FF12H	16-bit timer capture/compare register 000	CR000	R/W	–	–	√	0000H
FF13H							
FF14H	16-bit timer capture/compare register 010	CR010	R/W	–	–	√	0000H
FF15H							
FF16H	8-bit timer counter 50	TM50	R	–	√	–	00H
FF17H	8-bit timer compare register 50	CR50	R/W	–	√	–	00H
FF18H	8-bit timer H compare register 00	CMP00	R/W	–	√	–	00H
FF19H	8-bit timer H compare register 10	CMP10	R/W	–	√	–	00H
FF1AH	8-bit timer H compare register 01	CMP01	R/W	–	√	–	00H
FF1BH	8-bit timer H compare register 11	CMP11	R/W	–	√	–	00H
FF1FH	Serial I/O shift register 10	SIO10	R	–	√	–	00H
FF20H	Port function register 1	PF1	R/W	√	√	–	00H
FF21H	Port mode register 1	PM1	R/W	√	√	–	FFH
FF22H	Port mode register 2	PM2	R/W	√	√	–	FFH
FF23H	Port mode register 3	PM3	R/W	√	√	–	FFH
FF24H	Port mode register 4	PM4	R/W	√	√	–	FFH
FF28H	Port mode register 8	PM8	R/W	√	√	–	FFH
FF2AH	Port mode register 10	PM10	R/W	√	√	–	FFH
FF2BH	Port mode register 11	PM11	R/W	√	√	–	FFH
FF2CH	Port mode register 12	PM12	R/W	√	√	–	FFH
FF2EH	Port mode register 14	PM14	R/W	√	√	–	FFH
FF2FH	Port mode register 15	PM15	R/W	√	√	–	FFH
FF30H	Internal high-speed oscillation trimming register	HIOTRM	R/W	–	√	–	10H
FF31H	Pull-up resistor option register 1	PU1	R/W	√	√	–	00H
FF33H	Pull-up resistor option register 3	PU3	R/W	√	√	–	00H

Note μPD78F045x and 78F046x only.

Figure 4-10. Block Diagram of P43 and P44



P4: Port register 4
PU4: Pull-up resistor option register 4
PM4: Port mode register 4
RD: Read signal
WR××: Write signal

4.2.10 Port 15

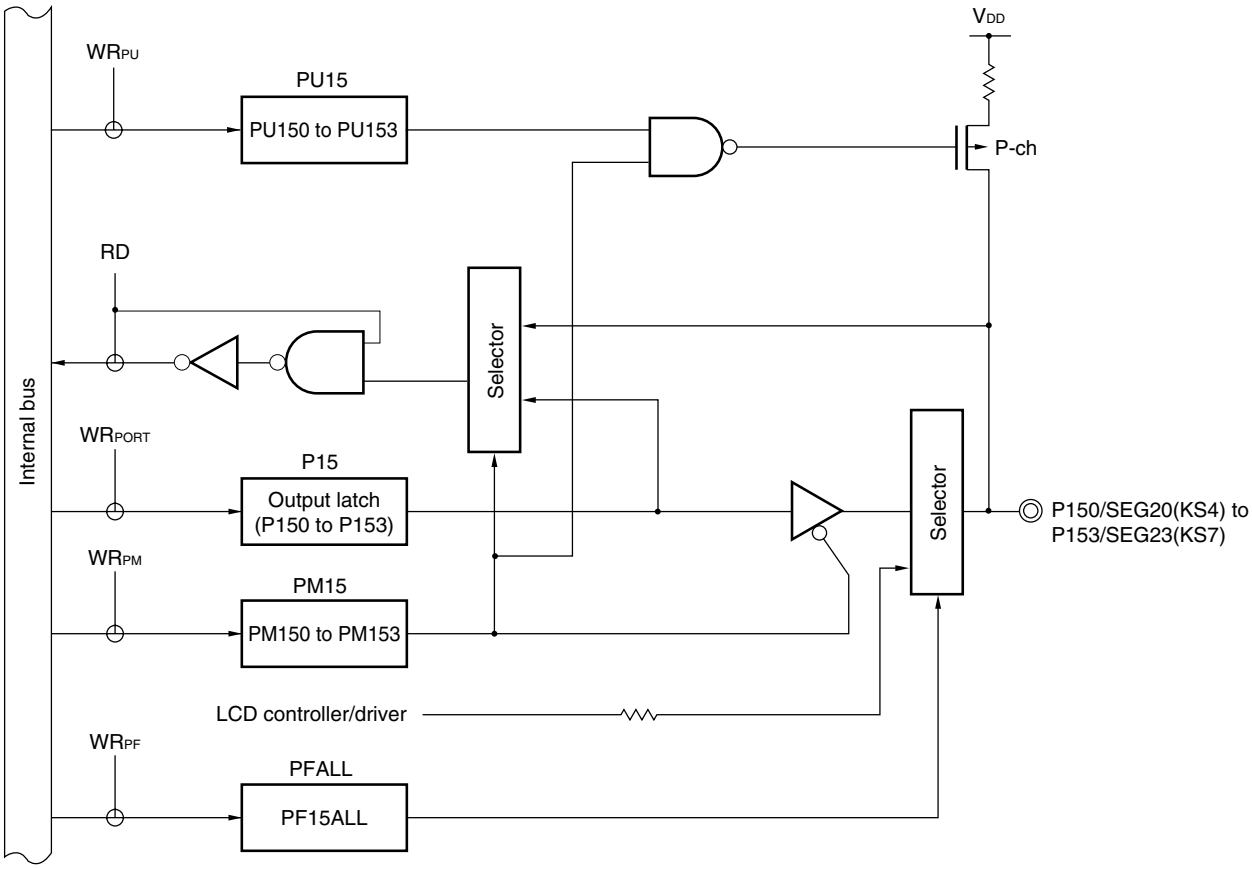
Port 15 is a 4-bit I/O port with an output latch. Port 15 can be set to the input mode or output mode in 1-bit units using port mode register 15 (PM15). When the P150 to P153 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 15 (PU15).

This port can also be used for segment output.

Reset signal generation sets port 15 to input mode.

Figure 4-20 shows a block diagram of port 15.

Figure 4-20. Block Diagram of P150 and P153



P15: Port register 15
PU15: Pull-up resistor option register 15
PM15: Port mode register 15
PFALL: Port function register ALL
RD: Read signal
WR××: Write signal

(3) Pull-up resistor option registers (PU1, PU3, PU4, PU8, PU10 to PU12, PU14, PU15)

These registers specify whether the on-chip pull-up resistors of P11 to P14, P31 to P34, P40 to P44, P80 to P83, P100 to P103, P110 to P113, P120, P140 to P143, or P150 to P153 are to be used or not. On-chip pull-up resistors can be used in 1-bit units only for the bits set to input mode of the pins to which the use of an on-chip pull-up resistor has been specified in PU1, PU3, PU4, PU8, PU10 to PU12, PU14, and PU15. On-chip pull-up resistors cannot be connected to bits set to output mode and bits used as alternate-function output pins, regardless of the settings of PU1, PU3, PU4, PU8, PU10 to PU12, PU14, and PU15.

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

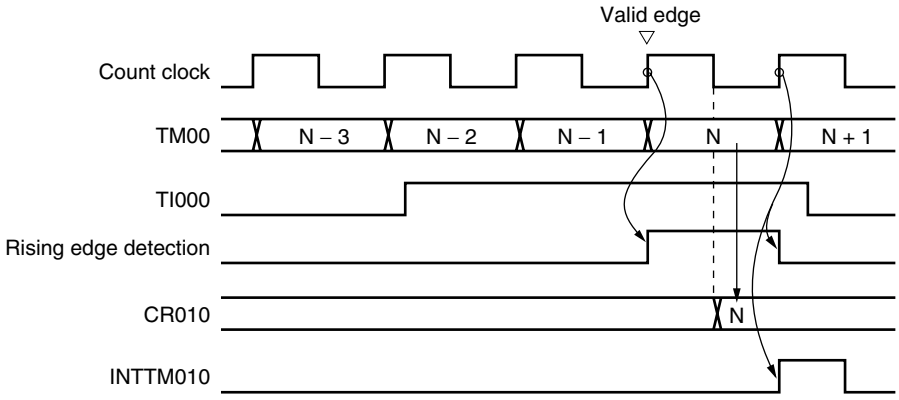
Figure 4-23. Format of Pull-up Resistor Option Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PU1	0	0	0	PU14	PU13	PU12	PU11	0	FF31H	00H	R/W
PU3	0	0	0	PU34	PU33	PU32	PU31	0	FF33H	00H	R/W
PU4	0	0	0	PU44Note	PU43Note	PU42Note	PU41Note	PU40Note	FF34H	00H	R/W
PU8	0	0	0	0	PU83	PU82	PU81	PU80	FF38H	00H	R/W
PU10	0	0	0	0	PU103	PU102	PU101	PU100	FF3AH	00H	R/W
PU11	0	0	0	0	PU113	PU112	PU111	PU110	FF3BH	00H	R/W
PU12	0	0	0	0	0	0	0	PU120	FF3CH	00H	R/W
PU14	0	0	0	0	PU143	PU142	PU141	PU140	FF3EH	00H	R/W
PU15	0	0	0	0	PU153	PU152	PU151	PU150	FF3FH	00H	R/W

PUmn	Pmn pin on-chip pull-up resistor selection (m = 1, 3, 4, 8, 10 to 12, 14, 15; n = 0 to 4)
0	On-chip pull-up resistor not connected
1	On-chip pull-up resistor connected

<R> **Note** For setting when using the segment key scan function, see **17.3 Registers Controlling LCD Controller/Driver**.

Figure 6-7. Example of CR010 Capture Operation (When Rising Edge Is Specified)



(3) 16-bit timer output control register 00 (TOC00)

TOC00 is an 8-bit register that controls TO00 output.

TOC00 can be rewritten while only OSPT00 is operating (when TMC003 and TMC002 = other than 00). Rewriting the other bits is prohibited during operation.

However, TOC004 can be rewritten during timer operation as a means to rewrite CR010 (see **6.5.1 Rewriting CR010 during TM00 operation**).

TOC00 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears TOC00 to 00H.

Caution Be sure to set TOC00 using the following procedure.

<1> Set TOC004 and TOC001 to 1.

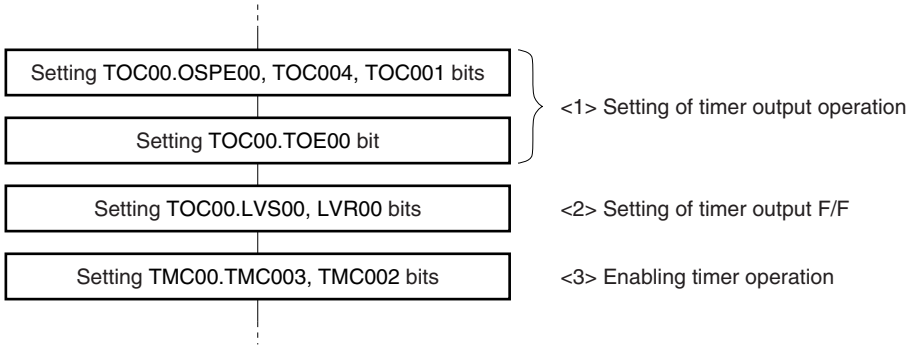
<2> Set only TOE00 to 1.

<3> Set either of LVS00 or LVR00 to 1.

(2) Setting LVS00 and LVR00

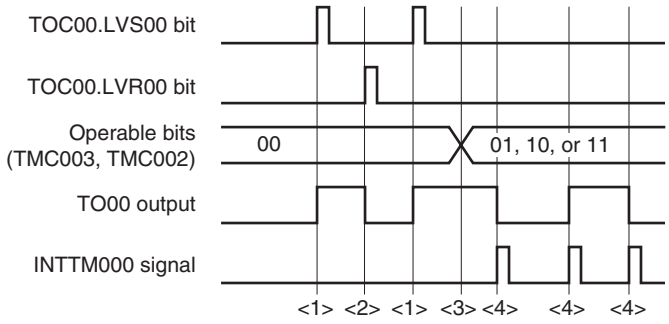
Set LVS00 and LVR00 using the following procedure.

Figure 6-57. Example of Flow for Setting LVS00 and LVR00 Bits



Caution Be sure to set LVS00 and LVR00 following steps <1>, <2>, and <3> above. Step <2> can be performed after <1> and before <3>.

Figure 6-58. Timing Example of LVR00 and LVS00



<1> The TO00 output goes high when LVS00 and LVR00 = 10.

<2> The TO00 output goes low when LVS00 and LVR00 = 01 (the pin output remains unchanged from the high level even if LVS00 and LVR00 are cleared to 00).

<3> The timer starts operating when TMC003 and TMC002 are set to 01, 10, or 11. Because LVS00 and LVR00 were set to 10 before the operation was started, the TO00 output starts from the high level. After the timer starts operating, setting LVS00 and LVR00 is prohibited until TMC003 and TMC002 = 00 (disabling the timer operation).

<4> The TO00 output level is inverted each time an interrupt signal (INTTM000) is generated.

CHAPTER 8 8-BIT TIMERS H0, H1, AND H2

8.1 Functions of 8-Bit Timers H0, H1, and H2

8-bit timers H0, H1, and H2 have the following functions.

- Interval timer
- Square-wave output[Note 1]
- PWM output[Note 2]
- Carrier generator (8-bit timer H1 only)[Note 3]

Notes 1. TMH0 and TMH1 only.

2. However, TOH0 and TOH1 only for TOHn

3. TMH1 only. TM51 and TMH1 can be used in combination as a carrier generator mode.

8.2 Configuration of 8-Bit Timers H0, H1, and H2

8-bit timers H0, H1, and H2 include the following hardware.

Table 8-1. Configuration of 8-Bit Timers H0, H1, and H2

Item	Configuration
Timer register	8-bit timer counter Hn
Registers	8-bit timer H compare register 0n (CMP0n) 8-bit timer H compare register 1n (CMP1n)
Timer output	TOHn[Note 1], output controller
Control registers	8-bit timer H mode register n (TMHMDn) 8-bit timer H carrier control register 1 (TMCYC1)[Note 2] Port mode register 3 (PM3) Port register 3 (P3)

Notes 1. TMH2 does not have an output pin (TOH2). It can only be used as an internal interrupt (INTTMH2) or an external event input enable signal for the TI52 pin.

2. 8-bit timer H1 only

Remark n = 0-2, however, TOH0 and TOH1 only for TOHn

Figures 8-1 and 8-3 show the block diagrams.

(2) Port mode register 3 (PM3)

This register sets port 3 input/output in 1-bit units.

When using the P33/TI000/RTCDIV/RTCCL/BUZ/INTP2 pin for buzzer output, clear PM33 and the output latches of P33 to 0.

PM3 is set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets PM3 to FFH.

Figure 11-3. Format of Port Mode Register 3 (PM3)

Address: FF23H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM3	1	1	1	PM34	PM33	PM32	PM31	1

PM3n	P3n pin I/O mode selection (n = 1 to 4)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

11.4 Operations of Buzzer Output Controller

The buzzer frequency is output as the following procedure.

<1> Select the buzzer output frequency with bits 5 and 6 (BCS0, BCS1) of the clock output selection register (CKS) (buzzer output in disabled status).

<2> Set bit 7 (BZOE) of CKS to 1 to enable buzzer output.

13.5 16-Bit ΔΣ Type A/D Converter Operations

13.5.1 Basic operations of 16-bit ΔΣ type A/D converter

<1> Set ADD0TEN[Note 1] = 1 (enable the delay time setting).[Note 2]
<2> Use ADD0DLY2 to ADD0DLY0[Note 1] to set the delay time.[Note 2]
<3> Set the ΔΣ A/D conversion target channel.
<4> Set ADDPON to 1 (ΔΣ A/D power-on).
<5> Set the conversion operation modes, such as the input mode, operation mode and sampling counts via the ADDCTL1 and ADDCTL0 registers.
<6> Conversion operation starts when ADDCE is set to 1, at least 1.2 μs after ADDPON has been set to 1. (Conversion operation also starts when ADDCE is set to 1 before 1.2 μs elapse after ADDPON has been set to 1, but the conversion result is not guaranteed in this case).[Note 3]
<7> When conversion is completed, an interrupt (INTDSAD) is generated and the result is stored in the ADDCR register. Read the ADDCR register value.
<8> If ADDCE is not to be set to 0 (conversion operation stop), repeat step 5. If conversion operation is to be stopped, set ADDCE to 0.
<9> When the current is to be reduced without using ΔΣ A/D, set ADDPON to 0 (ΔΣ A/D power-off).

Notes 1. Directly specify the addresses and write to ADD0TEN and ADD0DLY2 to ADD0DLY0 by using an 8-bit memory manipulation instruction.
2. Setting of the delay time is not required if the conversion accuracy is sufficient.
3. Writing to ADDCTL1 during conversion operation is prohibited.
When the pin settings subject to ΔΣ A/D conversion are altered during conversion operation, conversion results are not stored. When the target pin settings are altered, restart conversion operation.

13.5.2 Operation mode of 16-bit ΔΣ type A/D converter

Several operation modes can be set for the 16-bit ΔΣ type A/D converter.

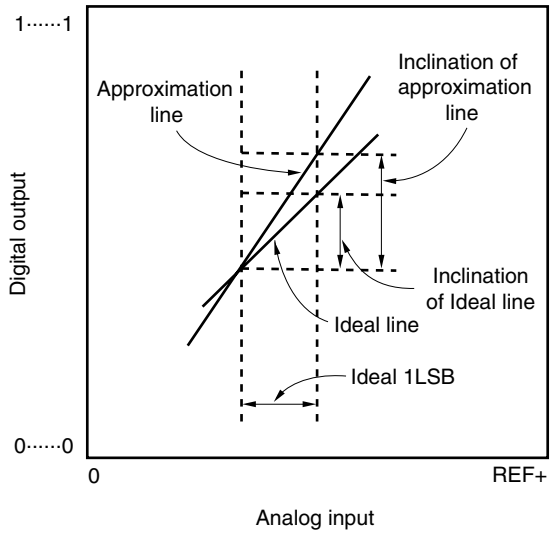
(1) Differential input mode/single input mode
Differential input mode or single input mode can be selected as the input mode for the 16-bit ΔΣ type A/D converter. The accuracy is higher in differential input mode than in single input mode. When using the differential input mode, input analog signals to DSn- and DSn+. When using the single input mode, input analog signals to DSn+ and set DSn- to the same potential as V_{SS} and AV_{SS}. Make sure that the central values of the DSn- and DSn+ input voltages are 0.5 REF+ in differential input mode.

(2) 16-bit ΔΣ type A/D high-accuracy mode
High-accuracy mode ON or OFF can be selected as the conversion accuracy mode for the 16-bit ΔΣ type A/D converter. The accuracy is higher when set to high-accuracy mode ON than when set to high-accuracy mode OFF.

(5) Gain error

The gain error is the ratio of the ideal inclination to the inclination of the approximation line.

Figure 13-18. Gain Error



$$\text{Gain error} = \frac{\text{Inclination of approximation line} - 1}{\text{Inclination of Ideal line}} \times 100\ [\%]$$

(6) Integral linearity error

This shows the degree to which the conversion characteristics deviate from the approximation line. It expresses the maximum value of the difference between the actual measurement value and the ideal straight line when the offset and gain error are 0.

Figure 13-19. Integral linearity error

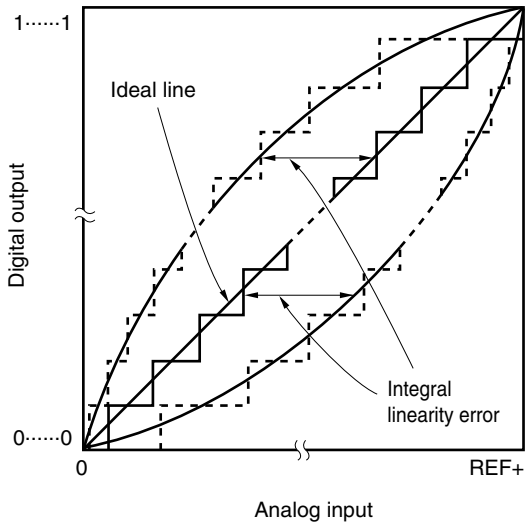
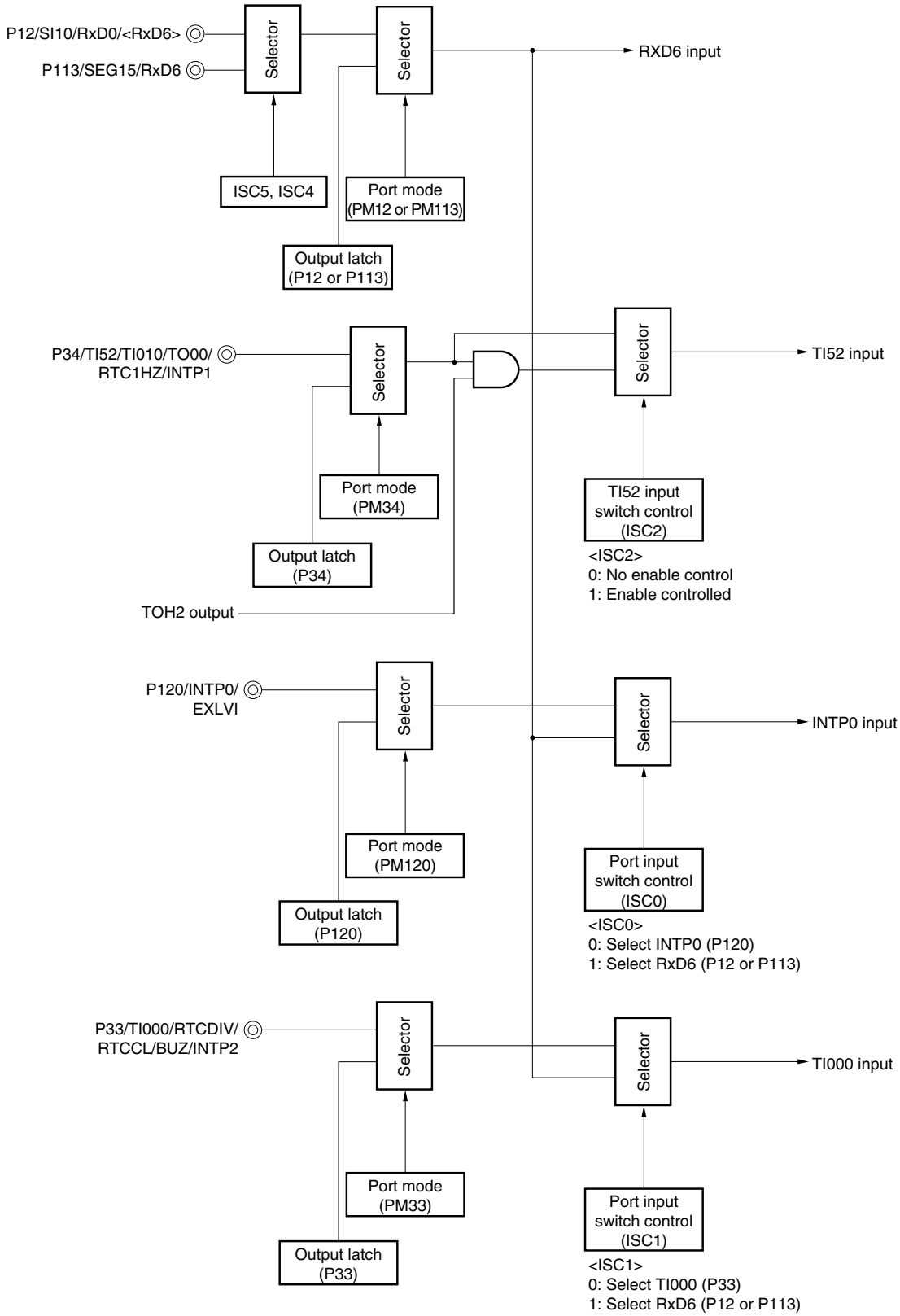
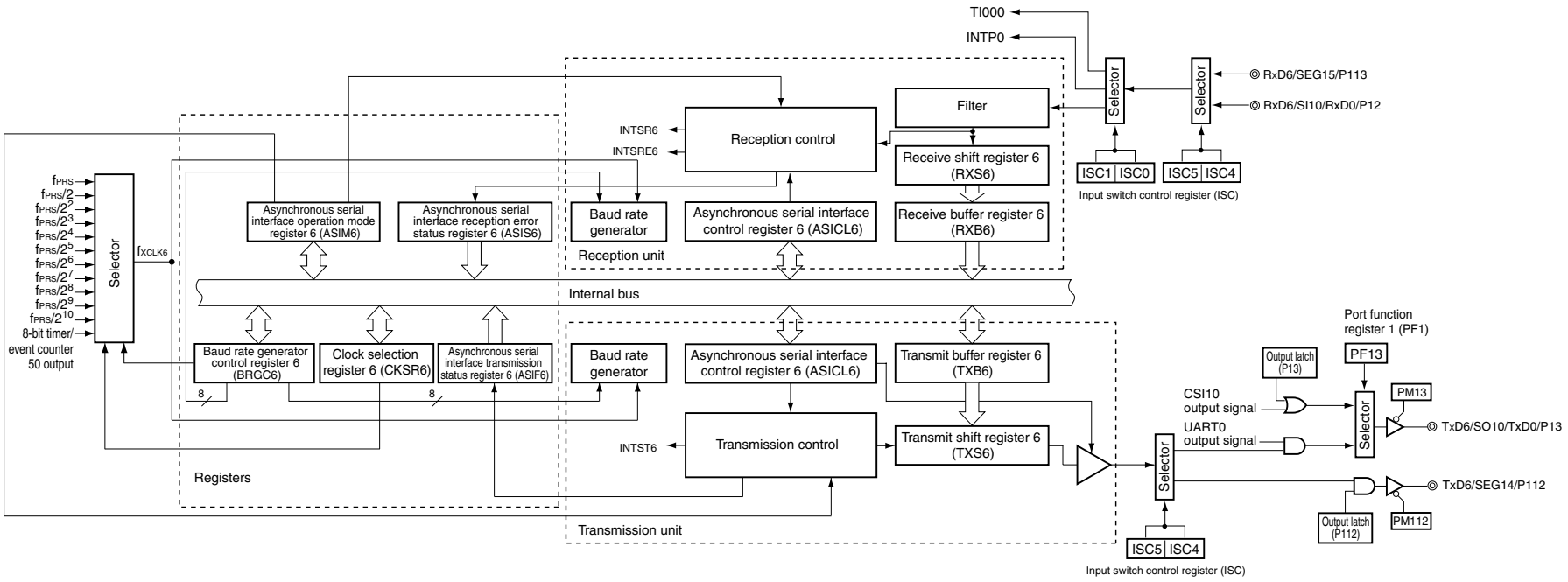


Figure 15-3. Port Configuration for LIN Reception Operation



Remark ISC0, ISC1, ISC2, ISC4, ISC5: Bits 0, 1, 2, 4 and 5 of the input switch control register (ISC) (see **Figure 15-11**)

Figure 15-4. Block Diagram of Serial Interface UART6



(c) Normal transmission

When bit 7 (POWER6) of asynchronous serial interface operation mode register 6 (ASIM6) is set to 1 and bit 6 (TXE6) of ASIM6 is then set to 1, transmission is enabled. Transmission can be started by writing transmit data to transmit buffer register 6 (TXB6). The start bit, parity bit, and stop bit are automatically appended to the data.

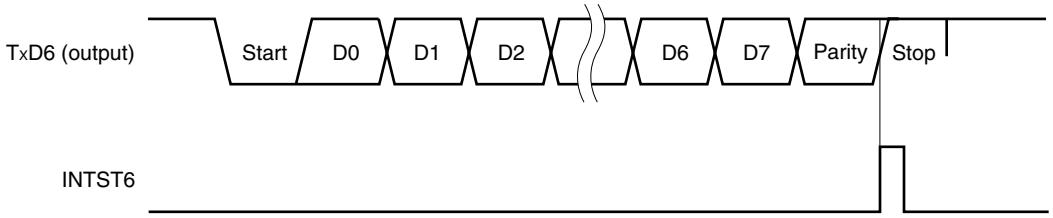
When transmission is started, the data in TXB6 is transferred to transmit shift register 6 (TXS6). After that, the transmit data is sequentially output from TXS6 to the TxD6 pin. When transmission is completed, the parity and stop bits set by ASIM6 are appended and a transmission completion interrupt request (INTST6) is generated.

Transmission is stopped until the data to be transmitted next is written to TXB6.

Figure 15-17 shows the timing of the transmission completion interrupt request (INTST6). This interrupt occurs as soon as the last stop bit has been output.

Figure 15-17. Normal Transmission Completion Interrupt Request Timing

1. Stop bit length: 1



2. Stop bit length: 2

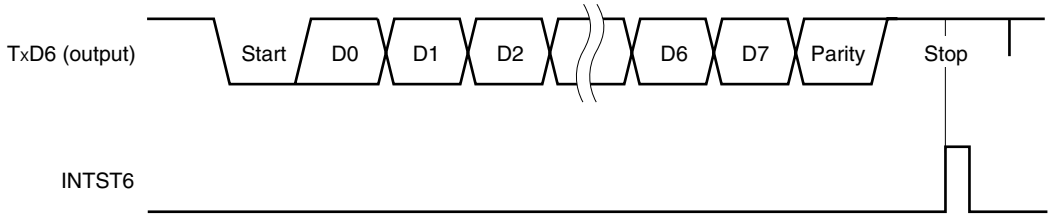
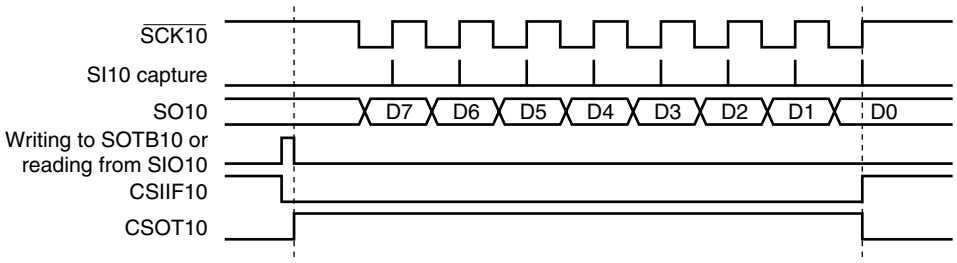
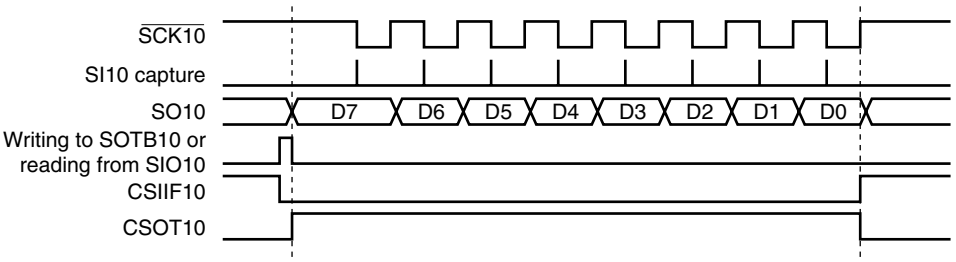


Figure 16-7. Timing of Clock/Data Phase

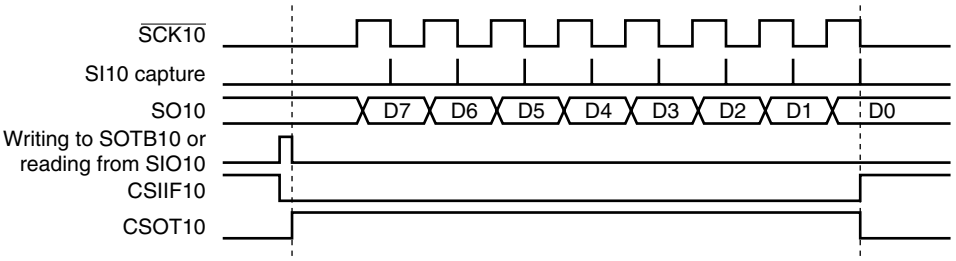
(a) Type 1: CKP10 = 0, DAP10 = 0, DIR10 = 0



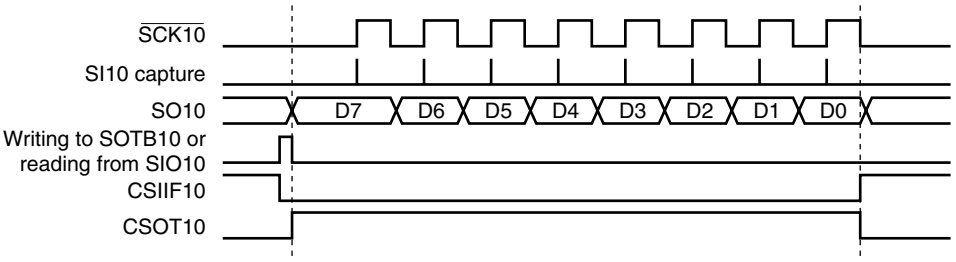
(b) Type 2: CKP10 = 0, DAP10 = 1, DIR10 = 0



(c) Type 3: CKP10 = 1, DAP10 = 0, DIR10 = 0



(d) Type 4: CKP10 = 1, DAP10 = 1, DIR10 = 0



Remark The above figure illustrates a communication operation where data is transmitted with the MSB first.

17.2 Configuration of LCD Controller/Driver

The LCD controller/driver consists of the following hardware.

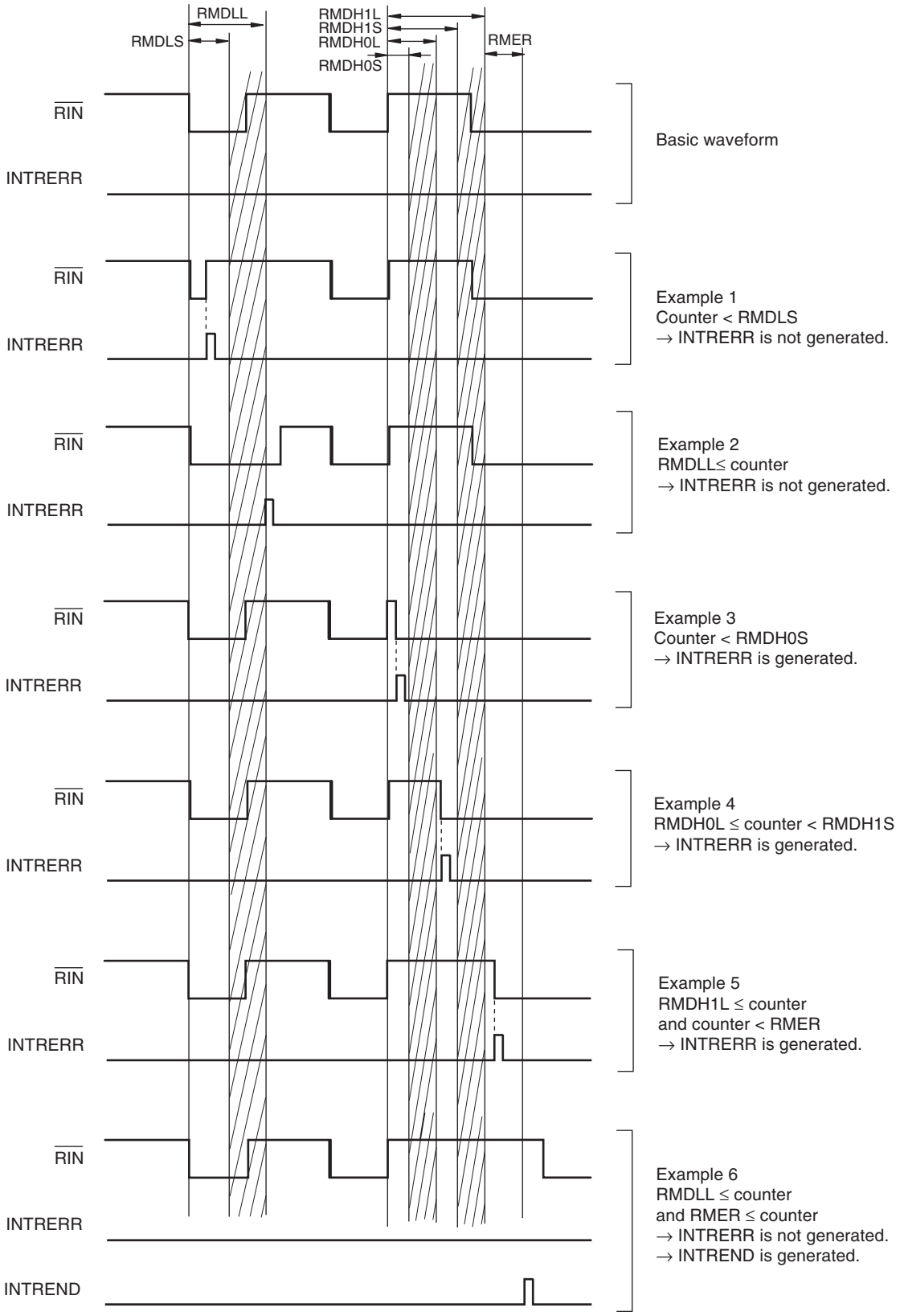
Table 17-2. Configuration of LCD Controller/Driver

Item	Configuration
Display outputs	μPD78F044x: 32 segment signals[Note 1] (SEG0 to SEG31), 8 common signals[Note 1] (COM0 to COM7) μPD78F045x: 32 segment signals[Note 1] (SEG0 to SEG31), 8 common signals[Note 1] (COM0 to COM7) μPD78F046x: 24 segment signals[Note 1] (SEG0 to SEG23), 8 common signals[Note 1] (COM0 to COM7)
Segment key source output	Segment key source signal: 8 (SEG16 (KS0)-SEG23 (KS7))
Control registers	LCD mode register (LCDMD) LCD display mode register (LCDM) LCD clock control register (LCDC0) Port function register 2 (PF2)[Note 2] Port function register ALL (PFALL) Key return mode register (KRM) Port mode register 4 (PM4) Pull-up resistor option register4 (PU4) Port register 14 (P14) Port register 15 (P15)

Notes 1. The four segment signal outputs (SEG0 to SEG3) and four common signal outputs (COM4 to COM7) are alternate-function pins. COM4 to COM7 can be used only when eight-time-slice mode is selected by the setting of the LCD display mode register.

2. μPD78F044x and 78F045x only.

Figure 19-15. Generation Timing of INTRERR Signal (Type C reception mode)



20.3 Registers Controlling Interrupt Functions

The following 6 types of registers are used to control the interrupt functions.

- Interrupt request flag register (IF0L, IF0H, IF1L, IF1H)
- Interrupt mask flag register (MK0L, MK0H, MK1L, MK1H)
- Priority specification flag register (PR0L, PR0H, PR1L, PR1H)
- External interrupt rising edge enable register (EGP)
- External interrupt falling edge enable register (EGN)
- Program status word (PSW)

Table 20-2 shows a list of interrupt request flags, interrupt mask flags, and priority specification flags corresponding to interrupt request sources.

Table 20-2. Flags Corresponding to Interrupt Request Sources (1/2)

Interrupt Source	Interrupt Request Flag		Interrupt Mask Flag		Priority Specification Flag	
		Register		Register		Register
INTLVI	LVIIF	IF0L	LVIMK	MK0L	LVIPR	PR0L
INTP0	PIF0		PMK0		PPR0	
INTP1	PIF1		PMK1		PPR1	
INTP2	PIF2		PMK2		PPR2	
INTP3	PIF3		PMK3		PPR3	
INTP4	PIF4		PMK4		PPR4	
INTSRE6	SREIF6		SREMK6		SREPR6	
INTSR6	SRIF6	IF0H	SRMK6	MK0H	SRPR6	PR0H
INTST6	STIF6		STMK6		STPR6	
INTCSI10	CSIIF10 Note 1		CSIMK10 Note 2		CSIPR10 Note 3	
INTST0	STIF0 Note 1		STMK0 Note 2		STPR0 Note 3	
INTTMH1	TMIFH1		TMMKH1		TMPRH1	
INTTMH0	TMIFH0		TMMKH0		TMPRH0	
INTTM50	TMIF50		TMMK50		TMPR50	
INTTM000	TMIF000		TMMK000		TMPR000	
INTTM010	TMIF010		TMMK010		TMPR010	

Notes 1. If either interrupt source INTCSI10 or INTST0 is generated, bit 2 of IF0H is set (1).

2. Bit 2 of MK0H supports both interrupt sources INTCSI10 and INTST0.

3. Bit 2 of PR0H supports both interrupt sources INTCSI10 and INTST0.

(4) External interrupt rising edge enable register (EGP), external interrupt falling edge enable register (EGN)

These registers specify the valid edge for INTP0 to INTP4.

EGP and EGN are set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Figure 20-5. Format of External Interrupt Rising Edge Enable Register (EGP) and External Interrupt Falling Edge Enable Register (EGN)

Address: FF48H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGP	0	0	0	EGP4	EGP3	EGP2	EGP1	EGP0

Address: FF49H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGN	0	0	0	EGN4	EGN3	EGN2	EGN1	EGN0

EGPn	EGNn	INTPn pin valid edge selection (n = 0 to 4)
0	0	Edge detection disabled
0	1	Falling edge
1	0	Rising edge
1	1	Both rising and falling edges

Table 20-3 shows the ports corresponding to EGPn and EGNn.

Table 20-3. Ports Corresponding to EGPn and EGNn

Detection Enable Register		Edge Detection Port	Interrupt Request Signal
EGP0	EGN0	P120/EXLVI	INTP0
EGP1	EGN1	P34/TI52/TI010/TO00/RTC1HZ	INTP1
EGP2	EGN2	P33/TI000/RTCDIV/RTCCL/BUZ	INTP2
EGP3	EGN3	P31/TOH1	INTP3
EGP4	EGN4	P14	INTP4

Caution Select the port mode by clearing EGPn and EGNn to 0 because an edge may be detected when the external interrupt function is switched to the port function.

Remark n = 0 to 4

Table 27-14. Interrupt Response Time (Library for Normal Model) (1/2)

Function Name	Interrupt Response Time (Unit: μs)					
	When entry RAM is allocated outside short direct addressing range			When entry RAM is allocated within short direct addressing range		
	RSTOP = 0 and RSTS = 1 (during stable operation of internal high-speed oscillator)		RSTOP = 1 (internal high-speed oscillator stopped)Note	RSTOP = 0 and RSTS = 1 (during stable operation of internal high-speed oscillator)		RSTOP = 1 (internal high-speed oscillator stopped)Note
	MCS = 0 (CPU operates with internal high-speed oscillation clock)	MCS = 1 (CPU operates with high-speed system clock)	MCS = 1 (CPU operates with high-speed system clock)	MCS = 0 (CPU operates with internal high-speed oscillation clock)	MCS = 1 (CPU operates with high-speed system clock)	MCS = 1 (CPU operates with high-speed system clock)
Block erase function	179/fCPU+1269	179/fCPU+1269	179/fCPU+1912	179/fCPU+703	179/fCPU+703	179/fCPU+713
Word write function	333/fCPU+1098	333/fCPU+1098	333/fCPU+1742	333/fCPU+533	333/fCPU+533	333/fCPU+543
Block verify function	179/fCPU+1013	179/fCPU+1013	179/fCPU+1656	179/fCPU+448	179/fCPU+448	179/fCPU+456
Block blank check function	179/fCPU+993	179/fCPU+993	179/fCPU+1637	179/fCPU+428	179/fCPU+428	179/fCPU+438
Set information function	80/fCPU+833	80/fCPU+833	80/fCPU+1477	80/fCPU+346	80/fCPU+346	80/fCPU+346
EEPROM write function	333/fCPU+1107	333/fCPU+1107	333/fCPU+1751	333/fCPU+542	333/fCPU+542	333/fCPU+552

Note This is the function processing time when the function is executed immediately after the self programming start function has been executed. The processing time after a function other than the self programming start function has been executed is the same as that of RSTOP = 0.

Remark RSTOP: Bit 0 of the internal oscillation mode register (RCM)
RSTS: Bit 7 of RCM
MCS: Bit 1 of main clock mode register (MCM)
f_{CPU}: CPU clock frequency
W: Number of words to be written (1 word = 4 bytes)