Renesas Electronics America Inc - UPD78F0462GK-GAJ-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	3-Wire SIO, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	46
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b, 3x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0462gk-gaj-ax

(3/3)

Item \ Part Number			78K0/LF3													
			μPD78F047x					μPD78F048x					μPD78F049x				
			80 Pins														
Flash memory (KB)			16	24	32	48	60	16	24	32	48	60	16	24	32	48	60
RAM (KB)			0.75	1	1	2	2	0.75	1	1	2	2	0.75	1	1	2	2
Power supply voltage			V_{DD} = 1.8 to 5.5 V														
Regulator			Provided														
Minimum instruction execution time			0.2 μs (10 MHz: V_{DD} = 2.7 to 5.5 V)/ 0.4 μs (5 MHz: V_{DD} = 1.8 to 5.5 V)														
Clock	Main	High-speed system clock	10 MHz: V_{DD} = 2.7 to 5.5 V/5 MHz: V_{DD} = 1.8 to 5.5 V														
		Internal high-speed oscillation clock	8 MHz (TYP.): V_{DD} = 1.8 to 5.5 V														
	Subclock		32.768 kHz (TYP.): V_{DD} = 1.8 to 5.5 V														
	Internal low-speed oscillation clock		240 kHz (TYP.): V_{DD} = 1.8 to 5.5 V														
Port	Total		62														
Timer	16 bits (TM0)		1 ch														
	8 bits (TM5)		3 ch														
	8 bits (TMH)		3 ch														
	RTC		1 ch														
	WDT		1 ch														
Serial interface	3-wire CSI/UART[Note 1]		1 ch														
	Automatic transmit/ receive 3-wire CSI		1 ch														
	UART supporting LIN-bus[Note 2]		1 ch														
LCD	Type		External resistance division and internal resistance division are switchable.														
	Segment signal		40 (36) [36 (32)] [Note 3, 4]										32 (28) [28 (24)] [Note 3, 4]				
	Common signal		4 (8)[Note 3]														
10-bit successive approximation type A/D			–					8 ch									
16-bit ΔΣ type A/D			–										3 ch				
Interrupt	External		7														
	Internal		20					21					22				
Segment key source signal output			8 ch														
Key interrupt			8 ch														
Reset	$\overline{\text{RESET}}$ pin		Provided														
	POC		1.59 V ±0.15 V (Time for rising up to 1.8 V : 3.6 ms (MAX.))														
	LVI		The detection level of the supply voltage is selectable in 16 steps.														
	WDT		Provided														
Clock output/ Buzzer output			Provided														
Remote controller receiver			Provided														
MCG			Provided														
On-chip debug function			Provided														
Operating ambient temperature			T_A = −40 to +85°C														

Notes 1. Select either of the functions of these alternate-function pins.

2. The LIN-bus supporting UART pins can be changed to the Automatic transmit/receive 3-wire CSI/UART pins (pin numbers 75 and 76).

3. The values in parentheses are the number of signal outputs when 8com is used.

<R> **4.** The values in square brackets are the number of signal outputs when using the UART6 pins (RxD6, TxD6) on the bottom side.

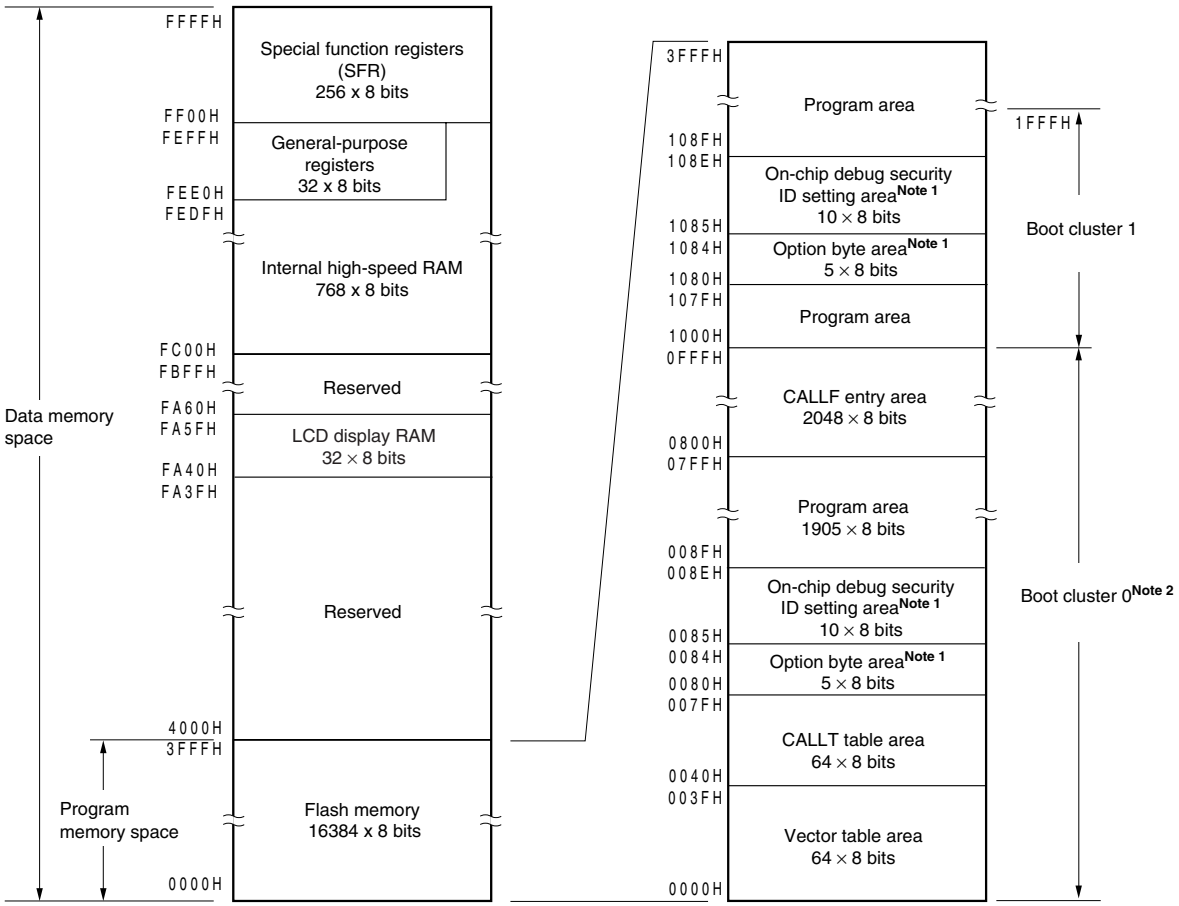
1.9 Outline of Functions (μPD78F046x)

(1/2)

Item		μPD78F0461	μPD78F0462	μPD78F0463	μPD78F0464	μPD78F0465
Internal memory	Flash memory (self-programming supported)[Note]	16 KB	24 KB	32 KB	48 KB	60 KB
	High-speed RAM[Note]	768 bytes	1 KB			
	Expansion RAM[Note]	–			1 KB	
	LCD display RAM	24 × 4 bits (with 4 com) or 20 × 8 bits (with 8 com)				
Memory space		64 KB				
Main system clock (oscillation frequency)	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) 2 to 10 MHz: V_{DD} = 2.7 to 5.5 V, 2 to 5 MHz: V_{DD} = 1.8 to 5.5 V				
	Internal high-speed oscillation clock	Internal oscillation 8 MHz (TYP.): V_{DD} = 1.8 to 5.5 V				
Subsystem clock (oscillation frequency)		XT1 (crystal) oscillation 32.768 kHz (TYP.): V_{DD} = 1.8 to 5.5 V				
Internal low-speed oscillation clock (for TMH1, WDT)		Internal oscillation 240 kHz (TYP.): V_{DD} = 1.8 to 5.5 V				
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)				
Minimum instruction execution time		0.2 μs (high-speed system clock: @ f_{XH} = 10 MHz operation)				
		0.25 μs (internal high-speed oscillation clock: @ f_{RH} = 8 MHz (TYP.) operation)				
		122 μs (subsystem clock: @ f_{SUB} = 32.768 kHz operation)				
Instruction set		• 8-bit operation and 16-bit operation • Bit manipulate (set, reset, test, and Boolean operation) • BCD adjust, etc.				
I/O ports		Total: 46 CMOS I/O: 42 CMOS input: 4				
Timers		• 16-bit timer/event counter: 1 channel • 8-bit timer/event counter: 3 channels (out of which 2 channels can perform PWM output) • 8-bit timer: 3 channels (out of which 2 channels can perform PWM output) • Real-time counter: 1 channel • Watchdog timer: 1 channel				
	Timer outputs	5 (PWM output: 4 and PPG output: 1)				
	RTC outputs	2 • 1 Hz (Subsystem clock: f_{SUB} = 32.768 kHz) • 512 Hz or 16.384 kHz or 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz)				
Buzzer output		• 1.22 kHz, 2.44 kHz, 4.88 kHz, 9.77 MHz (peripheral hardware clock: @ f_{PRS} = 10 MHz operation)				

Note The internal flash memory capacity, internal high-speed RAM capacity, and internal expansion RAM capacity can be changed using the internal memory size switching register (IMS) and the internal expansion RAM size switching register (IXS).

Figure 3-1. Memory Map (μPD78F0441, 78F0451)



Notes 1. When boot swap is not used: Set the option bytes to 0080H to 0084H, and the on-chip debug security IDs to 0085H to 008EH.

When boot swap is used: Set the option bytes to 0080H to 0084H and 1080H to 1084H, and the on-chip debug security IDs to 0085H to 008EH and 1085H to 108EH.

2. Writing boot cluster 0 can be prohibited depending on the setting of security (see **27.8 Security Setting**).

Remark The flash memory is divided into blocks (one block = 1 KB). For the address values and block numbers, see **Table 3-2 Correspondence Between Address Values and Block Numbers in Flash Memory**.

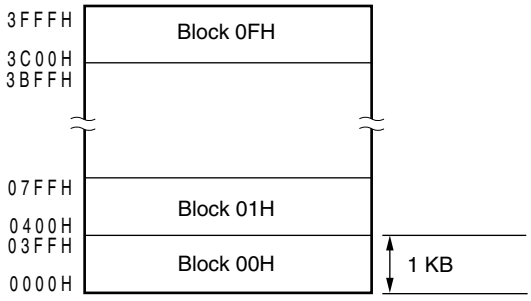
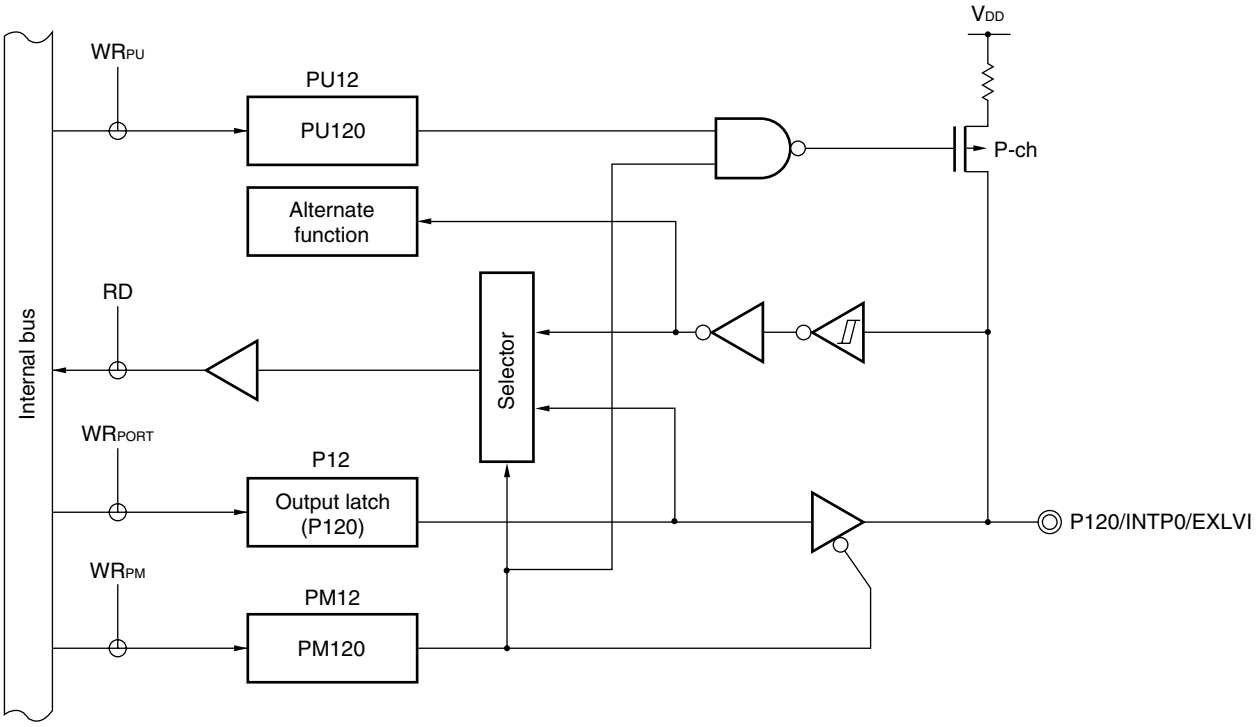


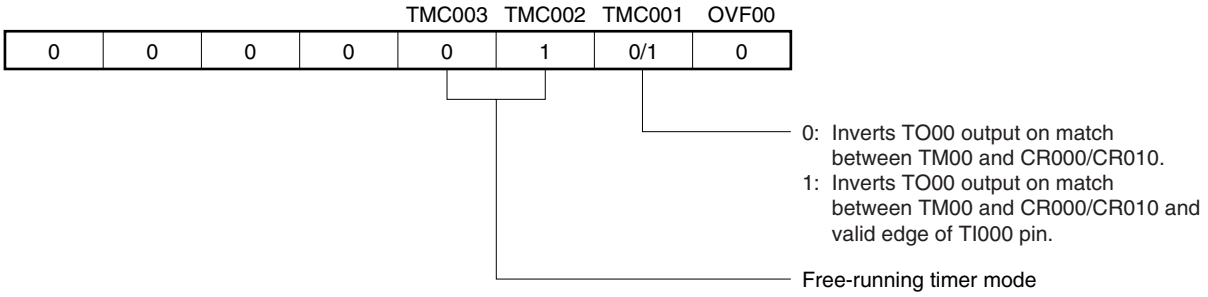
Figure 4-16. Block Diagram of P120



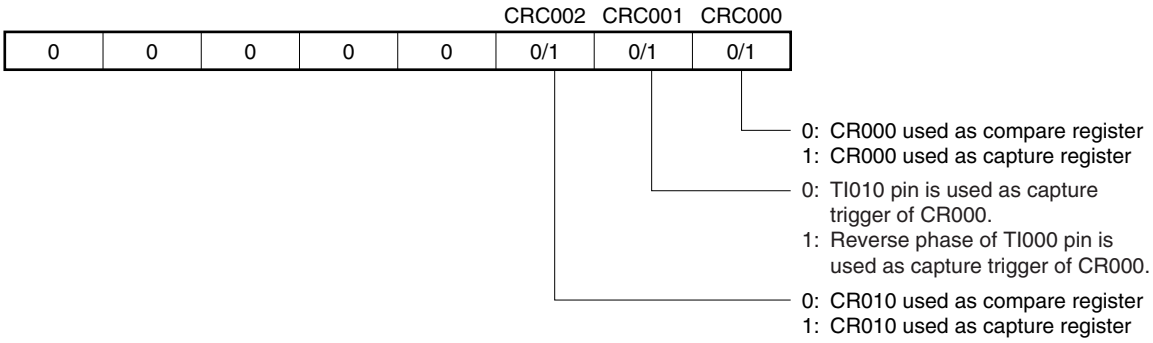
P12: Port register 12
PU12: Pull-up resistor option register 12
PM12: Port mode register 12
RD: Read signal
WR××: Write signal

Figure 6-39. Example of Register Settings in Free-Running Timer Mode (1/2)

(a) 16-bit timer mode control register 00 (TMC00)



(b) Capture/compare control register 00 (CRC00)



(c) 16-bit timer output control register 00 (TOC00)

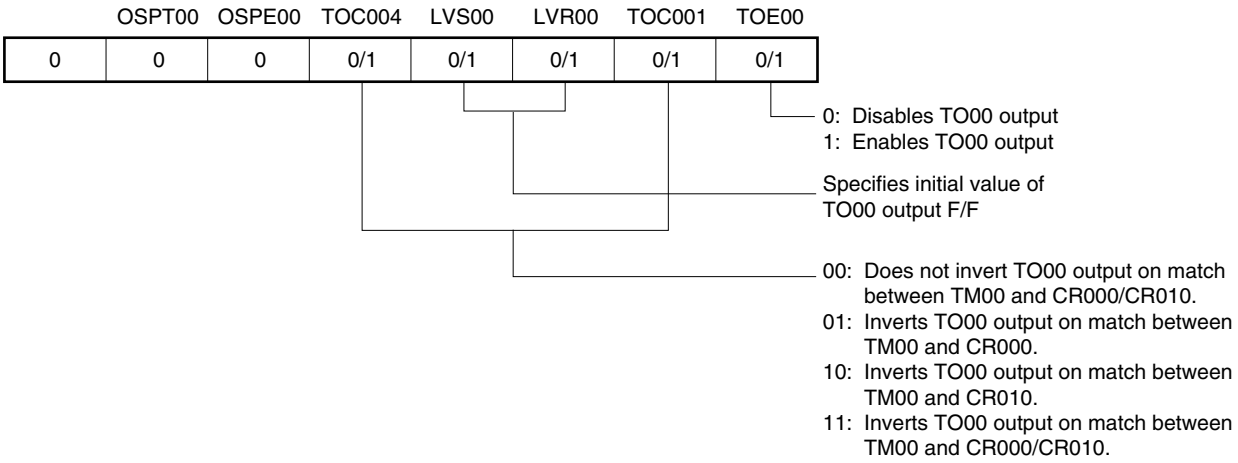
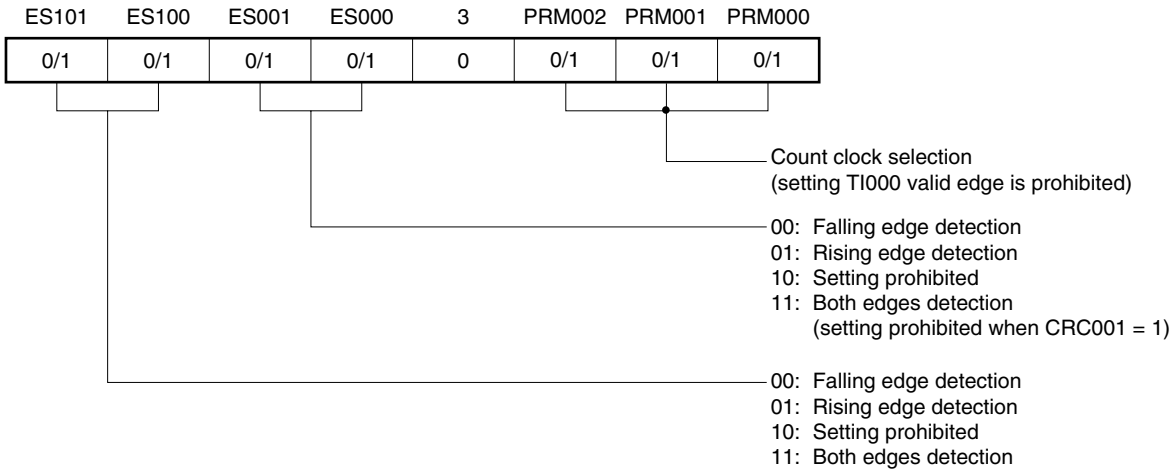


Figure 6-39. Example of Register Settings in Free-Running Timer Mode (2/2)

(d) Prescaler mode register 00 (PRM00)



(e) 16-bit timer counter 00 (TM00)

By reading TM00, the count value can be read.

(f) 16-bit capture/compare register 000 (CR000)

When this register is used as a compare register and when its value matches the count value of TM00, an interrupt signal (INTTM000) is generated. The count value of TM00 is not cleared.

To use this register as a capture register, select either the TI000 or TI010 pin input as a capture trigger. When the valid edge of the capture trigger is detected, the count value of TM00 is stored in CR000.

(g) 16-bit capture/compare register 010 (CR010)

When this register is used as a compare register and when its value matches the count value of TM00, an interrupt signal (INTTM010) is generated. The count value of TM00 is not cleared.

When this register is used as a capture register, the TI000 pin input is used as a capture trigger. When the valid edge of the capture trigger is detected, the count value of TM00 is stored in CR010.

Figure 7-1. Block Diagram of 8-Bit Timer/Event Counter 50

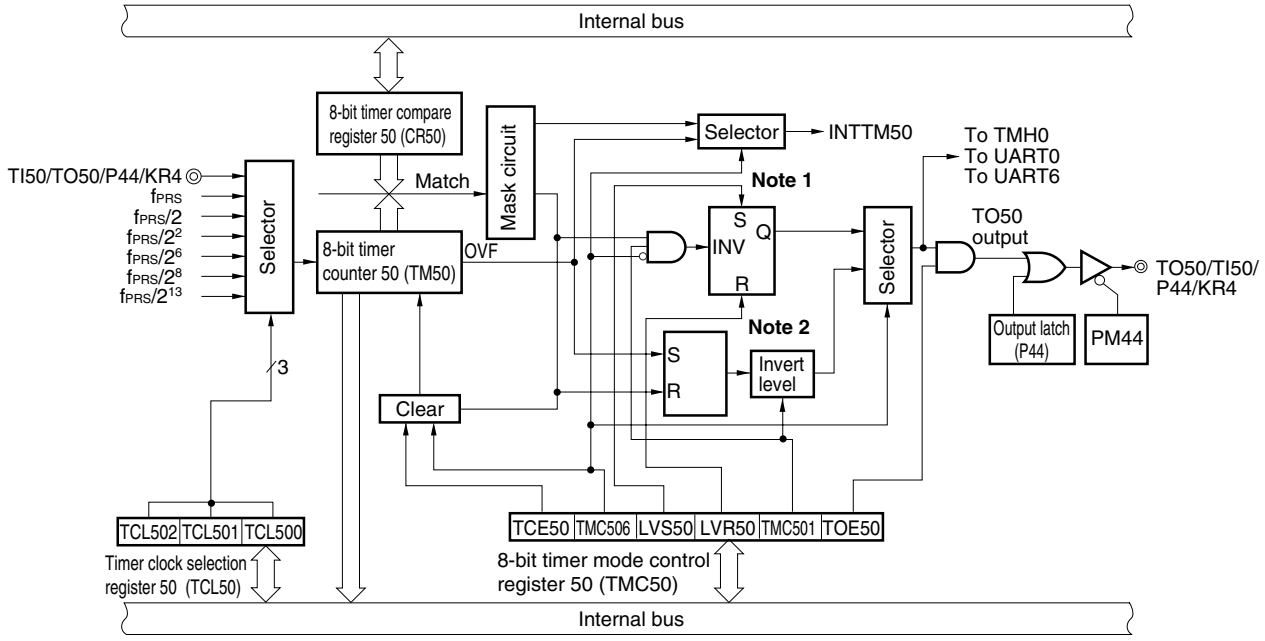
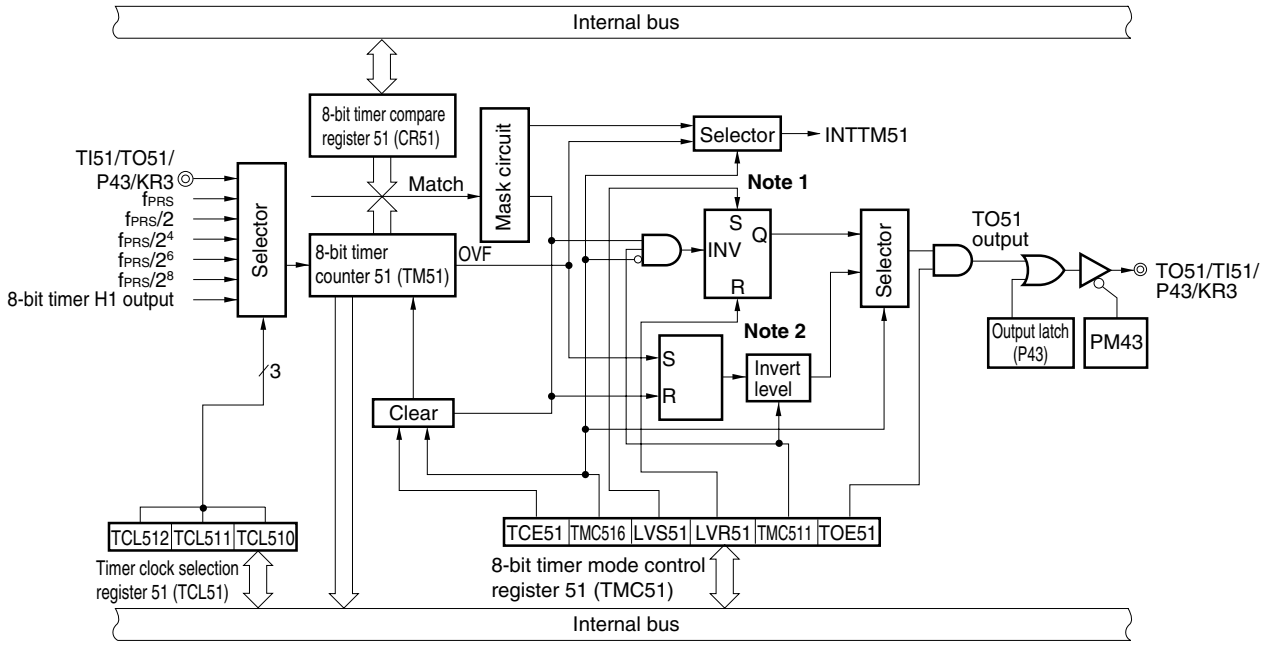


Figure 7-2. Block Diagram of 8-Bit Timer/Event Counter 51



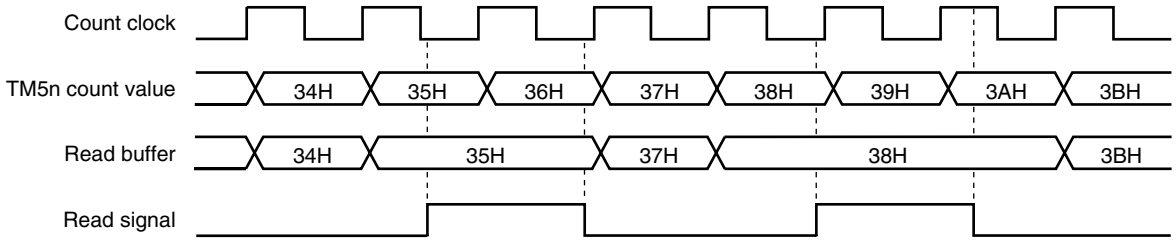
Notes 1. Timer output F/F

2. PWM output F/F

<R> **(3) Reading of 8-bit timer counter 5n (TM5n)**

TM5n can be read without stopping the actual counter, because the count values captured to the buffer are fixed when it is read. The buffer, however, may not be updated when it is read immediately before the counter counts up, because the buffer is updated at the timing the counter counts up.

Figure 7-21. 8-bit Timer Counter 5n (TM5n) Read Timing



Remark n = 0 to 2

10.2 Configuration of Watchdog Timer

The watchdog timer includes the following hardware.

Table 10-1. Configuration of Watchdog Timer

Item	Configuration
Control register	Watchdog timer enable register (WDTE)

How the counter operation is controlled, overflow time, and window open period are set by the option byte.

Table 10-2. Setting of Option Bytes and Watchdog Timer

Setting of Watchdog Timer	Option Byte (0080H)
Window open period	Bits 6 and 5 (WINDOW1, WINDOW0)
Controlling counter operation of watchdog timer	Bit 4 (WDTON)
Overflow time of watchdog timer	Bits 3 to 1 (WDCS2 to WDCS0)

Remark For the option byte, see **CHAPTER 26 OPTION BYTE**.

Figure 10-1. Block Diagram of Watchdog Timer

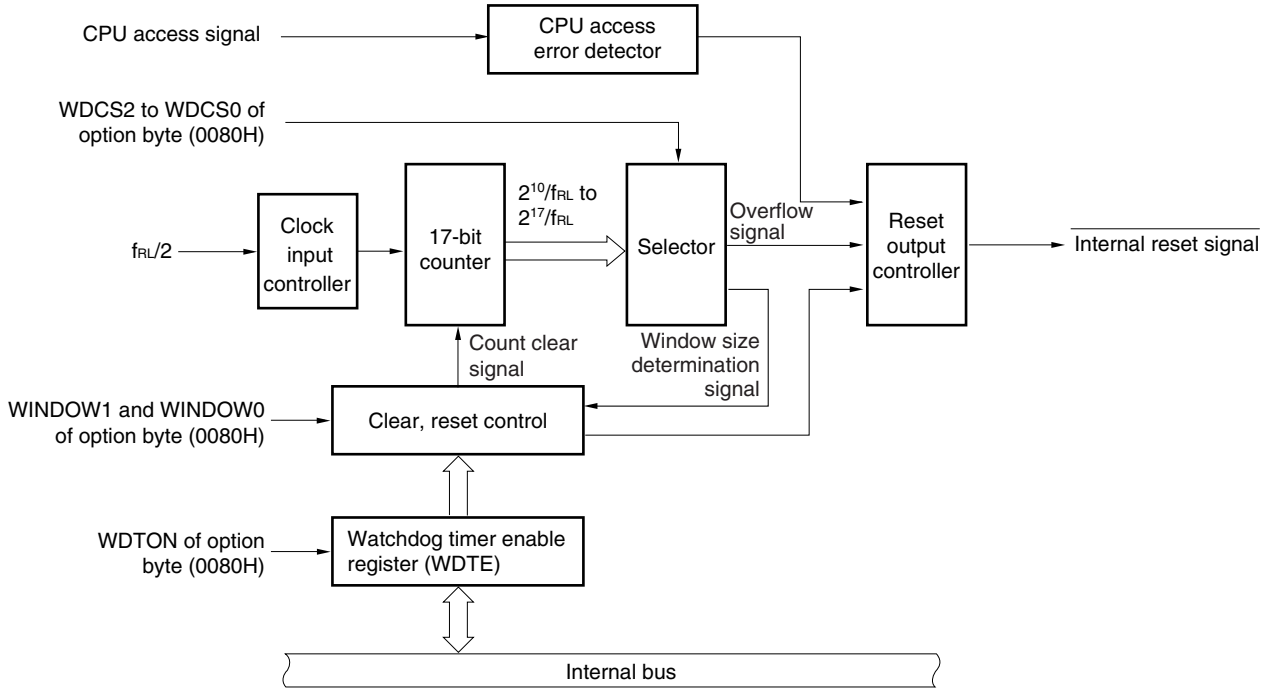


Table 13-1. Sampling Clock (Sampling Time) Setting Conditions

ADDN2	AV_{REF} Condition	Sampling Clock: f_{VP} (Conversion Time in 16-bit Resolution)
Differential input	3.5 V ≤ AV_{REF} ≤ 5.5 V	1.25 MHz max. (52.42 μs min.)
	2.7 V ≤ AV_{REF} < 3.5 V	625 kHz max. (104.85 μs min.)
Single input	2.85 V ≤ AV_{REF} ≤ 5.5 V	625 kHz max. (104.85 μs min.)
	2.7 V ≤ AV_{REF} < 2.85 V	525 kHz max. (124.83 μs min.)

Table 13-2. Examples of Sampling Time under Setting Conditions

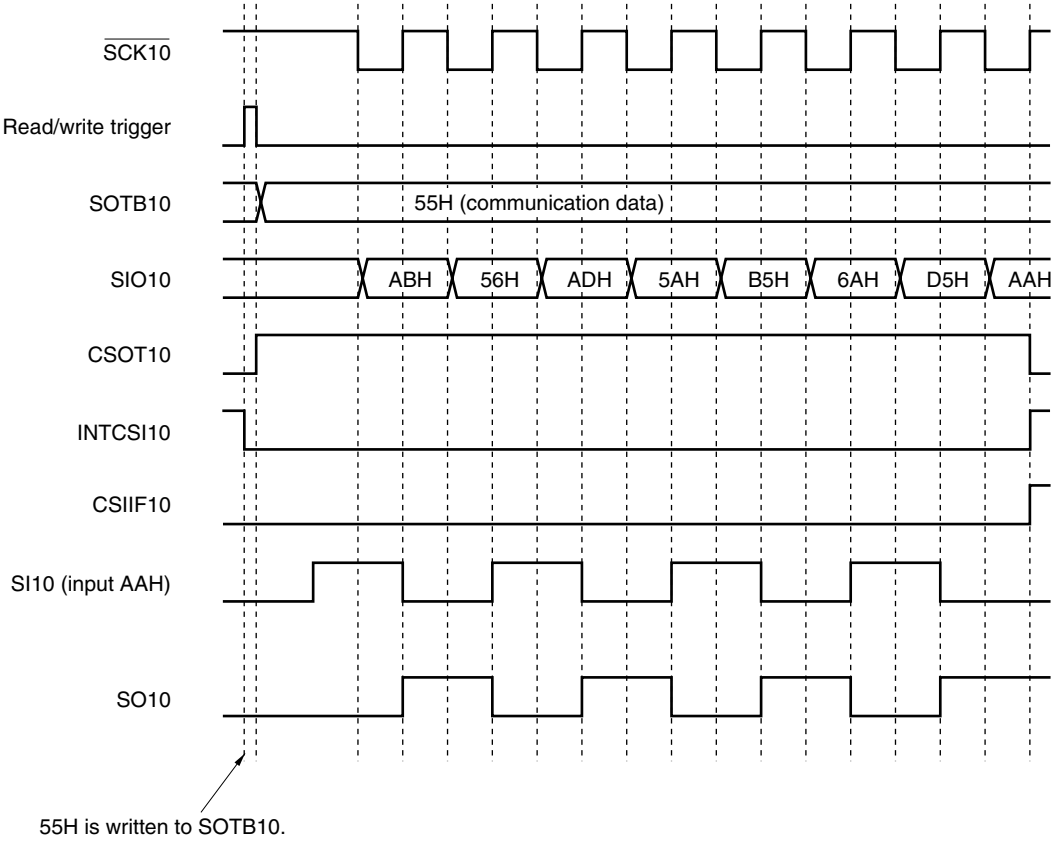
Number of Times of 16-bit ΔΣ Type A/D Sampling: N (Resolution)									
f_{PRS}	f_{VP}	65536 (16-bit)	32768 (15-bit)	16384 (14-bit)	8192 (13-bit)	4096 (12-bit)	2048 (11-bit)	1024 (10-bit)	256 (8-bit)
10 MHz	$f_{PRS}/4$	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited
	$f_{PRS}/8$[Note 1]	52.42 μs	26.21 μs	13.10 μs	6.55 μs	3.27 μs	1.63 μs	0.81 μs	0.20 μs
	$f_{PRS}/16$[Note 2]	104.85 μs	52.42 μs	26.21 μs	13.10 μs	6.55 μs	3.27 μs	1.63 μs	0.41 μs
8 MHz	$f_{PRS}/4$	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited
	$f_{PRS}/8$[Note 1]	65.53 μs	32.76 μs	16.38 μs	8.19 μs	4.09 μs	2.04 μs	1.02 μs	0.25 μs
	$f_{PRS}/16$	131.07 μs	65.53 μs	32.76 μs	16.38 μs	8.19 μs	4.09 μs	2.04 μs	0.51 μs
5 MHz	$f_{PRS}/4$[Note 1]	52.42 μs	26.21 μs	13.10 μs	6.55 μs	3.27 μs	1.63 μs	0.81 μs	0.40 μs
	$f_{PRS}/8$[Note 2]	104.85 μs	52.42 μs	26.21 μs	13.10 μs	6.55 μs	3.27 μs	1.63 μs	0.81 μs
	$f_{PRS}/16$	209.71 μs	104.85 μs	52.42 μs	26.21 μs	13.10 μs	6.55 μs	3.27 μs	1.63 μs
4 MHz	$f_{PRS}/4$[Note 1]	65.53 μs	32.76 μs	16.38 μs	8.19 μs	4.09 μs	2.04 μs	1.02 μs	0.25 μs
	$f_{PRS}/8$	131.07 μs	65.53 μs	32.76 μs	16.38 μs	8.19 μs	4.09 μs	2.04 μs	0.51 μs
	$f_{PRS}/16$	262.14 μs	131.07 μs	65.53 μs	32.76 μs	16.38 μs	8.19 μs	4.09 μs	1.02 μs
2 MHz	$f_{PRS}/4$	131.07 μs	65.53 μs	32.76 μs	16.38 μs	8.19 μs	4.09 μs	2.04 μs	0.51 μs
	$f_{PRS}/8$	262.14 μs	131.07 μs	65.53 μs	32.76 μs	16.38 μs	8.19 μs	4.09 μs	1.02 μs
	$f_{PRS}/16$	524.28 μs	262.14 μs	131.07 μs	65.53 μs	32.76 μs	16.38 μs	8.19 μs	2.04 μs
–	$f_{SUB}/2$	4 s	2 s	1 s	500 ms	250 ms	125 ms	62.5 ms	15.62 ms

Notes 1. Setting the differential input mode (2.7 V ≤ AV_{REF} < 3.5 V) and single input mode is prohibited since the sampling time conditions are not satisfied in these modes.

2. Setting the single input mode (2.7 V ≤ AV_{REF} < 2.85 V) is prohibited since the sampling time conditions are not satisfied in this modes.

Figure 16-6. Timing in 3-Wire Serial I/O Mode (2/2)

(b) Transmission/reception timing (Type 2: TRMD10 = 1, DIR10 = 0, CKP10 = 0, DAP10 = 1)



(6) Key return mode register (KRM)

This register is used to specify that a pin is to be used as a segment key scan input pin when using the segment key scan function.

See Figure 21-2 Format of Key Return Mode Register (KRM) when not using the segment key scan function.

KRM is set using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets 00H.

Figure 17-7. Format of Key return mode register (KRM)

Address: FF6EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
KRM	0	0	0	KRM4	KRM3	KRM2	KRM1	KRM0

KRMn	Setting segment key scan input pin (n = 0 to 4)
0	Does not use specified pin as segment key scan input pin.
1	Uses specified pin as segment key scan input pin.

Cautions 1. If KRM is changed, the interrupt request flag may be set. Therefore, disable interrupts and then change the KRM register. Clear the interrupt request flag and enable interrupts.

2. When set not to use the specified pin as a segment key scan input pin (KRMn = 0), the corresponding P4n pin can be used as a normal port.

3. When using the P40/KR0/V_{LC3} pin for the key interrupt function (KR0), set the LCD display mode register (LCDM) to a setting other than the 1/4 bias method. When set to the 1/4 bias method, the P40/KR0/V_{LC3} pin functions as V_{LC3}.

17.7 Display Modes

17.7.1 Static display example

Figure 17-18 shows how the three-digit LCD panel having the display pattern shown in Figure 17-17 is connected to the segment signals (SEG0 to SEG23) and the common signal (COM0) of the 78K0/LE3 chip. This example displays data "12.3" in the LCD panel. The contents of the display data memory (FA40H to FA57H) correspond to this display.

The following description focuses on numeral "2." (2.) displayed in the second digit. To display "2." in the LCD panel, it is necessary to apply the select or deselect voltage to the SEG8 to SEG15 pins according to Table 17-6 at the timing of the common signal COM0; see **Figure 17-17** for the relationship between the segment signals and LCD segments.

Table 17-6. Select and Deselect Voltages (COM0)

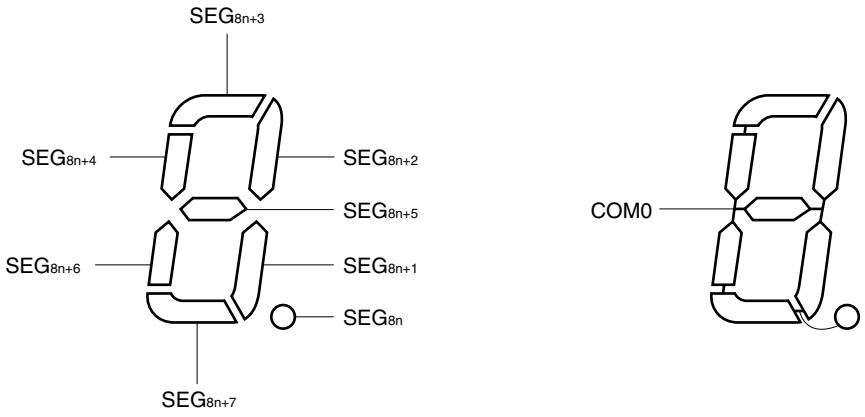
Segment / Common	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15
COM0	Select	Deselect	Select	Select	Deselect	Select	Select	Select

According to Table 17-6, it is determined that the bit-0 pattern of the display data memory locations (FA48H to FA4FH) must be 10110111.

Figure 17-19 shows the LCD drive waveforms of SEG11 and SEG12, and COM0. When the select voltage is applied to SEG11 at the timing of COM0, an alternate rectangle waveform, $+V_{LCD}/-V_{LCD}$, is generated to turn on the corresponding LCD segment.

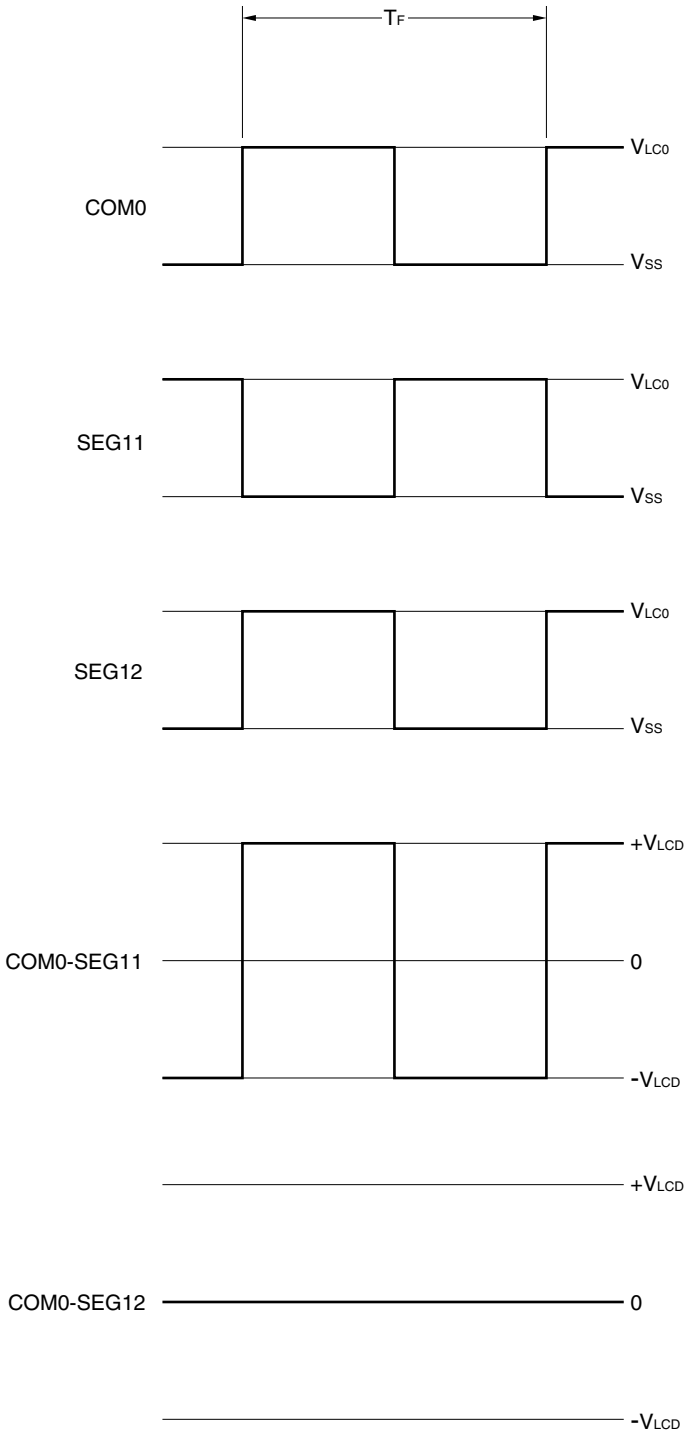
COM1 to COM3 are supplied with the same waveform as for COM0. So, COM0 to COM3 may be connected together to increase the driving capacity.

Figure 17-17 Static LCD Display Pattern and Electrode Connections



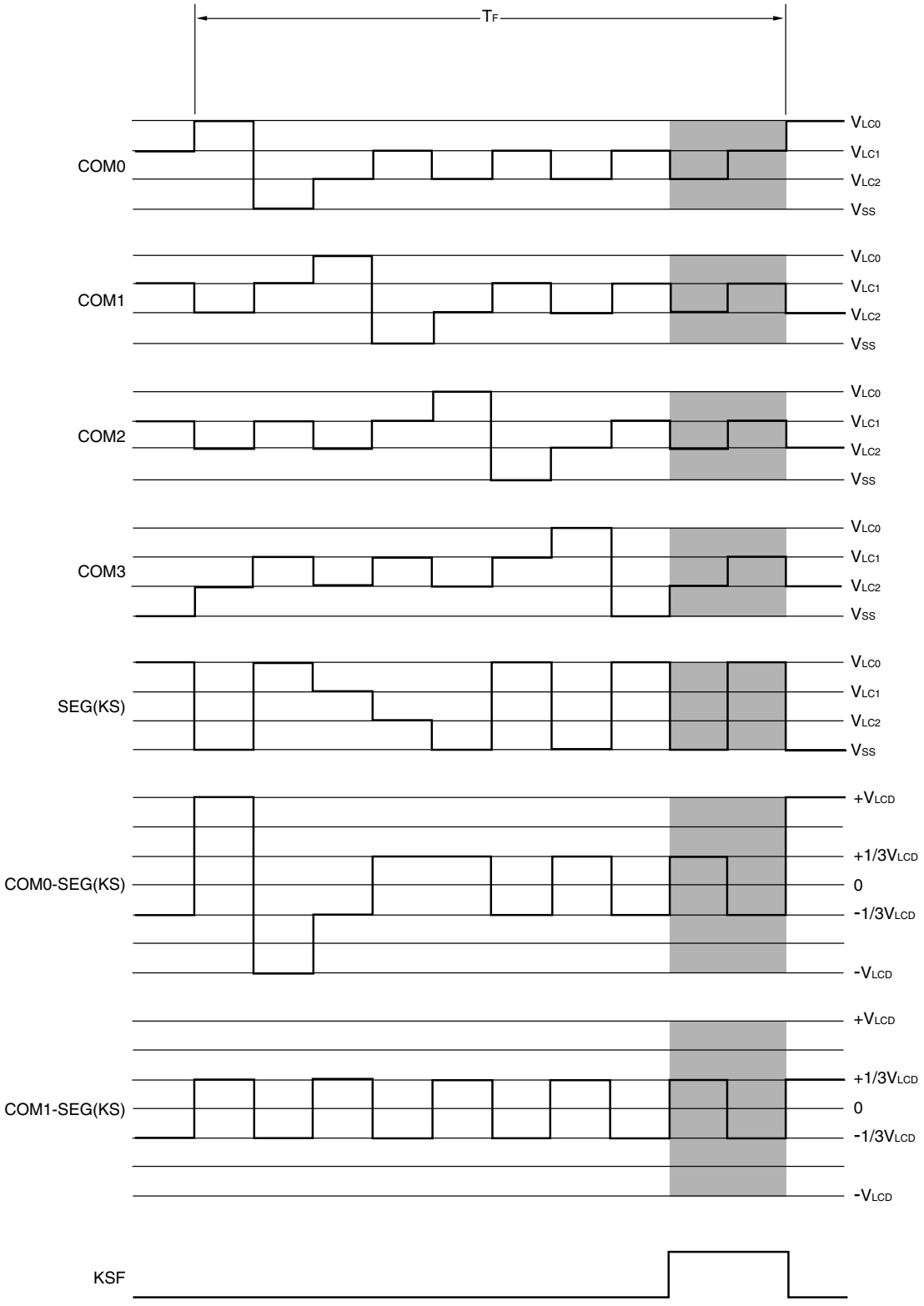
Remark n = 0 to 2

Figure 17-19. Static LCD Drive Waveform Examples



(b) When segment key scan function is used (KSON = 1)

<Key input wait>



Shaded sections: Segment key scan output period

17.7.5 Eight-time-slice display example

Figure 17-31 shows how the 15×8 dots LCD panel having the display pattern shown in Figure 17-30 is connected to the segment signals (SEG4 to SEG18) and the common signals (COM0 to COM7) of the 78K0/LE3 chip. This example displays data "123" in the LCD panel. The contents of the display data memory (addresses FA44H to FA52H) correspond to this display.

The following description focuses on numeral "3." (∃) displayed in the first digit. To display "3." in the LCD panel, it is necessary to apply the select or deselect voltage to the SEG4 and SEG8 pins according to Table 17-10 at the timing of the common signals COM0 to COM7; see Figure 17-30 for the relationship between the segment signals and LCD segments.

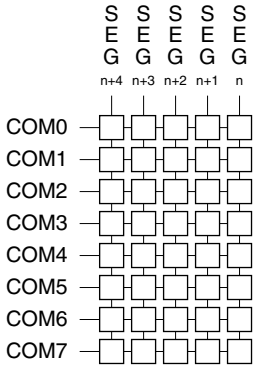
Table 17-10. Select and Deselect Voltages (COM0 to COM7)

Segment / Common	SEG4	SEG5	SEG6	SEG7	SEG8
COM0	Select	Select	Select	Select	Select
COM1	Deselect	Select	Deselect	Deselect	Deselect
COM2	Deselect	Deselect	Select	Deselect	Deselect
COM3	Deselect	Select	Deselect	Deselect	Deselect
COM4	Select	Deselect	Deselect	Deselect	Deselect
COM5	Select	Deselect	Deselect	Deselect	Select
COM6	Deselect	Select	Select	Select	Deselect
COM7	Deselect	Deselect	Deselect	Deselect	Deselect

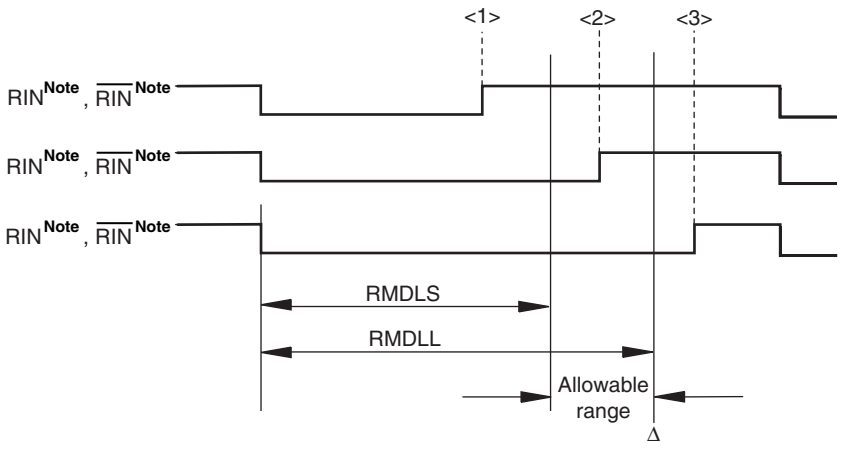
According to Table 17-10, it is determined that the display data memory location (FA44H) that corresponds to SEG4 must contain 00110001.

Figure 17-32 shows examples of LCD drive waveforms between the SEG4 signal and each common signal. When the select voltage is applied to SEG4 at the timing of COM0, a waveform is generated to turn on the corresponding LCD segment.

Figure 17-30. Eight-Time-Slice LCD Display Pattern and Electrode Connections



(3) Data low level width determination



Note RIN is generated in type A reception mode, and $\overline{\text{RIN}}$ is generated in type B and type C reception modes.

Relationship Between RMDLS/RMDLL/Counter	Position of Waveform	Corresponding Operation
Counter < RMDLS	<1>: Short	Error interrupt INTRERR is generated note. Measuring guide pulse high-level width is started.
RMDLS ≤ counter < RMDLL	<2>: Within the range	Measuring data high-level width is started.
RMDLL ≤ counter	<3>: Long	(Type A reception mode) Measuring the end width is started from the Δ point. (Type B, Type C reception modes) Error interrupt INTRERR is generated at the Δ point.note.

Note In type C reception mode, before the first INTDFULL interrupt is generated, INTRERR will not be generated. However, RMSR and RMSCR will be cleared.

(3) Priority specification flag registers (PR0L, PR0H, PR1L, PR1H)

The priority specification flag registers are used to set the corresponding maskable interrupt priority order.

PR0L, PR0H, PR1L, and PR1H are set by a 1-bit or 8-bit memory manipulation instruction. If PR0L and PR0H, and PR1L and PR1H are combined to form 16-bit registers PR0 and PR1, they are set by a 16-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

Figure 20-4. Format of Priority Specification Flag Registers (PR0L, PR0H, PR1L, PR1H)

Address: FFE8H After reset: FFH R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	<1>	<0>
PR0L	SREPR6	1	PPR4	PPR3	PPR2	PPR1	PPR0	LVIPR

Address: FFE9H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR0H	TMPR010	TMPR000	TMPR50	TMPRH0	TMPRH1	CSIPR10 STPR0	STPR6	SRPR6

Address: FFEAH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
<R> PR1L	TMPR52	DSADPR Note 2	RTCIPR	KRPR	TMPR51	RTCPR	SRPR0	ADPR Note 1

Address: FFEBH After reset: FFH R/W

Symbol	7	6	5	4	<3>	<2>	<1>	<0>
PR1H	1	1	1	1	RERRPR GPPR RENDPR DFULLPR	RINPR	MCGPR	TMHPR2

XXPRX	Priority level selection
0	High priority level
1	Low priority level

Notes 1. μPD78F045x and 78F046x only.

2. μPD78F046x only.

Caution Be sure to set bit 6 of PR0L and bits 4 to 7 of PR1H to 1.

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag
				Note 1	Note 2		Z AC CY
16-bit operation	**ADDW**	AX, #word	3	6	–	AX, CY ← AX + word	× × ×
	SUBW	AX, #word	3	6	–	AX, CY ← AX – word	× × ×
	CMPW	AX, #word	3	6	–	AX – word	× × ×
Multiply/ divide	**MULU**	X	2	16	–	AX ← A × X	
	DIVUW	C	2	25	–	AX (Quotient), C (Remainder) ← AX ÷ C	
Increment/ decrement	**INC**	r	1	2	–	r ← r + 1	× ×
		saddr	2	4	6	(saddr) ← (saddr) + 1	× ×
	DEC	r	1	2	–	r ← r – 1	× ×
		saddr	2	4	6	(saddr) ← (saddr) – 1	× ×
	INCW	rp	1	4	–	rp ← rp + 1	
	DECW	rp	1	4	–	rp ← rp – 1	
Rotate	**ROR**	A, 1	1	2	–	(CY, A_7 ← A_0, A_{m-1} ← A_m) × 1 time	×
	ROL	A, 1	1	2	–	(CY, A_0 ← A_7, A_{m+1} ← A_m) × 1 time	×
	RORC	A, 1	1	2	–	(CY ← A_0, A_7 ← CY, A_{m-1} ← A_m) × 1 time	×
	ROLC	A, 1	1	2	–	(CY ← A_7, A_0 ← CY, A_{m+1} ← A_m) × 1 time	×
	ROR4	[HL]	2	10	12	A_{3-0} ← $(HL)_{3-0}$, $(HL)_{7-4}$ ← A_{3-0}, $(HL)_{3-0}$ ← $(HL)_{7-4}$	
	ROL4	[HL]	2	10	12	A_{3-0} ← $(HL)_{7-4}$, $(HL)_{3-0}$ ← A_{3-0}, $(HL)_{7-4}$ ← $(HL)_{3-0}$	
BCD adjustment	**ADJBA**		2	4	–	Decimal Adjust Accumulator after Addition	× × ×
	ADJBS		2	4	–	Decimal Adjust Accumulator after Subtract	× × ×
Bit manipulate	**MOV1**	CY, saddr.bit	3	6	7	CY ← (saddr.bit)	×
		CY, sfr.bit	3	–	7	CY ← sfr.bit	×
		CY, A.bit	2	4	–	CY ← A.bit	×
		CY, PSW.bit	3	–	7	CY ← PSW.bit	×
		CY, [HL].bit	2	6	7	CY ← (HL).bit	×
		saddr.bit, CY	3	6	8	(saddr.bit) ← CY	
		sfr.bit, CY	3	–	8	sfr.bit ← CY	
		A.bit, CY	2	4	–	A.bit ← CY	
		PSW.bit, CY	3	–	8	PSW.bit ← CY	× ×
		[HL].bit, CY	2	6	8	(HL).bit ← CY	

Notes 1. When the internal high-speed RAM area is accessed or for an instruction with no data access

2. When an area except the internal high-speed RAM area is accessed

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

2. This clock cycle applies to the internal ROM program.

(2) 16-bit instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

First Operand \ Second Operand	#word	AX	rp[Note]	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW[Note]						INCW DECW PUSH POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp = BC, DE, HL

(3) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

First Operand \ Second Operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1