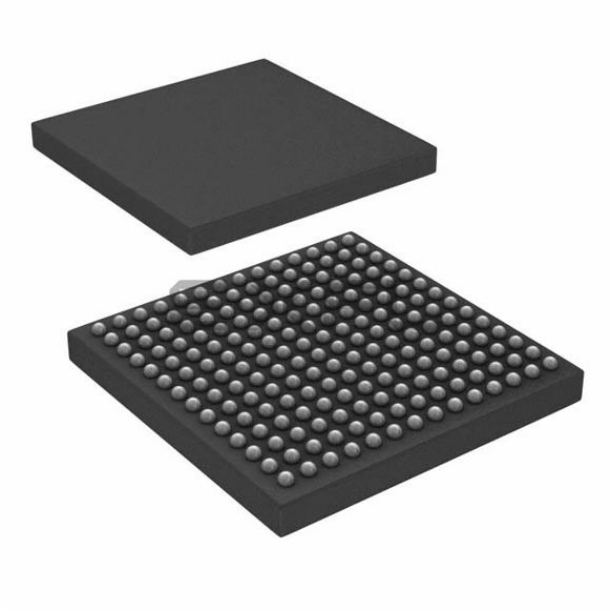

Welcome to E-XFL.COM

Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	SPI, SSP
Clock Rate	150MHz
Non-Volatile Memory	External
On-Chip RAM	112kB
Voltage - I/O	3.30V
Voltage - Core	2.50V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	196-BGA, CSPBGA
Supplier Device Package	196-MBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21991bbcz

ADSP-21991* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- USB-Based Emulator and High Performance USB-Based Emulator

DOCUMENTATION

Application Notes

- AN-227: Digital Control System Design with the ADSP-2100 Family
- EE-06: ADSP-21xx Serial Port Startup Issues
- EE-100: ADSP-218x External Overlay Memory
- EE-102: Mode D and ADSP-218x Pin Compatibility - the FAQs
- EE-104: Setting Up Streams with the VisualDSP Debugger
- EE-11: ADSP-2181 Priority Chain & IDMA Holdoffs
- EE-115: ADSP-2189 IDMA Interface to Motorola MC68300 Family of Microprocessors
- EE-12: Interrupts and Programmable Flags on the ADSP-2185/2186
- EE-121: Porting Code from ADSP-21xx to ADSP-219x
- EE-122: Coding for Performance on the ADSP-219x
- EE-123: An Overview of the ADSP-219x Pipeline
- EE-124: Booting up the ADSP-2192
- EE-125: ADSP-218x Embedded System Software Management and In-System-Programming (ISP)
- EE-128: DSP in C++: Calling Assembly Class Member Functions From C++
- EE-129: ADSP-2192 Interprocessor Communication
- EE-130: Making Fast Transition from ADSP-21xx to ADSP-219x
- EE-131: Booting the ADSP-2191/95/96 DSPs
- EE-133: Converting From Legacy Architecture Files To Linker Description Files for the ADSP-218x
- EE-139: Interfacing the ADSP-2191 to an AD7476 via the SPI Port
- EE-142: Autobuffering, C and FFTs on the ADSP-218x
- EE-144: Creating a Master-Slave SPI Interface Between Two ADSP-2191 DSPs
- EE-145: SPI Booting of the ADSP-2191 using the Atmel AD25020N on an EZ-KIT Lite Evaluation Board
- EE-146: Implementing a Boot Manager for ADSP-218x Family DSPs
- EE-152: Using Software Overlays with the ADSP-219x and VisualDSP 2.0++
- EE-153: ADSP-2191 Programmable PLL
- EE-154: ADSP-2191 Host Port Interface
- EE-156: Support for the H.100 protocol on the ADSP-2191

The flexible architecture and comprehensive instruction set of the ADSP-21991 support multiple operations in parallel. For example, in one processor cycle, the ADSP-21991 can:

- Generate an address for the next instruction fetch
- Fetch the next instruction
- Perform one or two data moves
- Update one or two data address pointers
- Perform a computational operation

These operations take place while the processor continues to:

- Receive and transmit data through the serial port
- Receive or transmit data over the SPI port
- Access external memory through the external memory interface
- Decrement the timers
- Operate the embedded control peripherals (ADC, PWM, EIU, etc.)

DSP Core Architecture

- 6.25 ns instruction cycle time (internal), for up to 160 MIPS sustained performance (6.67 ns instruction cycle time for 150 MIPS sustained performance)
- ADSP-218x family code compatible with the same easy to use algebraic syntax
- Single cycle instruction execution
- Up to 1M words of addressable memory space with twenty four bits of addressing width
- Dual purpose program memory for both instruction and data storage
- Fully transparent instruction cache allows dual operand fetches in every instruction cycle
- Unified memory space permits flexible address generation, using two independent DAG units
- Independent ALU, multiplier/accumulator, and barrel shifter computational units with dual 40-bit accumulators
- Single cycle context switch between two sets of computational and DAG registers
- Parallel execution of computation and memory instructions
- Pipelined architecture supports efficient code execution at speeds up to 160 MIPS
- Register file computations with all nonconditional, nonparallel computational instructions
- Powerful program sequencer provides zero overhead looping and conditional instruction execution
- Architectural enhancements for compiled C code efficiency
- Architecture enhancements beyond ADSP-218x family are supported with instruction set extensions for added registers, ports, and peripherals.

The clock generator module of the ADSP-21991 includes clock control logic that allows the user to select and change the main clock frequency. The module generates two output clocks: the DSP core clock, CCLK; and the peripheral clock, HCLK. CCLK can sustain clock values of up to 160 MHz, while HCLK can be equal to CCLK or CCLK/2 for values up to a maximum 80 MHz peripheral clock at the 160 MHz CCLK rate.

The ADSP-21991 instruction set provides flexible data moves and multifunction (one or two data moves with a computation) instructions. Every single word instruction can be executed in a single processor cycle. The ADSP-21991 assembly language uses