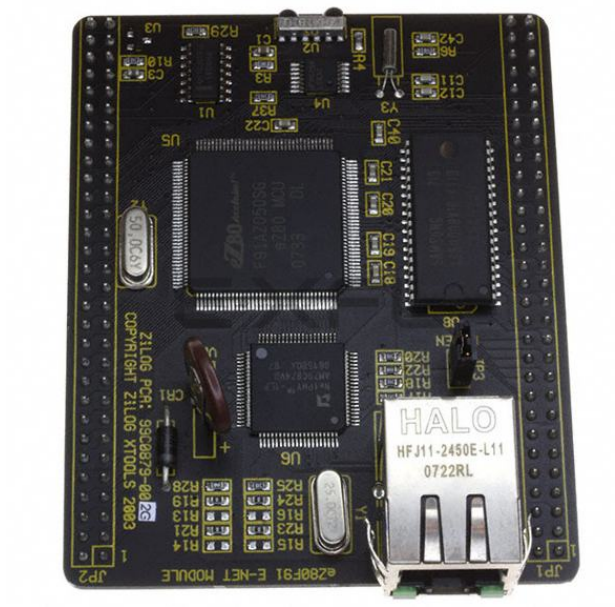
Zilog - EZ80F915050MODG Datasheet



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Applications of Embedded - Microcontroller,

Details	
Product Status	Obsolete
Module/Board Type	MCU, Ethernet Core
Core Processor	eZ80F91
Co-Processor	-
Speed	50MHz
Flash Size	256KB (Internal), 1MB (External)
RAM Size	8KB (Internal), 512KB (External)
Connector Type	Header 2x30
Size / Dimension	2.5" x 3.1" (63.5mm x 78.7mm)
Operating Temperature	0°C ~ 70°C
Purchase URL	https://www.e-xfl.com/product-detail/zilog/ez80f915050modg

Table 2. Pin Identification on the eZ80F91 Device (Continued)

LQFP Pin No	BGA Pin No	Symbol	Function	Signal Direction	Description
78	K12	PD5	GPIO Port D	Bidirectional	This pin is used for GPIO. It is individually programmed as input or output and is also used individually as an interrupt input. Each Port D pin, when programmed as output is selected to be an open-drain or open-source output. Port D is multiplexed with one UART.
		DSR0	Data Set Ready	Input, Active Low	Modem status signal to the UART. This signal is multiplexed with PD5.
79	K11	PD6	GPIO Port D	Bidirectional	This pin is used for GPIO. It is individually programmed as input or output and is also used individually as an interrupt input. Each Port D pin, when programmed as output is selected to be an open-drain or open-source output. Port D is multiplexed with one UART.
		DCD0	Data Carrier Detect	Input, Active Low	Modem status signal to the UART. This signal is multiplexed with PD6.
80	H8	PD7	GPIO Port D	Bidirectional	This pin is used for GPIO. It is individually programmed as input or output and is also used individually as an interrupt input. Each Port D pin, when programmed as output is selected to be an open-drain or open-source output. Port D is multiplexed with one UART.
		RI0	Ring Indicator	Input, Active Low	Modem status signal to the UART. This signal is multiplexed with PD7.
81	J11	V_{DD}	Power Supply		Power Supply.
82	J12	V_{SS}	Ground		Ground.
83	J10	LOOP_FILT	PLL Loop Filter	Analog	Loop Filter pin for the Analog PLL.
84	G7	PLL_V_{SS}	Ground		Ground for Analog PLL.
85	H12	X_{OUT}	System Clock Oscillator Output	Output	This pin is the output of the onboard crystal oscillator. When used, a crystal must be connected between X_{IN} and X_{OUT}.

Table 3. Register Map (Continued)

Address (hex)	Mnemonic	Name	Reset (hex)	CPU Access	Page No
003F	EMAC_FIAD	EMAC PHY Unit Select Address Register	00	R/W	316
0040	EMAC_PTMR	EMAC Transmit Polling Timer Register	00	R/W	316
0041	EMAC_RST	EMAC Reset Control Register	20	R/W	317
0042	EMAC_TLBP_L	EMAC Transmit Lower Boundary Pointer Low Byte	00	R/W	318
0043	EMAC_TLBP_H	EMAC Transmit Lower Boundary Pointer High Byte	00	R/W	318
0044	EMAC_BP_L	EMAC Boundary Pointer Low Byte	00	R/W	319
0045	EMAC_BP_H	EMAC Boundary Pointer High Byte	C0	R/W	319
0046	EMAC_BP_U	EMAC Boundary Pointer Upper Byte	FF	R/W	319
0047	EMAC_RHBP_L	EMAC Receive High Boundary Pointer Low Byte	00	R/W	320
0048	EMAC_RHBP_H	EMAC Receive High Boundary Pointer High Byte	00	R/W	321
0049	EMAC_RRP_L	EMAC Receive Read Pointer Low Byte	00	R/W	321
004A	EMAC_RRP_H	EMAC Receive Read Pointer High Byte	00	R/W	322
004B	EMAC_BUFSZ	EMAC Buffer Size Register	00	R/W	322
004C	EMAC_IEN	EMAC Interrupt Enable Register	00	R/W	323
004D	EMAC_ISTAT	EMAC Interrupt Status Register	00	R/W	325
004E	EMAC_PRSD_L	EMAC PHY Read Status Data Low Byte	00	R/W	326
004F	EMAC_PRSD_H	EMAC PHY Read Status Data High Byte	00	R/W	327
0050	EMAC_MIISTAT	EMAC MII Status Register	00	R/W	327
0051	EMAC_RWP_L	EMAC Receive Write Pointer Low Byte	00	R/W	328
0052	EMAC_RWP_H	EMAC Receive Write Pointer High Byte	00	R/W	329
0053	EMAC_TRP_L	EMAC Transmit Read Pointer Low Byte	00	R/W	329

Power-On Reset

A POR occurs every time the supply voltage to the part rises from below the Voltage Brownout threshold (V_{VBO}) to above the POR voltage threshold (V_{POR}). The internal bandgap-referenced voltage detector sends a continuous RESET signal to the Reset controller until the supply voltage (V_{CC}) exceeds the POR voltage threshold. After V_{CC} rises above V_{POR}, an on-chip analog delay element briefly maintains the RESET signal to the Reset controller. After this analog delay element times out, the Reset controller holds the eZ80F91 in RESET until the RESET mode timer expires. POR operation is displayed in Figure 3 The signals in Figure 3 are not drawn to scale but for displaying purposes only.

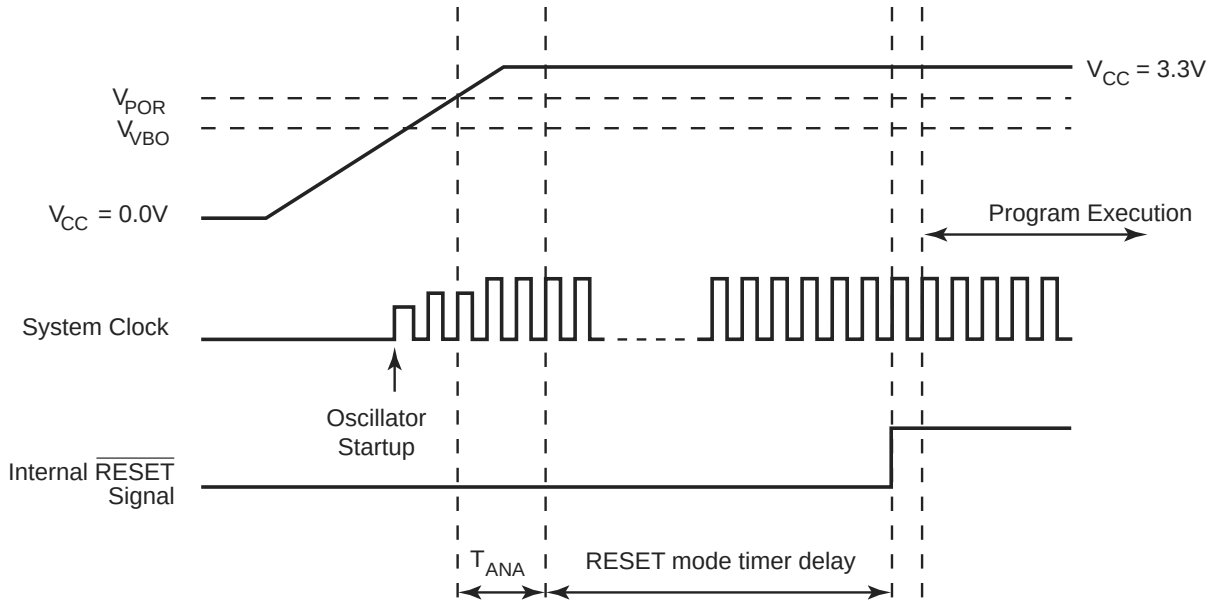

Figure 3. Power-On Reset Operation

Voltage Brownout Reset

If the supply voltage (V_{CC}) drops below the V_{VBO} after program execution begins, the eZ80F91 device resets. The VBO protection circuitry detects the low supply voltage and initiates a RESET via the Reset controller. The eZ80F91 remains in RESET until the supply voltage again returns above the POR voltage threshold (V_{POR}) and the Reset controller releases the internal RESET signal. The VBO circuitry rejects short negative brown-out pulses to prevent spurious RESET events.

VBO operation is displayed in Figure 4 on page 43. The signals in the figure are not drawn to scale but for illustration purposes only.

Table 14. Interrupt Priority Registers (INT_P0 = 0010h, INT_P1 = 0011h, INT_P2 = 0012h, INT_P3 = 0013h, INT_P4 = 0014h, INT_P5 = 0015h)

Bit	7	6	5	4	3	2	1	0
INT_P0 Reset	0	0	0	0	0	0	0	0
INT_P1 Reset	0	0	0	0	0	0*	0*	0
INT_P2 Reset	0	0	0	0	0	0	0	0
INT_P3 Reset	0	0	0	0	0	0	0	0
INT_P4 Reset	0	0	0	0	0	0	0	0
INT_P5 Reset	0	0	0	0	0	0	0	0
CPU Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: X = Undefined; R/W = Read/Write, *Unused.

Bit Position	Value	Description
7 INT_PX	0	Default Interrupt Priority
	1	Level One Interrupt Priority
6 INT_PX	0	Default Interrupt Priority
	1	Level One Interrupt Priority
5 INT_PX	0	Default Interrupt Priority
	1	Level One Interrupt Priority
4 INT_PX	0	Default Interrupt Priority
	1	Level One Interrupt Priority
3 INT_PX	0	Default Interrupt Priority
	1	Level One Interrupt Priority
2 INT_PX	0	Default Interrupt Priority
	1	Level One Interrupt Priority
1 INT_PX	0	Default Interrupt Priority
	1	Level One Interrupt Priority
0 INT_PX	0	Default Interrupt Priority
	1	Level One Interrupt Priority

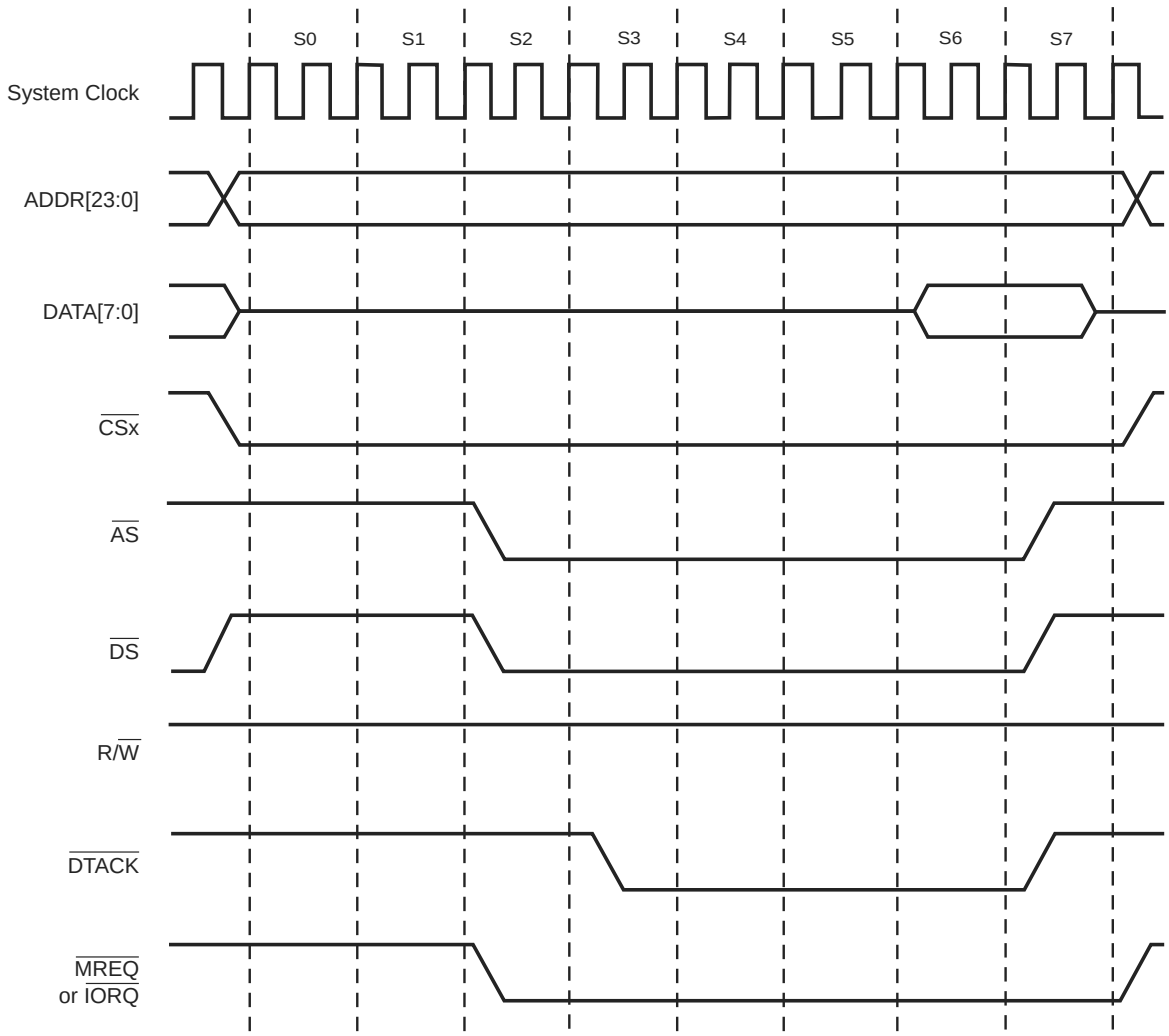

Figure 18. Example: Motorola Bus Mode Read Timing

MBIST Control

There are two Memory Built-In Self-Test (MBIST) controllers for the RAM blocks on the eZ80F91. MBIST_GPR is for General-Purpose RAM and MBIST_EMR is for EMAC RAM. Writing a 1 to MBIST_ON starts the MBIST testing. Writing a 0 to MBIST_ON stops the MBIST testing. On completion of the MBIST testing, MBIST_ON is automatically reset to 0. If RAM passes MBIST testing, MBIST_PASS is 1. The value in MBIST_PASS is only valid when MBIST_DONE is High. See Table 34.

Table 34. MBIST Control Register (MBIST_GPR=00B6h, MBIST_EMR=00B7h)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	R/W	R	R	R	R	R	R	R
Note: R/W = Read/Write; R = Read Only.								

Bit Position	Value	Description
7 MBIST_ON	0	MBIST Testing of the RAM is disabled.
	1	MBIST Testing of the RAM is enabled.
6 MBIST_DONE	0	MBIST Testing has not completed.
	1	MBIST Testing has completed.
5 MBIST_PASS	0	MBIST Testing has failed.
	1	MBIST Testing has passed.
[4:0]	00000	Reserved.

TMRx_RR_H and TMRx_RR_L. Downcounting continues on the next clock edge and the timer continues to count until disabled. An example of the timer operating in CONTINUOUS mode is displayed in Figure 28. Timer register information is listed in Table 51.

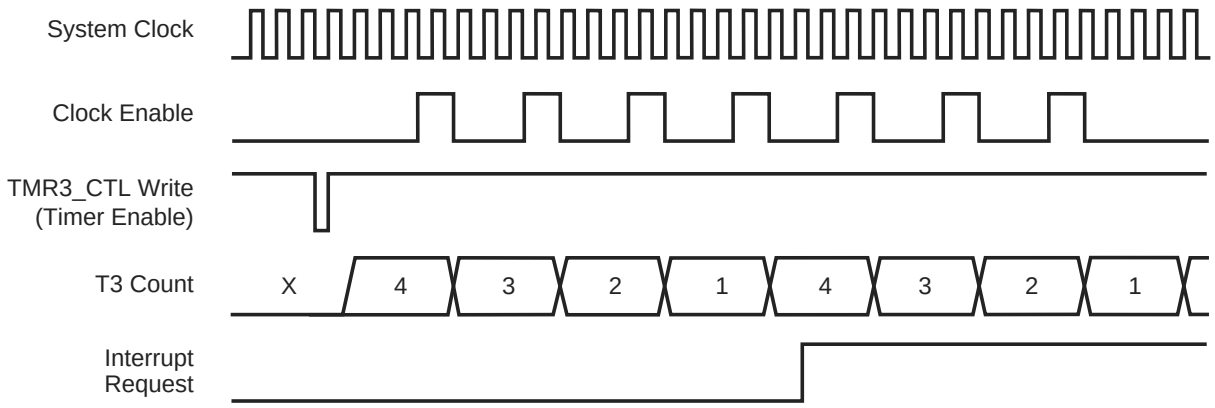

Figure 28. Example: PRT CONTINUOUS Mode Operation

Table 51. Example: PRT CONTINUOUS Mode Parameters

Parameter	Control Register(s)	Value
Timer Enable	TMRx_CTL[TIM_EN]	1
Reload	TMRx_CTL[RLD]	1
Prescaler Divider = 4	TMRx_CTL[CLK_DIV]	00b
CONTINUOUS Mode	TMRx_CTL[TIM_CONT]	1
End of Count Interrupt Enable	TMRx_IER[IRQ_EOC_EN]	1
Timer Reload Value	{TMRx_RR_H, TMRx_RR_L}	0004h

Timer Interrupts

The terminal count flag (TMRx_IIR[EOC]) is set to 1 whenever the timer reaches 0000h, its end-of-count value in SINGLE PASS mode, or when the timer reloads the start value in CONTINUOUS mode. The terminal count flag is only set when the timer reaches 0000h (or reloads) from 0001h. The timer interrupt flag is not set to 1 when the timer is loaded with the value 0000h, which selects the maximum time-out period.

The CPU is programmed to poll the EOC bit for time-out event. Alternatively, an interrupt service request signal is sent to the CPU by setting the TMRx_IER[EOC] bit to 1.

Timer Data Register High Byte

The Timerx Data Register—High Byte returns the High byte of the count value of the selected timer as it existed at the time that the Low byte was read. The Timer Data Register—High Byte (see Table 58) is read when the timer is in operation. Reading the current count value does not affect timer operation. To read the 16-bit data of the current count value, {TMRx_DR_H[7:0], TMRx_DR_L[7:0]}, first read the Timer Data Register—Low Byte followed by the Timer Data Register—High Byte. The Timer Data Register—High Byte value is latched into a temporary storage when a Read of the Timer Data Register—Low Byte occurs.

This register shares its address with the corresponding timer reload register.

Table 58. Timer Data Register High Byte (TMR0_DR_H = 0064h, TMR1_DR_H = 0069h, TMR2_DR_H = 0073h, TMR3_DR_H = 0078h)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	R	R	R	R	R	R	R	R

Note: R = Read only.

Bit Position	Value	Description
[7:0] TMR_DR_H	00h FFh	These bits represent the High byte of the 2-byte timer data value, {TMRx_DR_H[7:0], TMRx_DR_L[7:0]}. Bit 7 is bit 15 (msb) of the 16-bit timer data value. Bit 0 is bit 8 of the 16-bit timer data value.

Timer Input Capture Value A Register High Byte

The Timer x Input Capture Value A Register—High Byte (Table 63) stores the High byte of the capture value for external input FA. For Timer 1, the external input is IC0. For Timer 3, it is IC2.

Table 63. Timer Input Capture Value Register A High Byte (TMR1_CAPA_H = 006Ch, TMR3_CAPA_H = 007Dh)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	R	R	R	R	R	R	R	R

Note: R = Read only.

Bit Position	Value	Description
[7:0] TMRx_CAPA_H	00h FFh	These bits represent the High byte of the 2-byte capture value, {TMRx_CAPA_H[7:0], TMRx_CAPA_L[7:0]}. Bit 7 is bit 15 (msb) of the 16-bit data value. Bit 0 is bit 8 of the 16-bit timer data value.

Timer Input Capture Value B Register Low Byte

The Timer x Input Capture Value B Register—Low Byte (Table 64) stores the Low byte of the capture value for external input FB. For Timer 1, the external input is IC1. For Timer 3, it is IC3.

Table 64. Timer Input Capture Value Register B Low Byte (TMR1_CAPB_L = 006Dh, TMR3_CAPB_L = 007Eh)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	R	R	R	R	R	R	R	R

Note: R = Read only.

Bit Position	Value	Description
[7:0] TMRx_CAPB_L	00h FFh	These bits represent the Low byte of the 2-byte capture value, {TMRx_CAPB_H[7:0], TMRx_CAPB_L[7:0]}. Bit 7 is bit 7 of the 16-bit data value. Bit 0 is bit 0 (lsb) of the 16-bit timer data value.

Serial Peripheral Interface

The Serial Peripheral Interface (SPI) is a synchronous interface allowing several SPI-type devices to be interconnected. The SPI is a full-duplex, synchronous, character-oriented communication channel that employs a four-wire interface. The SPI block consists of a transmitter, receiver, baud rate generator, and control unit. During an SPI transfer, data is sent and received simultaneously by both the master and the slave SPI devices.

In a serial peripheral interface, separate signals are required for data and clock. The SPI is configured either as a master or as a slave. The connection of two SPI devices (one master and one slave) and the direction of data transfer is displayed in Figure 40 and Figure 41.

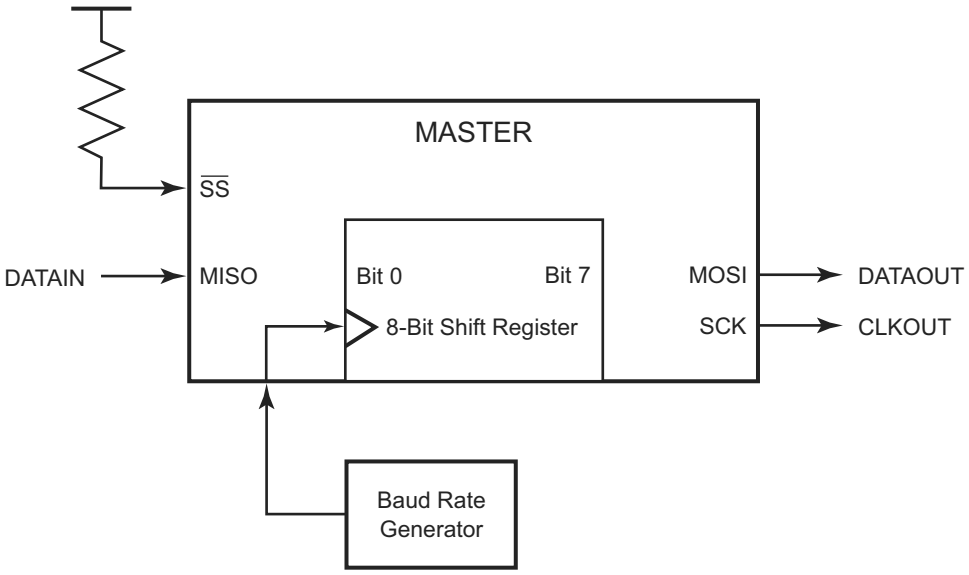

Figure 40. SPI Master Device

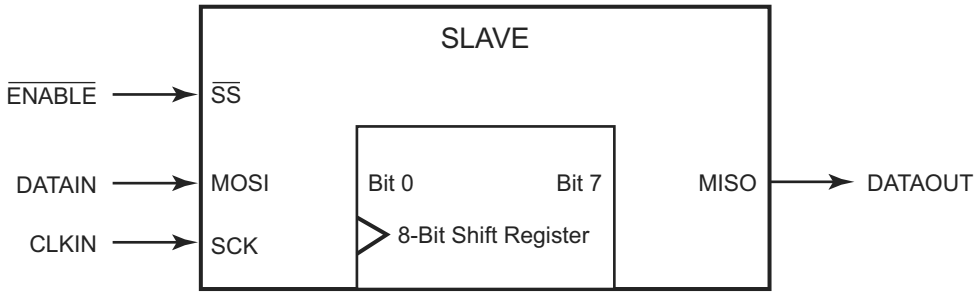

Figure 41. SPI Slave Device

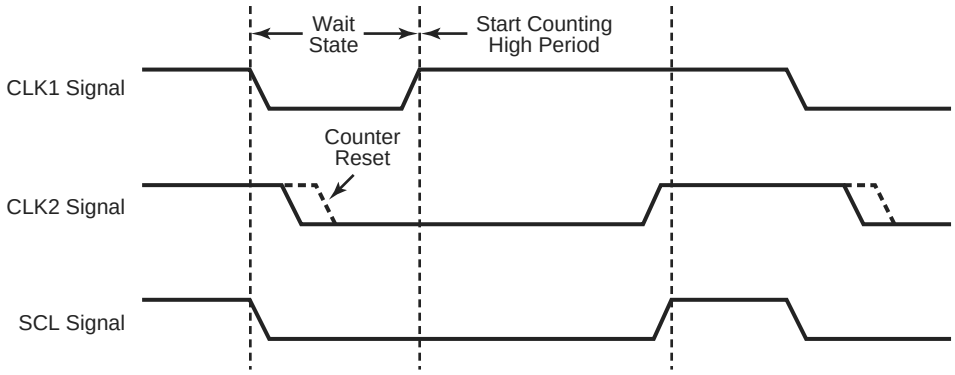

Figure 47. Clock Synchronization In I2C Protocol

Arbitration

Any master initiates a transfer if the bus is free. As a result, multiple masters each generates a START condition if the bus is free within a minimum period. If multiple masters generate a START condition, a START is defined for the bus. However, arbitration defines which MASTER controls the bus. Arbitration takes place on the SDA line. As mentioned, START conditions are initiated only while the SCL line is held High. If during this period, a master (M1) initiates a High-to-Low transition—that is, a START condition—while a second master (M2) transmits a Low signal on the line, then the first master, M1, cannot take control of the bus. As a result, the data output stage for M1 is disabled.

Arbitration continues for many bits. Its first stage is comparison of the address bits. If the masters are each trying to address the same device, arbitration continues with a comparison of the data. Because address and data information on the I2C bus is used for arbitration, no information is lost during this process. A master that loses the arbitration generates clock pulses until the end of the byte in which it loses the arbitration.

If a master also incorporates a slave function and it loses arbitration during the addressing stage, it is possible that the winning master is trying to address it. The losing master must switch over immediately to its slave receiver mode. Figure 47 displays the arbitration procedure for two masters. Of course, more masters can be involved, depending on how many masters are connected to the bus. The moment there is a difference between the internal data level of the master generating DATA 1 and the actual level on the SDA line, its data output is switched off, which means that a High output level is then connected to the bus. As a result, the data transfer initiated by the winning master is not affected. Because control of the I2C bus is decided solely on the address and data sent by competing masters, there is no central master, nor any order of priority on the bus.

Special attention must be paid if, during a serial transfer, the arbitration procedure is still in progress at the moment when a repeated START condition or a STOP condition is transmitted to the I2C bus. If it is possible for such a situation to occur, the masters involved

Bit Position	Value	Description
5 STA	0	Master mode START condition is sent.
	1	Master mode start-transmit START condition on the bus.
4 STP	0	Master mode STOP condition is sent.
	1	Master mode stop-transmit STOP condition on the bus.
3 IFLG	0	I^2C interrupt flag is not set.
	1	I^2C interrupt flag is set.
2 AAK	0	Not Acknowledge.
	1	Acknowledge.
[1:0]	00	Reserved.

I^2C Status Register

The I^2C_SR register is a Read Only register that contains a 5-bit status code in the five MSbs; the three LSbs are always 0. The Read Only I2C_SR registers share the same I/O addresses as the Write Only I2C_CCR registers. See Table 128.

Table 128. I^2C Status Registers (I2C_SR = 00CCh)

Bit	7	6	5	4	3	2	1	0
Reset	1	1	1	1	1	0	0	0
CPU Access	R	R	R	R	R	R	R	R

Note: R = Read only.

Bit Position	Value	Description
[7:3] STAT	00000 11111	5-bit I^2C status code.
[2:0]	000	Reserved.

There are 29 possible status codes, as listed in Table 129. When the I^2C_SR register contains the status code F8h, no relevant status information is available, no interrupt is generated, and the IFLG bit in the I^2C_CTL register is not set. All other status codes correspond to a defined state of the I^2C.

Table 133. ZDI Write Only Registers (Continued)

ZDI Address	ZDI Register Name	ZDI Register Function	Reset Value
08h	ZDI_ADDR2_L	Address Match 2 Low Byte	XXh
09h	ZDI_ADDR2_H	Address Match 2 High Byte	XXh
0Ah	ZDI_ADDR2_U	Address Match 2 Upper Byte	XXh
0Ch	ZDI_ADDR3_L	Address Match 3 Low Byte	XXh
0Dh	ZDI_ADDR3_H	Address Match 3 High Byte	XXh
0Eh	ZDI_ADDR3_U	Address Match 4 Upper Byte	XXh
10h	ZDI_BRK_CTL	Break Control Register	00h
11h	ZDI_MASTER_CTL	Master Control Register	00h
13h	ZDI_WR_DATA_L	Write Data Low Byte	XXh
14h	ZDI_WR_DATA_H	Write Data High Byte	XXh
15h	ZDI_WR_DATA_U	Write Data Upper Byte	XXh
16h	ZDI_RW_CTL	Read/Write Control Register	00h
17h	ZDI_BUS_CTL	Bus Control Register	00h
21h	ZDI_IS4	Instruction Store 4	XXh
22h	ZDI_IS3	Instruction Store 3	XXh
23h	ZDI_IS2	Instruction Store 2	XXh
24h	ZDI_IS1	Instruction Store 1	XXh
25h	ZDI_IS0	Instruction Store 0	XXh
30h	ZDI_WR_MEM	Write Memory Register	XXh

ZDI Read Only Registers

Table 134 lists the ZDI Read Only registers. Many of the ZDI Read Only addresses are shared with ZDI Write Only registers.

Table 134. ZDI Read Only Registers

ZDI Address	ZDI Register Name	ZDI Register Function	Reset Value
00h	ZDI_ID_L	eZ80fi Product ID Low Byte Register	08h
01h	ZDI_ID_H	eZ80 Product ID High Byte Register	00h
02h	ZDI_ID_REV	eZ80 Product ID Revision Register	XXh

Table 170. Opcode Map Second Opcode After 0EDh

Legend

Lower Nibble of 2nd Opcode

Upper Nibble of Second Opcode

4 SBC HL,BC

2

Mnemonic

First Operand

Second Operand

Lower Nibble (Hex)

Upper Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	IN0 B,(n)	OUT0 (n),B	LEA BC, IX+d	LEA BC, IY+d	TST A,B			LD BC, (HL)	IN0 C,(n)	OUT0 (n),C			TST A,C			LD (HL), BC
1	IN0 D,(n)	OUT0 (n),D	LEA DE, IX+d	LEA DE, IY+d	TST A,D			LD DE, (HL)	IN0 E,(n)	OUT0 (n),E			TST A,E			LD(HL), DE
2	IN0 H,(n)	OUT0 (n),H	LEA HL ,IX+d	LEA HL ,IY+d	TST A,H			LD HL, (HL)	IN0 L,(n)	OUT0 (n),L			TST A,L			LD (HL), HL
3		LD IY, (HL)	LEA IX ,IX+d	LEA IY ,IY+d	TST A,(HL)			LD IX, (HL)	IN0 A,(n)	OUT0 (n),A			TST A,A		LD (HL),IY	LD (HL), IX
4	IN B,(BC)	OUT (BC),B	SBC HL,BC	LD (Mmn), BC	NEG	RETN	IM 0	LD I,A	IN C,(C)	OUT (C),C	ADC HL,BC	LD BC, (Mmn)	MLT BC	RETI		LD R,A
5	IN D,(BC)	OUT (BC),D	SBC HL,DE	LD (Mmn), DE	LEA IX, IY+d	LEA IY, IX+d	IM 1	LD A,I	IN E,(C)	OUT (C),E	ADC HL,DE	LD DE, (Mmn)	MLT DE		IM 2	LD A,R
6	IBN H,(C)	OUT (BC),H	SBC HL,HL	LD (Mmn), HL	TST A,n	PEA IX+d	PEA IY+d	RRD	IN L,(C)	OUT (C),L	ADC HL,HL	LD HL, (Mmn)	MLT HL	LD MB,A	LD A,MB	RLD
7			SBC HL,SP	LD (Mmn), SP	TSTIO n		SLP		IN A,(C)	OUT (C),A	ADC HL,SP	LD SP, (Mmn)	MLT SP	STMIX	RSMIX	
8			INIM	OTIM	INI2						INDM	OTDM	IND2			
9			INIMR	OTIMR	INI2R						INDMR	OTDMR	IND2R			
A	LDI	CPI	INI	OUTI	OUTI2				LDD	CPD	IND	OUTD	OUTD2			
B	LDIR	CPIR	INIR	OTIR	OTI2R				LDDR	CPDR	INDR	OTDR	OTD2R			
C			INIRX	OTIRX				LD I,HL			INDRX	OTDRX				
D								LD HL,I								
E																
F																

Note: n = 8-bit data; Mmn = 16- or 24-bit addr or data; d = 8-bit two s-complement displacement.

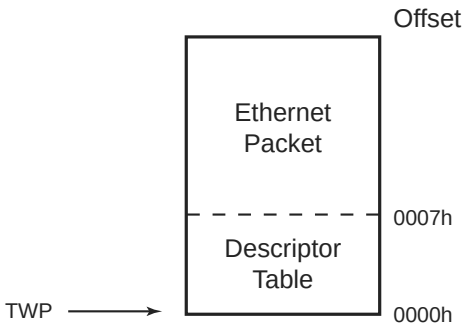

Figure 61. Descriptor Table

Note: For an official description of an Ethernet packet, refer to IEEE 802.3 specification, Figure 3-1.

The descriptor table contains three entries: the next pointer (NP), the packet size (Pkt_Size), and the packet status (Stat), as displayed in Figure 62.

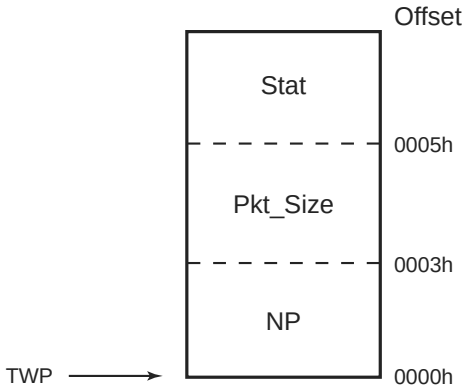

Figure 62. Descriptor Table Entries

NP is a 24-bit pointer to the start of the next packet. Pkt_Size contains the number of bytes of data in the Ethernet packet, including the four CRC bytes, but does not contain the seven descriptor table bytes. Stat contains the status of the packet. Stat differs for Transmit and Receive packets. See Table 178 on page 295 and Table 179 on page 295.

EMAC PHY Unit Select Address Register

The EMAC PHY Unit Select Address Register allows the selection of multiple connected external PHY devices. See Table 202.

Table 202. EMAC PHY Unit Select Address Register (EMAC_FIAD = 003Fh)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	R	R	R	R/W	R/W	R/W	R/W	R/W

Note: R = Read Only; R/W = Read/Write.

Bit Position	Value	Description
[7:5]	000	Reserved.
[4:0] FIAD	00h 1Fh	Programmable 5-bit value that selects an external PHY.

EMAC Transmit Polling Timer Register

This register sets the Transmit Polling Period in increments of TPTMR = SYSCLK ÷ 256. Whenever this register is written, the status of the Transmit Buffer Descriptor is checked to determine if the EMAC owns the Transmit Buffer. It then rechecks this status every TPTMR (calculated by TPTMR x EMAC_PTMR[7:0]). The Transmit Polling Timer is disabled if this register is set to 00h (which also disables the transmitting of packets). If a transmission is in progress when EMAC_PTMR is set to 00h, the transmission will complete. See Table 203.

Table 203. EMAC Transmit Polling Timer Register (EMAC_PTMR = 0040h)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: R/W = Read/Write.

Bit Position	Value	Description
[7:0] EMAC_PTMR	00h FFh	The Transmit polling period.

Table 218. EMAC PHY Read Status Data Register High Byte (EMAC_PRSD_H = 004Fh)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	R	R	R	R	R	R	R	R

Note: R = Read Only.

Bit Position	Value	Description
[7:0] EMAC_PRSD_H	00h FFh	These bits represent the High byte of the 2-byte EMAC PHY Read Status Data value, {EMAC_PRSD_H, EMAC_PRSD_L}. Bit 7 is bit 15 (msb) of the 16-bit value. Bit 0 is bit 8 of the 16-bit value.

EMAC MII Status Register

The EMAC MII Status Register is used to determine the current state of the external PHY device. See Table 219.

Table 219. EMAC MII Status Register (EMAC_MIISTAT = 0050h)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	R	R	R	R	R	R	R	R

Note: R = Read Only.

Bit Position	Value	Description
7 BUSY	1	MII management operation in progress Busy. This status bit goes busy whenever the LCTLD (PHY Write) or the RSTAT (PHY Read) is set in the EMAC_MIIMGT register. It is negated when the Write or Read operation to the PHY has completed. In SCAN mode, the BUSY will be asserted until the SCAN is disabled. Use the EmacIStat[MGTDONE] interrupt status bit to determine when the data is valid.
	0	Not Busy.
6 MIILF	1	Local copy of PHY Link fail bit.
	0	PHY Link OK.

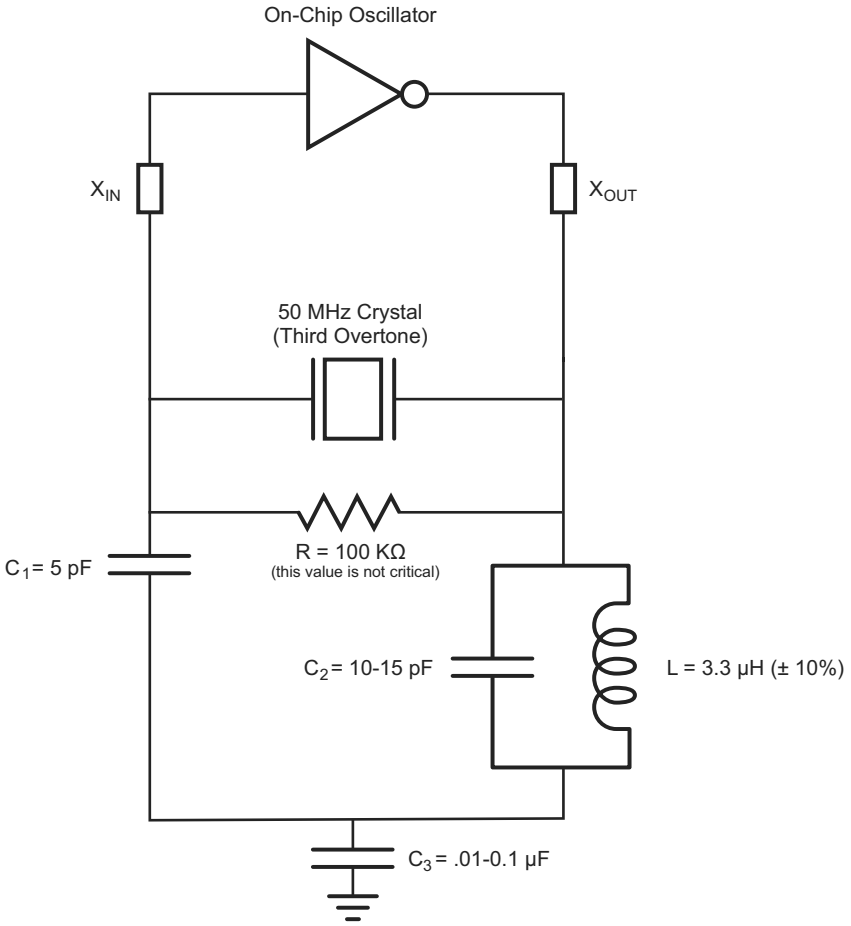

Figure 63. Recommended Crystal Oscillator Configuration 50 MHz Operation

Table 229. Recommended Crystal Oscillator Specifications 1 MHz Operation

Parameter	Frequency Dependent Value	Units	Comments
Frequency	1	MHz	
Resonance	Parallel		
Mode	Fundamental		
Series Resistance (R_S)	750	Ohms	Maximum
Load Capacitance (C_L)	13	pF	Maximum

Table 229. Recommended Crystal Oscillator Specifications 1 MHz Operation (Continued)

Parameter	Frequency Dependent Value	Units	Comments
Shunt Capacitance (C_0)	7	pF	Maximum
Drive Level	1	mW	Maximum

Table 230. Recommended Crystal Oscillator Specifications 10 MHz Operation

Parameter	Frequency Dependent Value	Units	Comments
Frequency	10	MHz	
Resonance	Parallel		
Mode	Fundamental		
Series Resistance (R_S)	35	Ohms	Maximum
Load Capacitance (C_L)	30	pF	Maximum
Shunt Capacitance (C_0)	7	pF	Maximum
Drive Level	1	mW	Maximum

32 kHz Real-Time Clock Crystal Oscillator Operation

Figure 64 on page 338 displays a recommended configuration for connecting the Real-Time Clock oscillator with an external 32 kHz fundamental mode, parallel-resonant crystal. The recommended crystal specifications are provided in Table 231 on page 338. A printed circuit board layout must not add more than 4 pF of stray capacitance to either the RTC_X_{IN} or RTC_X_{OUT} pins. If oscillation does not occur, reduce the values of capacitors C_1 and C_2 to decrease loading.

An on-chip MOS resistor sets the crystal drive current limit. This configuration does not require an external bias resistor across the crystal. An on-chip MOS resistor provides the biasing.

Table 234. POR and VBO Electrical Characteristics

		T_A = 40 ”C to 105 ”C				
Symbol	Parameter	Minimum	Typ	Maximum	Unit	Conditions
V_{VBO}	VBO Voltage Threshold	2.45	2.65	2.90	V	$V_{CC} = V_{VBO}$
V_{POR}	POR Voltage Threshold	2.55	2.75	2.95	V	$V_{CC} = V_{POR}$
V_{HYST}	POR/VBO Hysteresis	30	100	120	mV	
T_{ANA}	POR/VBO analog RESET duration	40		100	µs	
T_{VBO_MIN}	VBO pulse reject period		10		µs	
I_{POR_VBO}	POR/VBO DC current consumption		40	50	µA	
IS_{POR_VBO}	POR/VBO DC SLEEP mode current consumption		120	150	µA	VBO_OFF=0 (VBO enabled)
VCC_{RAMP}	V_{CC} ramp rate requirements to guarantee proper RESET occurs	0.1		100	V/ms	

Flash Memory Characteristics

Table 235 lists the Flash memory characteristics of the eZ80F91 device. For Flash programming and erase timing information, see Flash Memory on page 97.

Table 235. Flash Memory Electrical Characteristics and Timing

	V_{DD} = 3.0 V to 3.6 V; T_A = 40 ”C to 105 ”C				
Symbol	Minimum	Typical	Maximum	Units	Notes
Flash Byte Read Cycle Time	78			ns	

Current Consumption Under Various Operating Conditions

Figure 65 on page 342 displays the typical current consumption of the eZ80F91 device versus Vdd while operating at 25 ºC, with zero Wait states, and with either a 10 MHz, 20 MHz, or 50 MHz system clock.