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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	eZ80
Core Size	8-Bit
Speed	50MHz
Connectivity	Ethernet, I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	32
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/ez80f91az050ec

Table 2. Pin Identification on the eZ80F91 Device (Continued)

LQFP Pin No	BGA Pin No	Symbol	Function	Signal Direction	Description
17	F1	ADDR12	Address Bus	Bidirectional	Configured as an output in normal operation. The address bus selects a location in memory or I/O space to be read or written. Configured as an input during bus acknowledge cycles. Drives the Chip Select/Wait State Generator block to generate Chip Selects.
18	F2	ADDR13	Address Bus	Bidirectional	
19	F3	ADDR14	Address Bus	Bidirectional	
20	F4	ADDR15	Address Bus	Bidirectional	
21	G1	ADDR16	Address Bus	Bidirectional	
22	G2	V_{DD}	Power Supply		Power Supply.
23	G3	V_{SS}	Ground		Ground.
24	F5	ADDR17	Address Bus	Bidirectional	Configured as an output in normal operation. The address bus selects a location in memory or I/O space to be read or written. Configured as an input during bus acknowledge cycles. Drives the Chip Select/Wait State Generator block to generate Chip Selects.
25	H1	ADDR18	Address Bus	Bidirectional	
26	H2	ADDR19	Address Bus	Bidirectional	
27	G4	ADDR20	Address Bus	Bidirectional	
28	H3	ADDR21	Address Bus	Bidirectional	
29	J1	ADDR22	Address Bus	Bidirectional	
30	G5	ADDR23	Address Bus	Bidirectional	
31	J2	V_{DD}	Power Supply		Power Supply.
32	H4	V_{SS}	Ground		Ground.
33	J3	CS0	Chip Select 0	Output, Active Low	$\overline{CS0}$ Low indicates that an access is occurring in the defined $\overline{CS0}$ memory or I/O address space.
34	K1	CS1	Chip Select 1	Output, Active Low	$\overline{CS1}$ Low indicates that an access is occurring in the defined $\overline{CS1}$ memory or I/O address space.
35	K2	CS2	Chip Select 2	Output, Active Low	$\overline{CS2}$ Low indicates that an access is occurring in the defined $\overline{CS2}$ memory or I/O address space.
36	L1	CS3	Chip Select 3	Output, Active Low	$\overline{CS3}$ Low indicates that an access is occurring in the defined $\overline{CS3}$ memory or I/O address space.
37	M1	V_{DD}	Power Supply		Power Supply.
38	M2	V_{SS}	Ground		Ground.

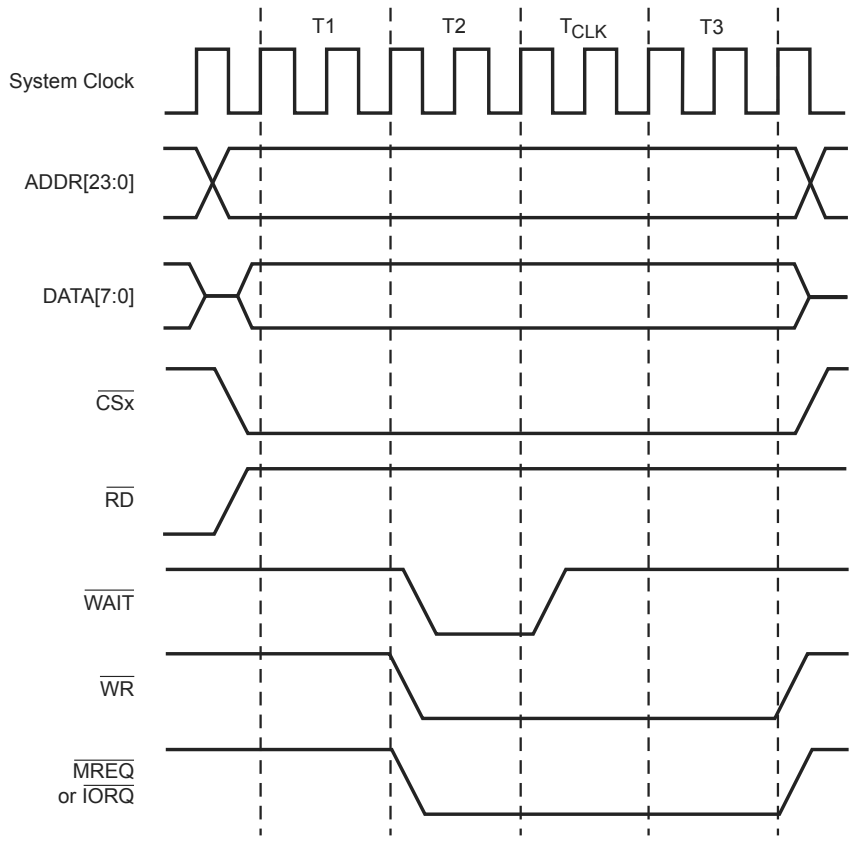

Figure 11. Example: Z80® Bus Mode Write Timing

Intel Bus Mode

Chip selects configured for Intel bus mode modify the CPU bus signals to duplicate a four-state memory transfer similar to that found on Intel-style microcontrollers. The bus signals and eZ80F91 pins are mapped as displayed in Figure 12 on page 74. In Intel bus mode, you select either multiplexed or nonmultiplexed address and data buses. In nonmultiplexed operation, the address and data buses are separate. In multiplexed operation, the lower byte of the address, ADDR[7:0], also appears on the data bus, DATA[7:0], during State T1 of the Intel bus mode cycle.

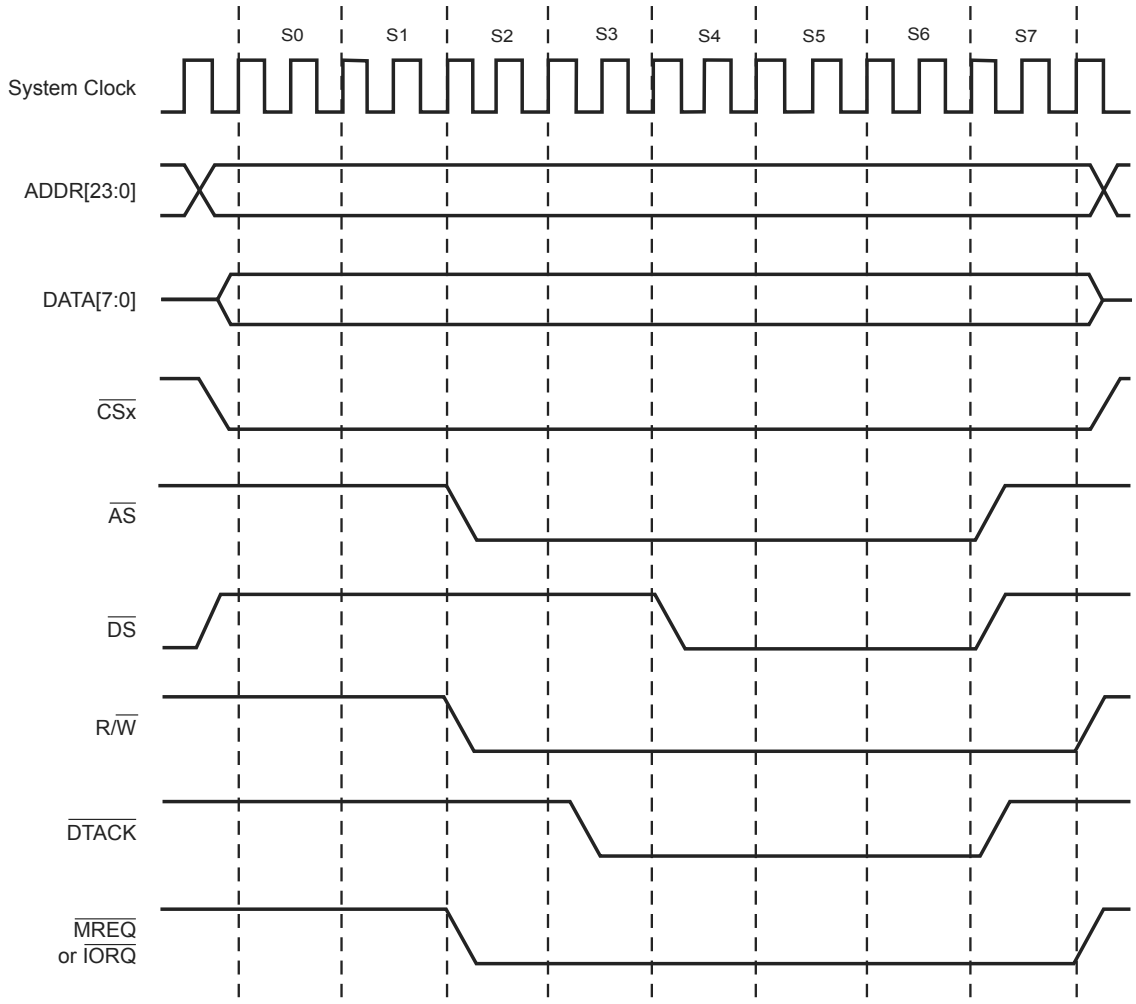

Figure 19. Example: Motorola Bus Mode Write Timing

Switching Between Bus Modes

When switching bus modes between Intel™ to Motorola, Motorola to Intel™, eZ80® to Motorola, or eZ80 to Intel™, there is one extra SCLK cycle added to the bus access. An extra clock cycle is not required for repeated access in any of the bus modes (for example, Intel™ to Intel™). An extra clock cycle is not required for Intel™ (or Motorola) to eZ80 bus mode (under normal operation). The extra clock cycle is not shown in the timing examples. Due to the asynchronous nature of these bus protocols, the extra delay does not impact peripheral communication.

Bit Position	Value	Description
[1] BLK1_PROT	0	Disable Write/Erase Protect on block 08000h to 0FFFFh.
	1	Enable Write/Erase Protect on block 08000h to 0FFFFh.
[0] BLK0_PROT	0	Disable Write/Erase Protect on block 00000h to 07FFFh.
	1	Enable Write/Erase Protect on block 00000h to 07FFFh.

Note: The lower 32 KB block (00000h to 07FFFh—BLK0) is called the Boot block and is protected using the external $\overline{WP}$ pin.

Flash Interrupt Control Register

There are two sources of interrupts from the Flash controller. These two sources are:

- Page Erase, Mass Erase, or Row Program completed successfully.
- An error condition occurred.

Either or both of these two interrupt sources are enabled by setting the appropriate bits in the Flash Interrupt Control register.

The Flash Interrupt Control register contains four status bits to indicate the following error conditions:

Row Program Time-Out—This bit signals a time-out during Row Programming. If the current row program operation does not complete within 4864 Flash controller clocks, the Flash controller terminates the row program operation by clearing bit 2 of the Flash Program Control Register and sets the RP_TM0 error bit to 1.

Write Violation—This bit indicates an attempt to write to a protected block of Flash memory (the Write was not performed).

Page Erase Violation—This bit indicates an attempt to erase a protected block of Flash memory (the requested page was not erased).

Mass Erase Violation—This bit indicates an attempt to MASS ERASE when there are one or more protected blocks in Flash memory (the MASS ERASE was not performed).

If the error condition interrupt is enabled, any of these four error conditions result in an interrupt request being sent to the eZ80F91device's interrupt controller. Reading the Flash Interrupt Control register clears all error condition flags and the DONE flag. See Table 42 on page 109.

  - TMR3_OC_CTL2
- Compare Value Registers
  - TMR3_OC3_H
  - TMR3_OC3_L
  - TMR3_OC2_H
  - TMR3_OC2_L
  - TMR3_OC1_H
  - TMR3_OC1_L
  - TMR3_OC0_H
  - TMR3_OC0_L

Multiple PWM mode uses the following 19 registers:

- PWM Control Registers
  - TMR3_PWM_CTL1
  - TMR3_PWM_CTL2
  - TMR3_PWM_CTL3
- PWM Rising Edge Values
  - TMR3_PWM3R_H
  - TMR3_PWM3R_L
  - TMR3_PWM2R_H
  - TMR3_PWM2R_L
  - TMR3_PWM1R_H
  - TMR*x*_PWM1R_L
  - TMR3_PWM0R_H
  - TMR3_PWM0R_L
- PWM Falling Edge Values
  - TMR3_PWM3F_H
  - TMR*x*_PWM3F_L
  - TMR3_PWM2F_H
  - TMR3_PWM2F_L
  - TMR3_PWM1F_H
  - TMR3_PWM1F_L
  - TMR3_PWM0F_H
  - TMR3_PWM0F_L

Pulse-Width Modulation Falling Edge—Low Byte

A parallel 16-bit Write of {TMR3_PWMxF_H[7–0], TMR3_PWMxF_L[7–0]} occurs when software initiates a Write to TMR3_PWMxF_L. The register is listed in Table 78.

Table 78. PWMx Falling-Edge Register—Low Byte (TMR3_PWM0F_L = 0084h, TMR3_PWM1F_L = 0086h, TMR3_PWM2F_L = 0088h, TMR3_PWM3F_L = 008Ah)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: R/W = Read/Write.

Bit Position	Value	Description
[7:0] PWMXF_L	00h–FFh	These bits represent the Low byte of the 16-bit value to set the falling edge COMPARE value for PWMx, {TMR3_PWMXF_H[7:0], TMR3_PWMXF_L[7:0]}. Bit 7 is bit 7 of the 16-bit timer data value. Bit 0 is bit 0 (lsb) of the 16-bit timer data value.

Pulse-Width Modulation Falling Edge—High Byte

Writing to TMR3_PWMxF_H stores the value in a temporary holding register. A parallel 16-bit Write of {TMR3_PWMxF_H[7–0], TMR3_PWMxF_L[7–0]} occurs when software initiates a Write to TMR3_PWMxF_L. The register is listed in Table 79.

Table 79. PWMx Falling-Edge Register—High Byte (TMR3_PWM0F_H = 0085h, TMR3_PWM1F_H = 0087h, TMR3_PWM2F_H = 0089h, TMR3_PWM3F_H = 008Bh)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: R/W = Read/Write.

Bit Position	Value	Description
[7:0] PWMXF_H	00h–FFh	These bits represent the High byte of the 16-bit value to set the falling edge COMPARE value for PWMx, {TMR3_PWMXF_H[7:0], TMR3_PWMXF_L[7:0]}. Bit 7 is bit 15 (msb) of the 16-bit timer data value. Bit 0 is bit 8 of the 16-bit timer data value.

- Write values to the RTC count registers to set the current time
- Write values to the RTC alarm registers to set the appropriate alarm conditions
- Write to RTC_CTRL to clear RTC_UNLOCK; clearing the RTC_UNLOCK bit resets and enables the clock divider

Real-Time Clock Registers

The RTC registers are accessed via the address and data buses using I/O instructions. The RTC_UNLOCK control bit controls access to the RTC count registers. When unlocked (RTC_UNLOCK = 1), the RTC count is disabled and the count registers are Read/Write. When locked (RTC_UNLOCK = 0), the RTC count is enabled and the count registers are Read Only. The default at RESET is for the RTC to be locked.

Real-Time Clock Seconds Register

This register contains the current seconds count. The value in the RTC_SEC register is unchanged by a RESET. The current setting of BCD_EN determines whether the values in this register are binary (BCD_EN = 0) or binary-coded decimal (BCD_EN = 1). Access to this register is Read Only if the RTC is locked, and Read/Write if the RTC is unlocked. See Table 80.

Table 80. Real-Time Clock Seconds Register (RTC_SEC = 00E0h)

Bit	7	6	5	4	3	2	1	0
Reset	X	X	X	X	X	X	X	X
CPU Access	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*

Note: X = Unchanged by RESET; R/W* = Read Only if RTC locked, Read/Write if RTC unlocked.

Binary-Coded-Decimal Operation (BCD_EN = 1)		
Bit Position	**Value**	**Description**
[7:4] TEN_SEC	0–5	The tens digit of the current seconds count.
[3:0] SEC	0–9	The ones digit of the current seconds count.
Binary Operation (BCD_EN = 0)		
Bit Position	**Value**	**Description**
[7:0] SEC	00h–3Bh	The current seconds count.

Real-Time Clock Day-of-the-Week Register

This register contains the current day-of-the-week count. The RTC_DOW register begins counting at 01h. The value in the RTC_DOW register is unchanged by a RESET. The current setting of BCD_EN determines whether the value in this register is binary (BCD_EN = 0) or binary-coded decimal (BCD_EN = 1). Access to this register is Read Only if the RTC is locked and Read/Write if the RTC is unlocked. See Table 83.

Table 83. Real-Time Clock Day-of-the-Week Register (RTC_DOW = 00E3h)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	X	X	X	X
CPU Access	R	R	R	R	R/W*	R/W*	R/W*	R/W*

Note: X = Unchanged by RESET; R = Read Only; R/W* = Read Only if RTC locked, Read/Write if RTC unlocked.

Binary-Coded Decimal Operation (BCD_EN = 1)		
Bit Position	**Value**	**Description**
[7:4]	0000	Reserved.
[3:0] DOW	1–7	The current day-of-the-week.count.

Binary Operation (BCD_EN = 0)		
Bit Position	**Value**	**Description**
[7:4]	0000	Reserved.
[3:0] DOW	01h–07h	The current day-of-the-week count.

Real-Time Clock Day-of-the-Month Register

This register contains the current day-of-the-month count. The RTC_DOM register begins counting at 01h. The value in the RTC_DOM register is unchanged by a RESET. The current setting of BCD_EN determines whether the values in this register are binary (BCD_EN = 0) or binary-coded decimal (BCD_EN = 1). Access to this register is Read Only if the RTC is locked, and Read/Write if the RTC is unlocked. See Table 84.

Table 84. Real-Time Clock Day-of-the-Month Register (RTC_DOM = 00E4h)

Bit	7	6	5	4	3	2	1	0
Reset	X	X	X	X	X	X	X	X
CPU Access	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*

Note: X = Unchanged by RESET; R/W* = Read Only if RTC locked, Read/Write if RTC unlocked.

Binary-Coded Decimal Operation (BCD_EN = 1)

Bit Position	Value	Description
[7:4] TENS_DOM	0–3	The tens digit of the current day-of-the-month count.
[3:0] DOM	0–9	The ones digit of the current day-of-the-month count.

Binary Operation (BCD_EN = 0)

Bit Position	Value	Description
[7:0] DOM	01h–1Fh	The current day-of-the-month count.

Bit Position	Value	Description
4 EPS	0	Even Parity Select. Use odd parity for transmit and receive. The total number of 1 bits in the transmit data plus parity bit is odd. Used as SPACE bit in Multidrop Mode. See Table 104 on page 189 for parity select definitions. Note: Receive Parity is set to SPACE in multidrop mode.
	1	Use even parity for transmit and receive. The total number of 1 bits in the transmit data plus parity bit is even. Used as MARK bit in Multidrop Mode. See Table 104 on page 189 for parity select definitions.
3 PEN	0	Parity bit transmit and receive is disabled.
	1	Parity bit transmit and receive is enabled. For transmit, a parity bit is generated and transmitted with every data character. For receive, the parity is checked for every incoming data character. In Multidrop Mode, receive parity is checked for space parity.
[2:0] CHAR	000–111	UART Character Parameter Selection. See Table 103 on page 189 for a description of the values.

Table 103. UART Character Parameter Definition

CHAR[2:0]	Character Length (Tx/Rx Data Bits)	Stop Bits (Tx Stop Bits)
000	5	1
001	6	1
010	7	1
011	8	1
100	5	2
101	6	2
110	7	2
111	8	2

IrDA specifications. The UART must be enabled to use the endec. For more information on the UART and its BRG, see Universal Asynchronous Receiver/Transmitter on page 175.

Transmit

The data to be transmitted via the IR transceiver is the data sent to UART0. The UART transmit signal, TxD, and Baud Rate Clock are used by the endec to generate the modulation signal, IR_TxD, that drives the infrared transceiver. Each UART bit is 16 clocks wide. If the data to be transmitted is a logical 1 (High), the IR_TxD signal remains Low (0) for the full 16-clock period. If the data to be transmitted is a logical 0, a 3-clock High (1) pulse is output following a 7-clock Low (0) period. Following the 3-clock High pulse, a 6-clock Low pulse completes the full 16-clock data period. Data transmission is displayed in Figure 38. During data transmission, the IR receive function must be disabled by clearing the IR_RxEN bit in the IR_CTL reg to 0 to prevent transmitter-to-receiver crosstalk.

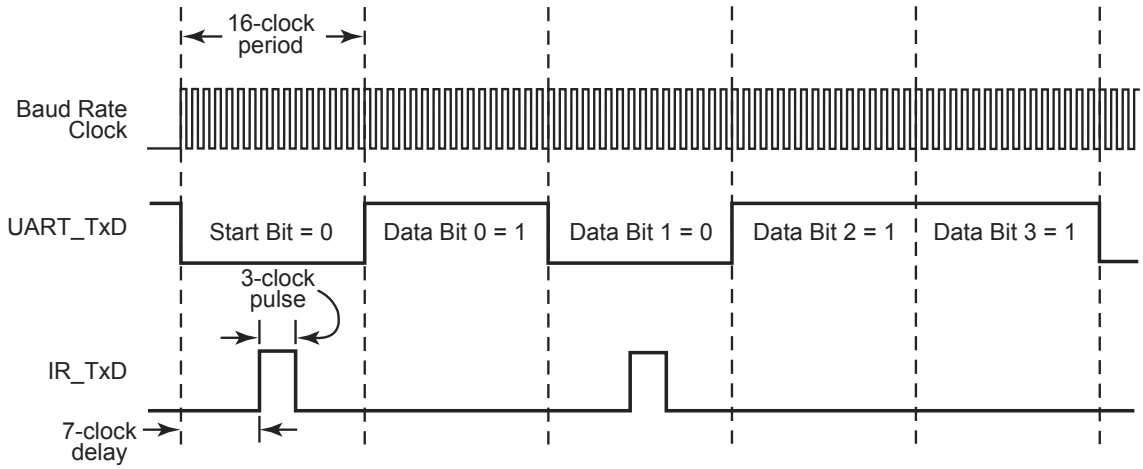

Figure 38. Infrared Data Transmission

Receive

Data received from the IR transceiver via the IR_RxD signal is decoded by the endec and passed to the UART. The IR_RxEN bit in the IR_CTL register must be set to enable the receiver decoder. The IrDA serial infrared (SIR) data format uses half duplex communication. Therefore, the UART must not be allowed to transmit while the receiver decoder is enabled. The UART Baud Rate Clock is used by the endec to generate the demodulated signal, RxD, that drives the UART. Each UART bit is 16 clocks wide. If the data to be received is a logical 1 (High), the IR_RxD signal remains High (1) for the full 16-clock

Table 112. SPI Baud Rate Generator Register—Low Byte (SPI_BRG_L = 00B8h)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	1	0
CPU Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: R/W = Read/Write.

Bit Position	Value	Description
[7:0] SPI_BRG_L	00h–FFh	These bits represent the Low byte of the 16-bit BRG divider value. The complete BRG divisor value is returned by {SPI_BRG_H, SPI_BRG_L}.

Table 113. SPI Baud Rate Generator Register—High Byte (SPI_BRG_H = 00B9h)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: R/W = Read/Write.

Bit Position	Value	Description
[7:0] SPI_BRG_H	00h–FFh	These bits represent the High byte of the 16-bit BRG divider value. The complete BRG divisor value is returned by {SPI_BRG_H, SPI_BRG_L}.

Bit Position	Value	Description
2 ign_low_1	0	The *Ignore the Low Byte* function of the ZDI Address Match 1 registers is disabled. If brk_addr1 is set to 1, ZDI initiates a break when the entire 24-bit address, ADDR[23:0], matches the 3-byte value {ZDI_ADDR1_U, ZDI_ADDR1_H, ZDI_ADDR1_L}.
	1	The *Ignore the Low Byte* function of the ZDI Address Match 1 registers is enabled. If brk_addr1 is set to 1, ZDI initiates a break when only the upper 2 bytes of the 24-bit address, ADDR[23:8], match the 2-byte value {ZDI_ADDR1_U, ZDI_ADDR1_H}. As a result, a break occurs anywhere within a 256-byte page.
1 ign_low_0	0	The *Ignore the Low Byte* function of the ZDI Address Match 1 registers is disabled. If brk_addr0 is set to 1, ZDI initiates a break when the entire 24-bit address, ADDR[23:0], matches the 3-byte value {ZDI_ADDR0_U, ZDI_ADDR0_H, ZDI_ADDR0_L}.
	1	The *Ignore the Low Byte* function of the ZDI Address Match 1 registers is enabled. If the brk_addr1 is set to 0, ZDI initiates a break when only the upper 2 bytes of the 24-bit address, ADDR[23:8], match the 2 bytes value {ZDI_ADDR0_U, ZDI_ADDR0_H}. As a result, a break occurs anywhere within a 256-byte page.
0 single_step	0	ZDI single step mode is disabled.
	1	ZDI single step mode is enabled. ZDI asserts a break following execution of each instruction.

Table 156. PLL Characteristics (Continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
F_{vco}	VCO frequency	Recommended operating conditions		50		MHz
G_{vco}	VCO Gain	Recommended operating conditions	36		120	MHz/V
D1	SCLK Duty Cycle from PLL or XTALOSC source	Recommended operating conditions	45	50	55	%
T1A	PLL Clock Jitter	F_{VCO} = 50 MHz. XTALOSC = 10 MHz		350	500	ps
Lock2	PLL Lock-Time	F_{VCO} = 50 MHz. XTALOSC = 3.579 MHz C_{pll1} = 220 pF, R_{pll} = 499 ¾, C_{pll2} = 0.056 µF				s
I_{oH1} (XTL)	High-level Output Current for XTAL2 pin	$V_{oH} = V_{DD}$–0.4 V PLL_CTL0[5:4] = 01	–0.3			mA
I_{oL1} (XTL)	Low-level Output Current for XTAL2 pin	V_{oL} = 0.4 V PLL_CTL0[5:4] = 01	0.6			mA
I_{oH2} (XTL)	High-level Output Current for XTAL2 pin	$V_{oH} = V_{DD}$–0.4 V PLL_CTL0[5:4] = 11				mA
I_{oL2} (XTL)	Low-level Output Current for XTAL2 pin	V_{oL} = 0.4 V PLL_CTL0[5:4] = 11				mA
V_{PP3M} (XTL)	Peak-to-peak voltage under oscillator conditions for XTAL2 pin	F_{OSC} = 3.579 MHz Cx1 = 10 pF Cx2 = 10 pF				V
V_{PP10M} (XTL)	Peak-to-peak voltage under oscillator conditions for XTAL2 pin	F_{OSC} = 10 MHz Cx1 = 10 pF Cx2 = 10 pF				V
C_{xtal1} (package type)	Capacitance measured from XTAL1 pin to GND	T = 25 ºC				pF
C_{xtal2} (package type)	Capacitance measured from XTAL2 pin to GND	T = 25 ºC				pF
C_{loop} (package type)	Capacitance measured from loop filter pin to GND	T = 25 ºC				pF

- Receive High Boundary Pointer (RHBP)—this register points to the end of the Receive buffer + 1.

Figure 60 displays the internal Ethernet shared memory.

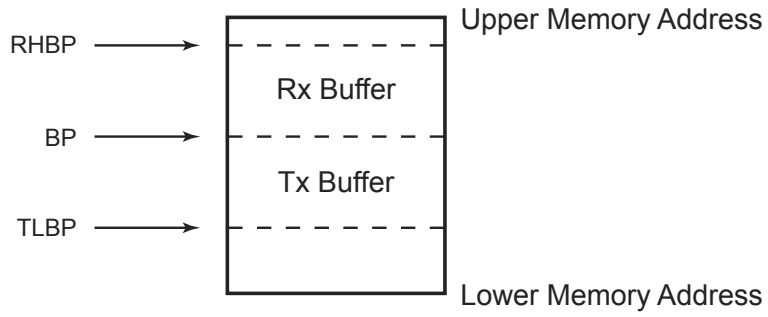

Figure 60. Internal Ethernet Shared Memory

The Transmit and Receive buffers are subdivided into packet buffers of 32, 64, 128, or 256 bytes in size. The packet buffer size is set in bits 7 and 6 of the EmacBufSize register. An Ethernet packet accommodate multiple packet buffers. First, however, a brief listing of the contents of a typical Ethernet packet is in order. See Table 177.

Table 177. Ethernet Packet Contents

Byte Range	Contents
Bytes 0–5	MAC destination address.
Bytes 6–11	MAC source address.
Bytes 12–13	Length/Type field.
Bytes 14–n	MAC Client Data.
Bytes (n+1)–(n+4)	Frame Check Sequence.

At the start of each packet is a descriptor table that describes the packet. Each actual Ethernet packet follows the descriptor table as displayed in Figure 61 on page 294.

EMAC Configuration Register 1

The EMAC Configuration Register 1 allows control of the padding, autodetection, cyclic redundancy checking (CRC) control, full-duplex, field length checking, maximum packet ignores, and proprietary header options. See Table 181.

Table 181. EMAC Configuration Register 1 (EMAC_CFG1 = 0021h)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: R/W = Read/Write.

Bit Position	Value	Description
7 PADEN	0	No padding. Assume all frames presented to EMAC have proper length.
	1	EMAC pads all short frames by adding zeroes to the end of the data field. This bit is used in conjunction with ADPADN and VLPAD.
6 ADPADN	0	Disable autodetection.
	1	Enable frame detection by comparing the two bytes following the source address with 0x8100 (VLAN Protocol ID) and pad accordingly. This bit is ignored if PADEN is cleared to 0.
5 VLPAD	0	Do not pad all short frames.
	1	EMAC pads all short frames to 64 bytes and append a valid CRC. This bit is ignored if PADEN is cleared to 0.
4 CRCEN	0	Do not append CRC.
	1	Append CRC to every frame regardless of padding options.
3 FULLD	0	HALF-DUPLEX mode. CSMA/CD is enabled.
	1	Enable FULL-DUPLEX mode. CSMA/CD is disabled.
2 FLCHK	0	Ignore the length field within Transmit/Receive frames.
	1	Both Transmit and Receive frame lengths are compared to the length/type field. If the length/type field represents a length then the frame length check is performed.
1 HUGEN	0	Limit the Receive frame-size to the number of bytes specified in the MAXF[15:0] field.
	1	Allow unlimited sized frames to be received. Ignore the MAXF[15:0] field.

Table 190. EMAC_IPGT Non-Back-to-Back Settings for Full- /Half-Duplex Modes

MII, RMII/SMII, PMD (100 Mbps)		MII, RMII/SMII (10 Mbps)		ENDEC Mode (10 Mbps)	
Clock Period = 40 ns		Clock Period = 400 ns		Clock Period = 100 ns	
IPGR2[6:0]	Interpacket Gap	IPGR2[6:0]	Interpacket Gap	IPGR2[6:0]	Interpacket Gap
00h	0.24 µs	00h	2.4 µs	00h	0.6 µs
10h	0.88 µs	10h	8.8 µs	10h	2.2 µs
*12h	0.96 µs	12h	9.6 µs	20h	3.8 µs
20h	1.52 µs	20h	15.2 µs	40h	7.0 µs
40h	2.80 µs	40h	28.0 µs	5Ah	9.6 µs
7Fh	5.32 µs	7Fh	53.2 µs	7Fh	13.3 µs

Note: *The IEEE 802.3, 802.3(u) minimum values are shaded.

A non-back-to-back Transmit IPG is determined by the following formula:

(6 clocks + IPGR2 clocks) * clock period = IPG

The difference in values between Table 189 on page 306 and Table 190 is due to the asynchronous nature of the Carrier Sense (CRS). The CRS must undergo a 2-clock synchronization before the internal Tx state machine detects it. This synchronization equates to a 6-clock intrinsic delay between packets instead of the 3-clock intrinsic delay in the back-to-back packet mode. More information covering this topic is found in the IEEE 802.3/4.2.3.2.1 Carrier Deference section.

EMAC Interpacket Gap Register

The EMAC Interpacket Gap (IPG) is a programmable field representing the IPG between back-to-back packets. It is the IPG parameter used in FULL-DUPLEX and HALF-DUPLEX modes between back-to-back packets. Set this field to the appropriate number of IPG bytes. The default setting of `15h` represents the minimum IPG of 0.96 µs (at 100 Mbps) or 9.6 µs (at 10 Mbps). See Table 191.

Table 191. EMAC Interpacket Gap Register (EMAC_IPGT = 002Dh)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	1	0	1	0	1
CPU Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: R = Read Only; R/W = Read/Write

Table 213. EMAC Receive Read Pointer Register—High Byte (EMAC_RRP_H = 004Ah)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	R	R	R	R/W	R/W	R/W	R/W	R/W

Note: R = Read Only, R/W = Read/Write.

Bit Position	Value	Description
[7:0] EMAC_RRP_H	00h–FFh	These bits represent the High byte of the 2-byte EMAC Receive Read Pointer value, {EMAC_RRP_H, EMAC_RRP_L}. Bit 7 is bit 15 (msb) of the 16-bit value. Bits 7:5 default to 000 on reset; bit 0 is bit 8 of the 16-bit value.

EMAC Buffer Size Register

The lower six bits of this register set the level at which the EMAC either transmits a pause control frame or jams the Ethernet bus, depending on the mode selected. When each of these bits contain a zero, this feature is disabled.

In FULL-DUPLEX mode, a Pause Control Frame is transmitted as a One-shot operation. The software must free up a number of Rx buffers so that the number of buffers remaining, EmacBlksLeft, is greater than TCPF_LEV.

In HALF-DUPLEX mode, the EMAC jams the Ethernet by sending a continuous stream of hexadecimal 5s (`5fh`). When the software frees up the Rx buffers and the number of buffers remaining, EmacBlksLeft, is greater than TCPF_LEV, the EMAC stops jamming.

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