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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	eZ80
Core Size	8-Bit
Speed	50MHz
Connectivity	Ethernet, I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	32
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/ez80f91az050eg

Table 2. Pin Identification on the eZ80F91 Device (Continued)

LQFP Pin No	BGA Pin No	Symbol	Function	Signal Direction	Description
127	C7	TxD2	MII Transmit Data	Output	This pin is used by the Ethernet MAC for the MII Interface to the PHY. Transmit Data is synchronous to the rising-edge of Tx_CLK.
128	D7	TxD1	MII Transmit Data	Output	This pin is used by the Ethernet MAC for the MII Interface to the PHY. Transmit Data is synchronous to the rising-edge of Tx_CLK.
129	A6	TxD0	MII Transmit Data	Output	This pin is used by the Ethernet MAC for the MII Interface to the PHY. Transmit Data is synchronous to the rising-edge of Tx_CLK.
130	B6	Tx_EN	MII Transmit Enable	Output	This pin is used by the Ethernet MAC for the MII Interface to the PHY. Transmit Enable is synchronous to the rising-edge of Tx_CLK.
131	C6	Tx_CLK	MII Transmit Clock	Input	This pin is used by the Ethernet MAC for the MII Interface to the PHY. Transmit Clock is the Nibble or Symbol Clock provided by the MII PHY interface.
132	E7	Tx_ER	MII Transmit Error	Output	This pin is used by the Ethernet MAC for the MII Interface to the PHY. Transmit Error is synchronous to the rising-edge of Tx_CLK.
133	A5	V_{DD}	Power Supply		Power Supply.
134	B5	V_{SS}	Ground		Ground.
135	D6	Rx_ER	MII Receive Error	Input	This pin is used by the Ethernet MAC for the MII Interface to the PHY. Receive Error is provided by the MII PHY interface synchronous to the rising-edge of Rx_CLK.
136	C5	Rx_CLK	MII Receive Clock	Input	This pin is used by the Ethernet MAC for the MII Interface to the PHY. Receive Clock is the Nibble or Symbol Clock provided by the MII PHY interface.

Table 3. Register Map (Continued)

Address# (hex)	Mnemonic	Name	Reset (hex)	CPU Access	Page No
0026	EMAC_STAD_1	EMAC Station Address—Byte 1	00	R/W	304
0027	EMAC_STAD_2	EMAC Station Address—Byte 2	00	R/W	304
0028	EMAC_STAD_3	EMAC Station Address—Byte 3	00	R/W	304
0029	EMAC_STAD_4	EMAC Station Address—Byte 4	00	R/W	304
002A	EMAC_STAD_5	EMAC Station Address—Byte 5	00	R/W	304
002B	EMAC_TPTV_L	EMAC Transmit Pause # Timer Value—Low Byte	00	R/W	305
002C	EMAC_TPTV_H	EMAC Transmit Pause # Timer Value—High Byte	00	R/W	305
002D	EMAC_IPGT	EMAC Inter-Packet Gap	15	R/W	306
002E	EMAC_IPGR1	EMAC Non-Back-Back IPG	0C	R/W	308
002F	EMAC_IPGR2	EMAC Non-Back-Back IPG	12	R/W	308
0030	EMAC_MAXF_L	EMAC Maximum Frame # Length—Low Byte	00	R/W	309
0031	EMAC_MAXF_H	EMAC Maximum Frame # Length—High Byte	06	R/W	310
0032	EMAC_AFR	EMAC Address Filter Register	00	R/W	311
0033	EMAC_HTBL_0	EMAC Hash Table—Byte 0	00	R/W	312
0034	EMAC_HTBL_1	EMAC Hash Table—Byte 1	00	R/W	312
0035	EMAC_HTBL_2	EMAC Hash Table—Byte 2	00	R/W	312
0036	EMAC_HTBL_3	EMAC Hash Table—Byte 3	00	R/W	312
0037	EMAC_HTBL_4	EMAC Hash Table—Byte 4	00	R/W	312
0038	EMAC_HTBL_5	EMAC Hash Table—Byte 5	00	R/W	312
0039	EMAC_HTBL_6	EMAC Hash Table—Byte 6	00	R/W	312
003A	EMAC_HTBL_7	EMAC Hash Table—Byte 7	00	R/W	312
003B	EMAC_MIIMGT	EMAC MII Management Register	00	R/W	313
003C	EMAC_CTLD_L	EMAC PHY Configuration # Data—Low Byte	00	R/W	314
003D	EMAC_CTLD_H	EMAC PHY Configuration # Data—High Byte	00	R/W	315
003E	EMAC_RGAD	EMAC PHY Register Address Register	00	R/W	315

Interrupt Controller

The interrupt controller on the eZ80F91 device routes the interrupt request signals from the internal peripherals, external devices (via internal port I/O) and the nonmaskable interrupt (NMI) pin to the CPU.

Maskable Interrupts

On the eZ80F91 device, all maskable interrupts use the CPU's vectored interrupt function. The size of I register is modified to 16 bits in the eZ80F91 device differing from the previous versions of eZ80® CPU, to allow for a 16 MB range of interrupt vector table placement. Additionally, the size of the IVECT register is increased from 8 bits to 9 bits to provide an interrupt vector table that is expanded and more easily integrated with other interrupts.

The vectors are 4 bytes (32 bits) apart, even though only 3 bytes (24 bits) are required. A fourth byte is implemented for both programmability and expansion purposes.

Starting the interrupt vectors at 40h allows for easy implementation of the interrupt controller vectors with the RST vectors. Table 12 lists the interrupt vector sources by priority for each of the maskable interrupt sources. The maskable interrupt sources are listed in order of their priority, with vector 40h being the highest-priority interrupt. In ADL mode, the full 24-bit interrupt vector is located at starting address {I[15:1], IVECT[8:0]}, where I[15:0] is the CPU's Interrupt Page Address register.

Table 12. Interrupt Vector Sources by Priority

Priority	Vector	Source	Priority	Vector	Source
0	040h	EMAC Rx	24	0A0h	Port B 0
1	044h	EMAC Tx	25	0A4h	Port B 1
2	048h	EMAC SYS	26	0A8h	Port B 2
3	04Ch	PLL	27	0ACh	Port B 3
4	050h	Flash	28	0B0h	Port B 4
5	054h	Timer 0	29	0B4h	Port B 5
6	058h	Timer 1	30	0B8h	Port B 6
7	05Ch	Timer 2	31	0BCh	Port B 7
8	060h	Timer 3	32	0C0h	Port C 0
9	064h	Unused*	33	0C4h	Port C 1
10	068h	Unused*	34	0C8h	Port C 2

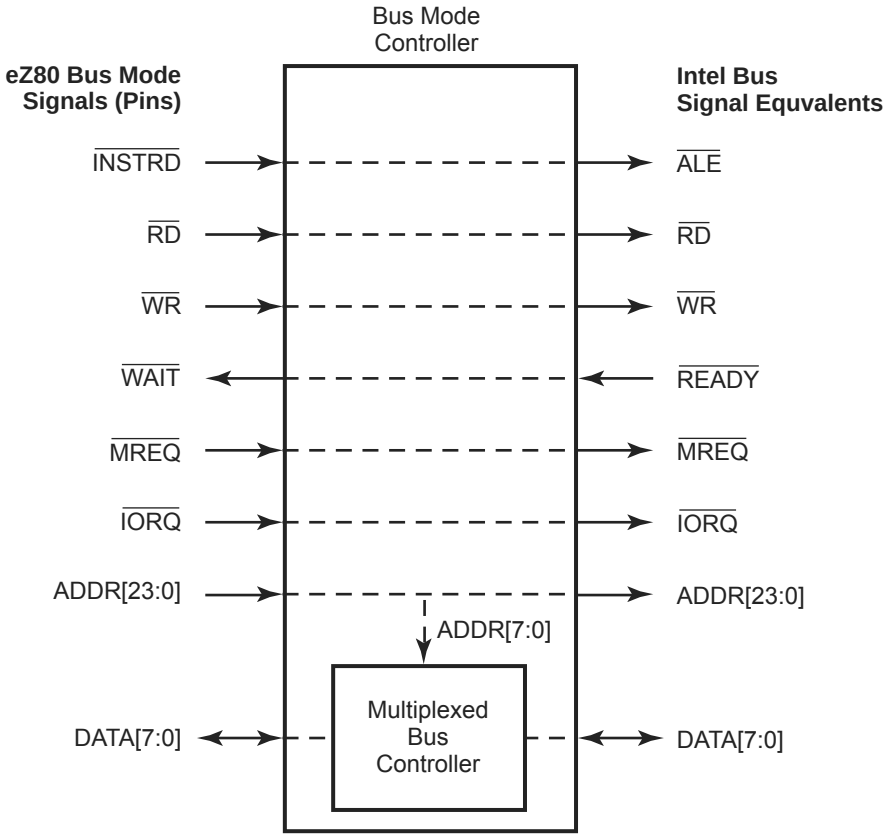

Figure 12. Intel Bus Mode Signal and Pin Mapping

Intel™ Bus Mode—Separate Address and Data Buses

During Read operations with separate address and data buses, the Intel bus mode employs four states—T1, T2, T3, and T4 as listed in Table 21.

Table 21. Intel Bus Mode Read States—Separate Address and Data Buses

STATE T1	The Read cycle begins in State T1. The CPU drives the address onto the address bus and the associated chip select signal is asserted. The CPU drives the ALE signal High at the beginning of T1. In the middle of T1, the CPU drives ALE Low to facilitate the latching of the address.
STATE T2	During State T2, the CPU asserts the $\overline{RD}$ signal. Depending on the instruction, either the $\overline{MREQ}$ or $\overline{IORQ}$ signal is asserted.

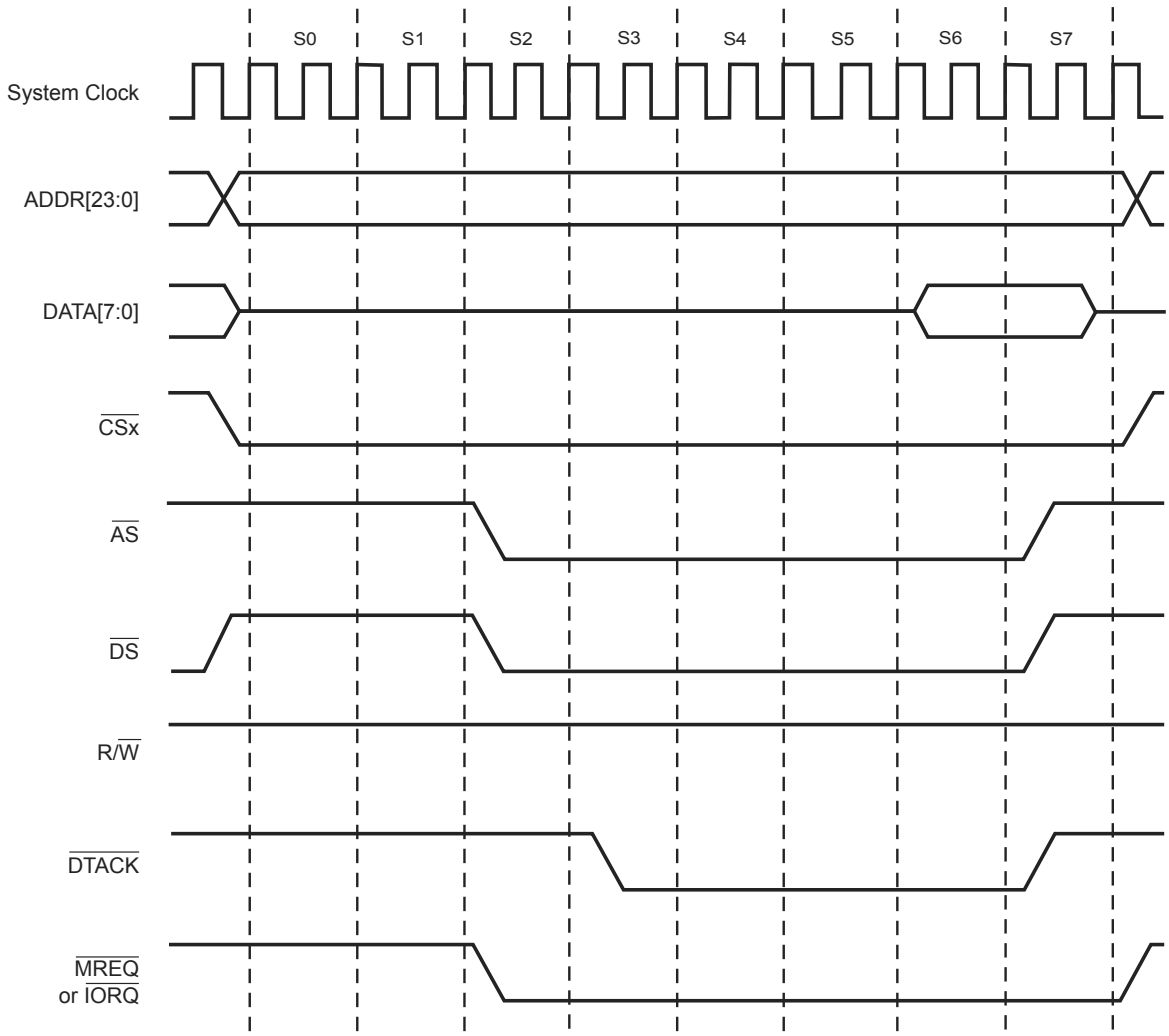

Figure 18. Example: Motorola Bus Mode Read Timing

Random Access Memory

The eZ80F91 device features 8 KB (8192 bytes) of single-port data Random Access Memory (RAM) for general-purpose use and 8 KB of RAM for the EMAC. RAM is enabled or disabled, and it is relocated to the top of any 64 KB page in memory. Data is passed to and from RAM via the 8-bit data bus. On-chip RAM operates with zero wait states. EMAC RAM is accessed via the bus master and executes with zero or one Wait states.

General-purpose RAM occupies memory addresses in the RAM Address Upper Byte register in the range {RAM_ADDR_U[7:0], E000h} to {RAM_ADDR_U[7:0], FFFFh}. EMAC RAM occupies memory addresses in the range {RAM_ADDR_U[7:0], C000h} to {RAM_ADDR_U[7:0], DFFFh}. Following a RESET, RAM is enabled when RAM_ADDR_U is set to FFh. Figure 22 displays a memory map for on-chip RAM. In this example, RAM_ADDR_U is set to 7Ah. Figure 22 is not drawn to scale, as RAM occupies only a very small fraction of the available 16 MB address space.

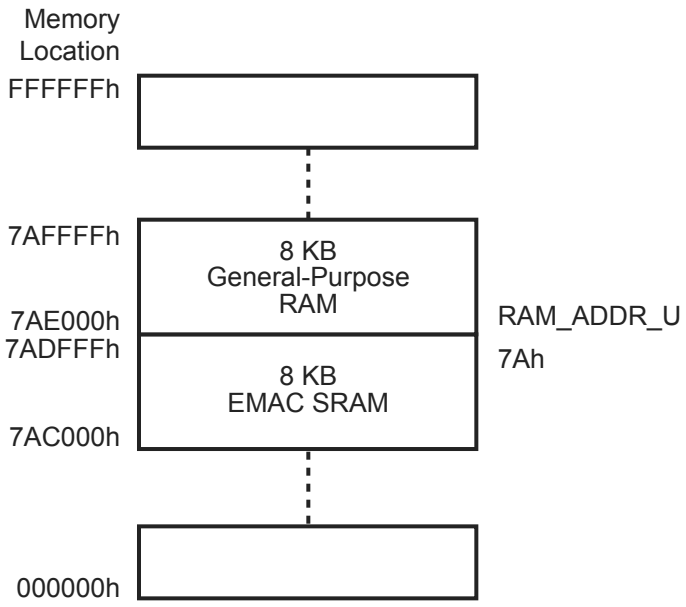

Figure 22. Example: eZ80F91 On-Chip RAM Memory Addressing

When enabled, on-chip RAM assumes priority over on-chip Flash memory and any memory chip selects that is also enabled in the same address space. If an address is generated in a range that is covered by both the RAM address space and a particular memory chip

Pulse-Width Modulation Control Register 2

The PWM Control Register 2 (see Table 74) controls pulse-width modulation AND/OR and edge delay functions.

Table 74. PWM Control Register 2 (PWM_CTL2 = 007Ah)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: R/W = Read/Write.

Bit# Position	Value	Description
[7:6] AON_EN	00	Disable AND/OR features on $\overline{PWM}$
	01	Enable AND logic on $\overline{PWM}$
	10	Enable OR logic on $\overline{PWM}$
	11	Disable AND/OR features on $\overline{PWM}$
[5:4] AO_EN	00	Disable AND/OR features on PWM
	01	Enable AND logic on PWM
	10	Enable OR logic on PWM
	11	Disable AND/OR features on PWM

Real-Time Clock Alarm Minutes Register

This register contains the alarm minutes value. The value in the RTC_AMIN register is unchanged by a RESET. The current setting of BCD_EN determines whether the values in this register are binary (BCD_EN = 0) or binary-coded decimal (BCD_EN = 1). See Table 89.

Table 89. Real-Time Clock Alarm Minutes Register (RTC_AMIN = 00E9h)

Bit	7	6	5	4	3	2	1	0
Reset	X	X	X	X	X	X	X	X
CPU Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: X = Unchanged by RESET; R/W = Read/Write.

Binary-Coded Decimal Operation (BCD_EN = 1)		
Bit Position	**Value**	**Description**
[7:4] ATEN_MIN	0–5	The tens digit of the alarm minutes value.
[3:0] AMIN	0–9	The ones digit of the alarm minutes value.

Binary Operation (BCD_EN = 0)		
Bit Position	**Value**	**Description**
[7:0] AMIN	00h–3Bh	The alarm minutes value.

Bit Position	Value	Description
3 OUT2	0–1	No function in normal operation. In LOOP BACK mode, this bit is connected to the DCD bit in the UART Status Register.
2 OUT1	0–1	No function in normal operation. In LOOP BACK mode, this bit is connected to the RI bit in the UART Status Register.
1 RTS	0–1	Request to Send. In normal operation, the $\overline{RTS}$ output port is the inverse of this bit. In LOOP BACK mode, this bit is connected to the CTS bit in the UART Status Register.
0 DTR	0–1	Data Terminal Ready. In normal operation, the $\overline{DTR}$ output port is the inverse of this bit. In LOOP BACK mode, this bit is connected to the DSR bit in the UART Status Register.

UART Line Status Register

This register is used to show the status of UART interrupts and registers. See Table 106

Table 106. UART Line Status Registers (UART0_LSR = 00C5h, UART1_LSR = 00D5h)

Bit	7	6	5	4	3	2	1	0
Reset	0	1	1	0	0	0	0	0
CPU Access	R	R	R	R	R	R	R	R
Note: R = Read only.								

Bit Position	Value	Description
7 ERR	0	Always 0 when operating in with the FIFO disabled. With the FIFO enabled, this bit is reset when the UARTx_LSR register is read and there are no more bytes with error status in the FIFO.
	1	Error detected in the FIFO. There is at least 1 parity, framing or break indication error in the FIFO.
6 TEMT	0	Transmit holding register/FIFO is not empty or transmit shift register is not empty or transmitter is not idle.
	1	Transmit holding register/FIFO and transmit shift register are empty; and the transmitter is idle. This bit cannot be set to 1 during the BREAK condition. This bit only becomes 1 after the BREAK command is removed.

Infrared Encoder/Decoder Register

After a RESET, the Infrared Encoder/Decoder Register is set to its default value. Any Writes to unused register bits are ignored and reads return a value of 0. The IR_CTL register is listed in Table 110.

Table 110. Infrared Encoder/Decoder Control Registers (IR_CTL = 00BFh)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
Note: R = Read only; R/W = Read/Write.								

Bit Position	Value	Description
[7:4] MIN_PULSE	0000	Minimum receive pulse width control. When this field is equal to 0x0, the IrDA decoder uses edge detection to accept arbitrarily narrow (that is, short) input pulses.
	1h-Fh	When not equal to 0x0, this field forms the most-significant four bits of the 6-bit down-counter used to determine if an input pulse will be ignored because it is too narrow. The lower two counter bits are hard-coded to load with 0x3, resulting in a total down-count equal to ((IR_CTL[4:0]MIN_PULSE * 4) + 3). To be accepted, input pulses must have a width greater than or equal to the down-count value times the system clock period.
3	0	Reserved.
2 LOOP_BACK	0	Internal LOOP BACK mode is disabled.
	1	Internal LOOP BACK mode is enabled. IR_TxD output is inverted and connected to IR_RxD input for internal loop back testing.
1 IR_RxEN	0	IR_RxD data is ignored.
	1	IR_RxD data is passed to UART0 RxD.
0 IR_EN	0	Endec is disabled.
	1	Endec is enabled.

SPI Signals

The four basic SPI signals are:

- MISO (Master In, Slave Out)
- MOSI (Master Out, Slave In)
- SCK (SPI Serial Clock)
- $\overline{SS}$ (Slave Select)

These SPI signals are discussed in the following paragraphs. Each signal is described in both MASTER and SLAVE modes.

Master In, Slave Out

The Master In, Slave Out (MISO) pin is configured as an input in a master device and as an output in a slave device. It is one of the two lines that transfer serial data, with the most-significant bit (msb) sent first. The MISO pin of a slave device is placed in a high-impedance state if the slave is not selected. When the SPI is not enabled, this signal is in a high-impedance state.

Master Out, Slave In

The Master Out, Slave In (MOSI) pin is configured as an output in a master device and as an input in a slave device. It is one of the two lines that transfer serial data, with the msb sent first. When the SPI is not enabled, this signal is in a high-impedance state.

Slave Select

The active Low Slave Select ($\overline{SS}$) input signal is used to select the SPI as a slave device. It must be Low prior to all data communication and must stay Low for the duration of the data transfer.

The $\overline{SS}$ input signal must be High for the SPI to operate as a master device. If the $\overline{SS}$ signal goes Low in Master mode, a Mode Fault error flag (MODF) is set in the SPI_SR register. For more information, see SPI Status Register on page 209.

When the clock phase (CPHA) is set to 0, the shift clock is the logical OR of $\overline{SS}$ with SCK. In this clock phase mode, $\overline{SS}$ must go High between successive characters in an SPI message. When CPHA is set to 1, $\overline{SS}$ remains Low for several SPI characters. In cases where there is only one SPI slave, its $\overline{SS}$ line could be tied Low as long as CPHA is set to 1. For more information on CPHA, see SPI Control Register on page 208.

Serial Clock

The Serial Clock (SCK) is used to synchronize data movement both in and out of the device via its MOSI and MISO pins. The master and slave are each capable of exchanging a byte of data during a sequence of eight clock cycles. Because SCK is generated by the master, the SCK pin becomes an input on a slave device. The SPI contains an internal

I²C Serial I/O Interface

I²C General Characteristics

The Inter-Integrated Circuit (I²C) serial I/O bus is a two-wire communication interface that operates in four modes:

- MASTER TRANSMIT
- MASTER RECEIVE
- SLAVE TRANSMIT
- SLAVE RECEIVE

The I²C interface consists of a Serial Clock (SCL) and Serial Data (SDA). Both SCL and SDA are bidirectional lines connected to a positive supply voltage via an external pull-up resistor. When the bus is free, both lines are High. The output stages of devices connected to the bus must be configured as open-drain outputs. Data on the I²C bus are transferred at a rate of up to 100 kbps in STANDARD mode, or up to 400 kbps in FAST mode. One clock pulse is generated for each data bit transferred.

Clocking Overview

If another device on the I²C bus drives the clock line when the I²C is in MASTER mode, the I²C synchronizes its clock to the I²C bus clock. The High period of the clock is determined by the device that generates the shortest High clock period. The Low period of the clock is determined by the device that generates the longest Low clock period.

The Low period of the clock is stretched by a slave to slow down the bus master. The Low period is also stretched for handshaking purposes. This result is accomplished after each bit transfer or each byte transfer. The I²C stretches the clock after each byte transfer until the IFLG bit in the I2C_CTL register is cleared to 0.

Bus Arbitration Overview

In MASTER mode, the I²C checks that each transmitted logic 1 appears on the I²C bus as a logic 1. If another device on the bus overruled and pulls the SDA signal Low, arbitration is lost. If arbitration is lost during the transmission of a data byte or a Not Acknowledge (NACK) bit, the I²C returns to an idle state. If arbitration is lost during the transmission of an address, the I²C switches to SLAVE mode so that it recognizes its own slave address or the general call address.

Table 118. I²C Master Transmit Status Codes

Code	I²C State	Microcontroller Response	Next I²C Action
18h	Addr+W transmitted ACK received[1]	For a 7-bit address: write byte to DATA, clear IFLG	Transmit data byte, receive ACK
		Or set STA, clear IFLG	Transmit repeated START
		Or set STP, clear IFLG	Transmit STOP
		Or set STA & STP, clear IFLG	Transmit STOP then START
		For a 10-bit address: write extended address byte to data, clear IFLG	Transmit extended address byte
20h	Addr+W transmitted, ACK not received	Same as code 18h	Same as code 18h
38h	Arbitration lost	Clear IFLG	Return to idle
		Or set STA, clear IFLG	Transmit START when bus is free
68h	Arbitration lost, # +W received, # ACK transmitted	Clear IFLG, AAK = 0[2]	Receive data byte, transmit NACK
		Or clear IFLG, AAK = 1	Receive data byte, transmit ACK
78h	Arbitration lost, General call address received, ACK transmitted	Same as code 68h	Same as code 68h
B0h	Arbitration lost, # SLA+R received, # ACK transmitted[3]	Write byte to DATA, clear IFLG, clear AAK = 0	Transmit last byte, receive ACK
		Or write byte to DATA, clear IFLG, set AAK = 1	Transmit data byte, receive ACK

Notes
1. W is defined as the Write bit; that is, the lsb is cleared to 0.
2. AAK is an I²C control bit that identifies which ACK signal to transmit.
3. R is defined as the Read bit; that is, the lsb is set to 1.

If 10-bit addressing is used, the status code is 18h or 20h after the first part of a 10-bit address, plus the Write bit, are successfully transmitted.

After this interrupt is serviced and the second part of the 10-bit address is transmitted, the I2C_SR register contains one of the codes listed in Table 119.

ZDI Bus Control Register

The ZDI Bus Control register controls bus requests during DEBUG mode. It enables or disables bus acknowledge in ZDI DEBUG mode and allows ZDI to force assertion of the $\overline{BUSACK}$ signal. This register must only be written during ZDI DEBUG mode (that is, following a break). See Table 140.

Table 140. ZDI Bus Control Register (ZDI_BUS_CTL = 17h in the ZDI Register Write Only Address Space)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	W	W	W	W	W	W	W	W

Note: W = Write Only.

Bit Position	Value	Description
7 ZDI_BUSAK_EN	0	Bus requests by external peripherals using the $\overline{BUSREQ}$ pin are ignored. The bus acknowledge signal, $\overline{BUSACK}$, is not asserted in response to any bus requests.
	1	Bus requests by external peripherals using the $\overline{BUSREQ}$ pin are accepted. A bus acknowledge occurs at the end of the current ZDI operation. The bus acknowledge is indicated by asserting the $\overline{BUSACK}$ pin in response to a bus request.
6 ZDI_BUSAK	0	Deassert the bus acknowledge pin ($\overline{BUSACK}$) to return control of the address and data buses back to ZDI.
	1	Assert the bus acknowledge pin ($\overline{BUSACK}$) to pass control of the address and data buses to an external peripheral.
[5:0]	000000	Reserved.

Instruction Store 4:0 Registers

The ZDI Instruction Store registers are located in the ZDI Register Write Only address space. They are written with instruction data for direct execution by the CPU. When the ZDI_IS0 register is written, the eZ80F91 device exits the ZDI break state and executes a single instruction. The opcodes and operands for the instruction come from these Instruction Store registers. The Instruction Store Register 0 is the first byte fetched, followed by Instruction Store registers 1, 2, 3, and 4, as necessary. Only the bytes the CPU requires to execute the instruction must be stored in these registers. Some CPU instructions, when combined with the MEMORY mode suffixes (.SIS, .SIL, .LIS, or .LIL), require 6 bytes to

Table 160. Exchange Instructions

Mnemonic	Instruction
EX	Exchange registers
EXX	Exchange CPU Multibyte register banks

Table 161. Input/Output Instructions

Mnemonic	Instruction
IN	Input from I/O
IN0	Input from I/O on Page 0
IND (INDR)	Input from I/O and Decrement (with Repeat)
INDRX	Input from I/O and Decrement Memory Address with Stationary I/O Address
IND2 (IND2R)	Input from I/O and Decrement (with Repeat)
INDM (INDMR)	Input from I/O and Decrement (with Repeat)
INI (INIR)	Input from I/O and Increment (with Repeat)
INIRX	Input from I/O and Increment Memory Address with Stationary I/O Address
INI2 (INI2R)	Input from I/O and Increment (with Repeat)
INIM (INIMR)	Input from I/O and Increment (with Repeat)
OTDM (OTDMR)	Output to I/O and Decrement (with Repeat)
OTDRX	Output to I/O and Decrement Memory Address with Stationary I/O Address
OTIM (OTIMR)	Output to I/O and Increment (with Repeat)
OTIRX	Output to I/O and Increment Memory Address with Stationary I/O Address
OUT	Output to I/O
OUT0	Output to I/0 on Page 0
OUTD (OTDR)	Output to I/O and Decrement (with Repeat)
OUTD2 (OTD2R)	Output to I/O and Decrement (with Repeat)
OUTI (OTIR)	Output to I/O and Increment (with Repeat)

EMAC Interrupts

Eight different sources of interrupts from the EMAC are listed in Table 176.

Table 176. EMAC Interrupts

Interrupt	Description
EMAC System Interrupts	
Transmit State Machine Error	Bit 7 (TxFSMERR_STAT) of the EMAC Interrupt Status Register (EMAC_ISTAT). A Transmit State Machine Error must not occur. However, if this bit is set, the entire transmitter module must be reset.
MIIMGT Done	Bit 6 (MGTDONE_STAT) of the Interrupt Status Register (EMAC_ISTAT). This bit is set when communicating to the PHY over the MII during a Read or Write operation.
Receive Overrun	Bit 2 (Rx_OVR_STAT) of the Interrupt Status Register (EMAC_ISTAT). If this bit is set, all incoming packets are ignored until this bit is cleared by software.
EMAC Transmitter Interrupts	
Transmit Control Frame	Transmit Control Frame = Bit 1 (Tx_CF_STAT) of the Interrupt Status Register (EMAC_ISTAT). Denotes when control frame transmission is complete.
Transmit Done	Bit 0 (Tx_DONE_STAT) of the Interrupt Status Register (EMAC_ISTAT). Denotes when packet transmission is complete.
EMAC Receiver Interrupts	
Receive Packet	Bit 5 (Rx_CF_STAT) of the Interrupt Status Register (EMAC_ISTAT). Denotes when packet reception is complete.
Receive Pause Packet	Bit 4 (Rx_PCF_STAT) of the Interrupt Status Register (EMAC_ISTAT). Denotes when pause packet reception is complete.
Receive Done	Bit 3 (Rx_DONE_STAT) of the Interrupt Status Register (EMAC_ISTAT). Denotes when packet reception is complete.

EMAC Shared Memory Organization

Internal Ethernet SRAM shares memory with the CPU. This memory is divided into the Transmit buffer and the Receive buffer by defining three registers, as listed below.

- Transmit Lower Boundary Pointer (TLBP)—this register points to the start of the Transmit buffer in the internal Ethernet shared memory space.
- Boundary Pointer (BP)—this register points to the start of the Receive buffer.

EMAC Interrupt Status Register

When a Receive overrun occurs, all incoming packets are ignored until the Rx_OVR_STAT status bit is cleared by software. Consequently, software controls when the receiver is re-enabled after an overrun. Enable the Rx_OVR interrupt to detect overrun conditions when they occur. Clear this condition when the Rx buffers are freed to avoid additional overrun errors. See Table 216.

Note: Status bits are not self-clearing. Each status bit is cleared by writing a 1 into the selected bit.

Table 216. EMAC Interrupt Status Register (EMAC_ISTAT = 004Dh)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: R/W = Read/Write.

Bit Position	Value	Description
7 TxFSMERR_STAT	1	An internal error occurs in the EMAC Transmit path. The Transmit path must be reset to reset this error condition.
	0	Normal operation—no Transmit state machine errors.
6 MGTDONE_STAT	1	The MII Management interrupt has completed a Read (RSTAT or SCAN) or a Write (LDCTLD) access to the PHY.
	0	The MII Management interrupt does not occur.
5 Rx_CF_STAT	1	Receive Control Frame interrupt (Receive Interrupt) occurs.
	0	Receive Control Frame interrupt does not occur.
4 Rx_PCF_STAT	1	Receive Pause Control Frame interrupt (Receive Interrupt) occurs.
	0	Disable Receive Pause Control Frame interrupt (Receive Interrupt) does not occur.
3 Rx_DONE_STAT	1	Receive Done interrupt (Receive Interrupt) occurs.
	0	Disable Receive Done interrupt (Receive Interrupt) does not occur.
2 Rx_OVR_STAT	1	Receive Overrun interrupt (System Interrupt) occurs.
	0	Receive Overrun interrupt (System Interrupt) does not occur.

Electrical Characteristics

Absolute Maximum Ratings

Stresses greater than those listed in Table 232 can cause permanent damage to the device. These ratings are stress ratings only. Operation of the device at any condition outside those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability. For improved reliability, unused inputs must be tied to one of the supply voltages (V_{DD} or V_{SS}).

Table 232. Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units	Notes
Ambient temperature under bias (ºC)	–40	+105	ºC	1
Storage temperature (ºC)	–65	+150	C	
Voltage on any pin with respect to V_{SS}	–0.3	+5.5	V	2
Voltage on V_{DD} pin with respect to V_{SS}	–0.3	+3.6	V	
Total power dissipation		830	mW	
Maximum current out of V_{SS}		230	mA	
Maximum current into V_{DD}		230	mA	
Maximum current on input and/or inactive output pin	–15	+15	µA	
Maximum output current from active output pin	–8	+8	mA	
Flash memory Writes to Same Single Address	—	2	—	3
Flash Memory Data Retention	100	—	Years	
Flash Memory Write/Erase Endurance	10,000	—	Cycles	4

Notes
1. Operating temperature is specified in DC Characteristics.
2. This voltage applies to all pins except X_{IN} and X_{OUT}.
3. Before next erase operation.
4. Write cycles.

DC Characteristics

Table 233 on page 340 lists the DC characteristics of the eZ80F91 device.