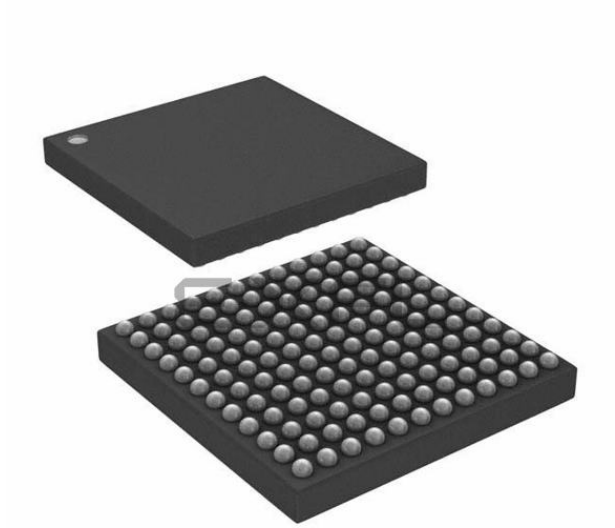

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	eZ80
Core Size	8-Bit
Speed	50MHz
Connectivity	Ethernet, I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	32
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LBGA
Supplier Device Package	144-BGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/ez80f91na050ec00tr

Table 2. Pin Identification on the eZ80F91 Device (Continued)

LQFP Pin No	BGA Pin No	Symbol	Function	Signal Direction	Description
103	D11	PB3	GPIO Port B	Bidirectional with Schmitt-trigger input	This pin is used for GPIO. It is individually programmed as input or output and is also used individually as an interrupt input. Each Port B pin, when programmed as output is selected to be an open-drain or open-source output.
		SCK	SPI Serial Clock	Bidirectional with Schmitt-trigger input	SPI serial clock. This signal is multiplexed with PB3.
104	E9	PB4	GPIO Port B	Bidirectional with Schmitt-trigger input	This pin is used for GPIO. It is individually programmed as input or output and is also used individually as an interrupt input. Each Port B pin, when programmed as output is selected to be an open-drain or open-source output.
		IC2	Input Capture	Schmitt-trigger input	Input Capture A Signal to Timer 3. This signal is multiplexed with PB4.
105	D10	PB5	GPIO Port B	Bidirectional with Schmitt-trigger input	This pin is used for GPIO. It is individually programmed as input or output and is also used individually as an interrupt input. Each Port B pin, when programmed as output is selected to be an open-drain or open-source output.
		IC3	Input Capture	Schmitt-trigger input	Input Capture B Signal to Timer 3. This signal is multiplexed with PB5.

Table 2. Pin Identification on the eZ80F91 Device (Continued)

LQFP Pin No	BGA Pin No	Symbol	Function	Signal Direction	Description
117	B9	PA3	GPIO Port A	Bidirectional	This pin is used for GPIO. It is individually programmed as input or output and is also used individually as an interrupt input. Each Port A pin, when programmed as output is selected to be an open-drain or open-source output.
		PWM3	PWM Output 3	Output	This pin is used by Timer 3 for PWM 3. This signal is multiplexed with PA3.
		OC3	Output Compare 3	Output	This pin is used by Timer 3 for Output Compare 3 This signal is multiplexed with PA3.
118	A9	PA4	GPIO Port A	Bidirectional	This pin is used for GPIO. It is individually programmed as input or output and is also used individually as an interrupt input. Each Port A pin, when programmed as output is selected to be an open-drain or open-source output.
		PWM0	PWM Output 0 Inverted	Output	This pin is used by Timer 3 for negative PWM 0. This signal is multiplexed with PA4.
		TOUT0	Timer Out	Output	This pin is used by Timer 0 timer-out signal. This signal is multiplexed with PA4.
119	C9	PA5	GPIO Port A	Bidirectional	This pin is used for GPIO. It is individually programmed as input or output and is also used individually as an interrupt input. Each Port A pin, when programmed as output is selected to be an open-drain or open-source output.
		PWM1	PWM Output 1 Inverted	Output	This pin is used by Timer 3 for negative PWM 1. This signal is multiplexed with PA5.
		TOUT2	Timer Out	Output	This pin is used by the Timer 2 timer-out signal. This signal is multiplexed with PA5.

Table 3. Register Map (Continued)

Address (hex)	Mnemonic	Name	Reset (hex)	CPU Access	Page No
007D	PWM0R_H	PWM 0 Rising-Edge Register—High Byte	XX	R/W	157
	TMR3_CAPA_H	Timer 3 Capture Value A Register—High Byte	XX	R/W	141
007E	PWM1R_L	PWM 1 Rising-Edge Register—Low Byte	XX	R/W	157
	TMR3_CAPB_L	Timer 3 Capture Value B Register—Low Byte	XX	R/W	141
007F	PWM1R_H	PWM 1 Rising-Edge Register—High Byte	XX	R/W	157
	TMR3_CAPB_H	Timer 3 Capture Value B Register—High Byte	XX	R/W	142
0080	PWM2R_L	PWM 2 Rising-Edge Register—Low Byte	XX	R/W	157
	TMR3_OC_CTL1	Timer 3 Output Compare Control Register 1	00	R/W	132
0081	PWM2R_H	PWM 2 Rising-Edge Register—High Byte	XX	R/W	157
	TMR3_OC_CTL2	Timer 3 Output Compare Control Register 2	00	R/W	132
0082	PWM3R_L	PWM 3 Rising-Edge Register—Low Byte	XX	R/W	157
	TMR3_OC0_L	Timer 3 Output Compare 0 Value Register—Low Byte	XX	R/W	144
0083	PWM3R_H	PWM 3 Rising-Edge Register—High Byte	XX	R/W	157
	TMR3_OC0_H	Timer 3 Output Compare 0 Value Register—High Byte	XX	R/W	145
0084	PWM0F_L	PWM 0 Falling-Edge Register—Low Byte	XX	R/W	158
	TMR3_OC1_L	Timer 3 Output Compare 1 Value Register—Low Byte	XX	R/W	144

boundary. Setting the LSB of the I register produces no effect on the interrupt vector address.

Table 13. Vectored Interrupt Operation

Memory Mode	ADL Bit	MADL Bit	Operation
Z80® Mode	0	0	Read the LSB of the interrupt vector placed on the internal vectored interrupt bus, IVECT [8:0], by the interrupting peripheral. IEF1 ← 0 IEF2 ← 0 The Starting Program Counter is effective {MBASE, PC[15:0]}. Push the 2-byte return address PC[15:0] onto the ({MBASE,SPS}) stack. The ADL mode bit remains cleared to 0. The interrupt vector address is located at { MBASE, I[7:1], IVECT[8:0] }. PC[23:0] ← ({ MBASE, I[7:1], IVECT[8:0] }). The interrupt service routine must end with RETI.
ADL Mode	1	0	Read the LSB of the interrupt vector placed on the internal vectored interrupt bus, IVECT [8:0], by the interrupting peripheral. IEF1 ← 0 IEF2 ← 0 The Starting Program Counter is PC[23:0]. Push the 3-byte return address, PC[23:0], onto the SPL stack. The ADL mode bit remains set to 1. The interrupt vector address is located at { I[15:1], IVECT[8:0] }. PC[23:0] ← ({ I[15:1], IVECT[8:0] }). The interrupt service routine must end with RETI.
Z80 Mode	0	1	**Read the LSB of the interrupt vector placed on the internal vectored interrupt bus, IVECT[8:0], bus by the interrupting peripheral.** • **IEF1 ← 0** • **IEF2 ← 0** • The Starting Program Counter is effective {MBASE, PC[15:0]}. • Push the 2-byte return address, PC[15:0], onto the SPL stack. • Push a 00h byte onto the SPL stack to indicate an interrupt from Z80 mode (because ADL = 0). • Set the ADL mode bit to 1. • The interrupt vector address is located at { I[15:1], IVECT[8:0] }. • PC[23:0] ← **({ I[15:1], IVECT[8:0] })**. • The interrupt service routine must end with RETI.L

FLASH_DATA register causes an autoincrement of the Flash address stored in the Flash Address registers (FLASH_PAGE, FLASH_ROW, FLASH_COL). See Table 43.

Table 43. Flash Page Select Register (FLASH_PAGE = 00FCh)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: R/W = Read/Write, R = Read Only.

Bit Position	Value	Description
[7] INFO_EN	0	Flash I/O access to PAGE ERASE operations are directed to main Flash memory. Info page is NOT affected by a MASS ERASE operation.
	1	Flash I/O access to PAGE ERASE operations are directed to the information page. PAGE ERASE operations only affect the information page. Info page is included during a MASS ERASE operation.
[6:0] FLASH_PAGE	00h–7Fh	Page address of Flash memory to be used during the PAGE ERASE or I/O access of main Flash memory. When INFO_EN is set to 1, this field is ignored.

Watchdog Timer Operation

Enabling and Disabling the Watchdog Timer

The WDT is disabled on a RESET. To enable the WDT, the application program must set WDT_EN, which is bit 7 of the WDT_CTL register. After WDT_EN is set, no Writes are allowed to the WDT_CTL register. When enabled, the WDT cannot be disabled except by a RESET.

Time-Out Period Selection

There are four choices of time-out periods for the WDT. The WDT time-out period is defined by the WDT_PERIOD WDT_CTL[1:0] field and WDT_CLK WDT_CTL[3:2] field of the Watchdog Timer control register (WDT_CTL = 0093h). The approximate time-out period and corresponding clock cycles for three different WDT clock sources are listed in Table 47.

The WDT time-out period divider is set to one of the four available settings for the selected frequency of the WDT clock source. Basing the divider settings on the clock source values provides a time-out range from few seconds to few msecs, regardless of the frequency setting.

Table 47. WDT Approximate Time-Out Delays for Possible Clock Sources

WDT_CLK[3:2]	**00**		**01**		**10**		**11**	
	50 MHz system clock		32.768 kHz RTC clock		Internal RC oscillator (~10 kHz)		Reserved	
WDT_PERIOD[1:0]	Divider	Timeout	Divider	Timeout	Divider	Timeout	Divider	Timeout
00	2^{27}	2.68 s	2^{17}	4.00 s	2^{15}	3.28 s	-	-
01	2^{25}	0.67 s	2^{14}	0.5 s	2^{13}	0.82 s	-	-
10	2^{22}	83.9 ms	2^{11}	62.5 ms	2^{9}	51.2 ms	-	-
11	2^{18}	5.2 ms	2^{7}	3.9 ms	2^{5}	3.2 ms	-	-

RESET or NMI Generation

A WDT time-out causes a RESET or sends a NMI signal to the CPU. The default operation is for the WDT to cause a RESET.

If the NMI_OUT bit in the WDT_CTL register is set to 0, then on a WDT time-out, the RST_FLAG bit in the WDT_CTL register is set to 1. The RST_FLAG bit is polled by the CPU to determine the source of the RESET event.

2 IRQ_ICB_EN	0	Interrupt requests for ICx are disabled (valid only in INPUT CAPTURE mode). Timer 1: the capture pin is IC1. Timer 3: the capture pin is IC3.
	1	Interrupt requests for ICx are enabled (valid only in INPUT CAPTURE mode). For Timer 1: the capture pin is IC1. For Timer 3: the capture pin is IC3.
1 IRQ_ICA_EN	0	Interrupt requests for ICA or PWM power trip are disabled (valid only in INPUT CAPTURE and PWM modes). For Timer 1: the capture pin is IC0. For Timer 3: the capture pin is IC2.
	1	Interrupt requests for ICA or PWM power trip are enabled (valid only in INPUT CAPTURE and PWM modes). For Timer 1: the capture pin is IC0. For Timer 3: the capture pin is IC2.
0 IRQ_EOC_EN	0	Interrupt on end-of-count is disabled.
	1	Interrupt on end-of-count is enabled.

Pulse-Width Modulation Control Register 2

The PWM Control Register 2 (see Table 74) controls pulse-width modulation AND/OR and edge delay functions.

Table 74. PWM Control Register 2 (PWM_CTL2 = 007Ah)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: R/W = Read/Write.

Bit Position	Value	Description
[7:6] AON_EN	00	Disable AND/OR features on $\overline{PWM}$
	01	Enable AND logic on $\overline{PWM}$
	10	Enable OR logic on $\overline{PWM}$
	11	Disable AND/OR features on $\overline{PWM}$
[5:4] AO_EN	00	Disable AND/OR features on PWM
	01	Enable AND logic on PWM
	10	Enable OR logic on PWM
	11	Disable AND/OR features on PWM

Real-Time Clock Month Register

This register contains the current month count. The RTC_MON register begins counting at 01h. The value in the RTC_MON register is unchanged by a RESET. The current setting of BCD_EN determines whether the values in this register are binary (BCD_EN = 0) or binary-coded decimal (BCD_EN = 1). Access to this register is Read Only if the RTC is locked, and Read/Write if the RTC is unlocked. See Table 85.

Table 85. Real-Time Clock Month Register (RTC_MON = 00E5h)

Bit	7	6	5	4	3	2	1	0
Reset	X	X	X	X	X	X	X	X
CPU Access	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*

Note: X = Unchanged by RESET; R/W* = Read Only if RTC locked, Read/Write if RTC unlocked.

Binary-Coded Decimal Operation (BCD_EN = 1)

Bit Position	Value	Description
[7:4] TENS_MON	0–1	The tens digit of the current month count.
[3:0] MON	0–9	The ones digit of the current month count.

Binary Operation (BCD_EN = 0)

Bit Position	Value	Description
[7:0] MON	01h–0Ch	The current month count.

Real-Time Clock Alarm Seconds Register

This register contains the alarm seconds value. The value in the RTC_ASEC register is unchanged by a RESET. The current setting of BCD_EN determines whether the values in this register are binary (BCD_EN = 0) or binary-coded decimal (BCD_EN = 1). See Table 88.

Table 88. Real-Time Clock Alarm Seconds Register (RTC_ASEC = 00E8h)

Bit	7	6	5	4	3	2	1	0
Reset	X	X	X	X	X	X	X	X
CPU Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: X = Unchanged by RESET; R/W = Read/Write.

Binary-Coded Decimal Operation (BCD_EN = 1)		
Bit Position	**Value**	**Description**
[7:4] ATEN_SEC	0–5	The tens digit of the alarm seconds value.
[3:0] ASEC	0–9	The ones digit of the alarm seconds value.

Binary Operation (BCD_EN = 0)		
Bit Position	**Value**	**Description**
[7:0] ASEC	00h–3Bh	The alarm seconds value.

Universal Asynchronous Receiver/Transmitter

The UART module implements all of the logic required to support the asynchronous communications protocol. The module also implements two separate 16-byte-deep FIFOs for both transmission and reception. A block diagram of the UART is displayed in Figure 36.

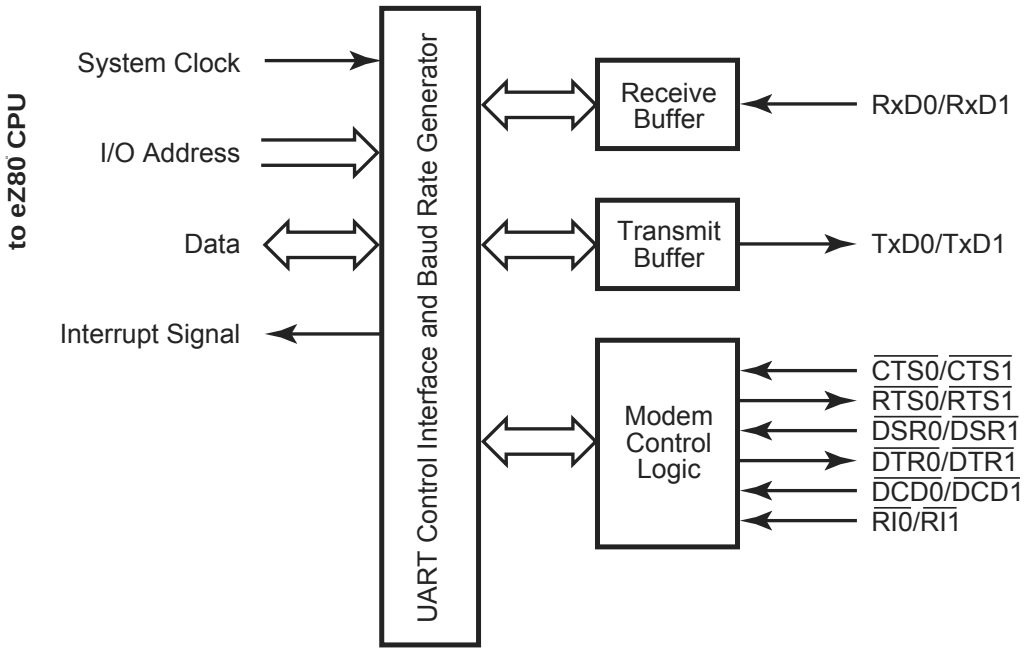

Figure 36. UART Block Diagram

The UART module provides the following asynchronous communications protocol-related features and functions:

- 5-, 6-, 7-, 8- or 9-bit data transmission.
- Even/odd, space/mark, address/data, or no parity bit generation and detection.
- Start and stop bit generation and detection (supports up to two stop bits).
- Line break detection and generation.
- Receiver overrun and framing errors detection.
- Logic and associated I/O to provide modem handshake capability.

Table 96. UART Transmit Holding Registers (UART0_THR = 00C0h, UART1_THR = 00D0h)

Bit	7	6	5	4	3	2	1	0
Reset	X	X	X	X	X	X	X	X
CPU Access	W	W	W	W	W	W	W	W

Note: W = Write Only.

Bit Position	Value	Description
[7:0] TxD	00h–FFh	Transmit data byte.

UART Receive Buffer Register

The bits in this register reflect the data received. If less than eight bits are programmed for reception, the lower bits of the byte reflect the bits received, whereas upper unused bits are 0. The Receive FIFO is mapped at this address. If the FIFO is disabled, this buffer is only one byte deep.

These registers share the same address space as the UARTx_THR and UARTx_BRG_L registers. See Table 97.

Table 97. UART Receive Buffer Registers (UART0_RBR = 00C0h, UART1_RBR = 00D0h)

Bit	7	6	5	4	3	2	1	0
Reset	X	X	X	X	X	X	X	X
CPU Access	R	R	R	R	R	R	R	R

Note: R = Read only.

Bit Position	Value	Description
[7:0] RxD	00h–FFh	Receive data byte.

UART Interrupt Enable Register

The UARTx_IER register is used to enable and disable the UART interrupts. The UARTx_IER registers share the same I/O addresses as the UARTx_BRG_H registers. See Table 98 on page 185.

Table 112. SPI Baud Rate Generator Register—Low Byte (SPI_BRG_L = 00B8h)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	1	0
CPU Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: R/W = Read/Write.

Bit Position	Value	Description
[7:0] SPI_BRG_L	00h–FFh	These bits represent the Low byte of the 16-bit BRG divider value. The complete BRG divisor value is returned by {SPI_BRG_H, SPI_BRG_L}.

Table 113. SPI Baud Rate Generator Register—High Byte (SPI_BRG_H = 00B9h)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: R/W = Read/Write.

Bit Position	Value	Description
[7:0] SPI_BRG_H	00h–FFh	These bits represent the High byte of the 16-bit BRG divider value. The complete BRG divisor value is returned by {SPI_BRG_H, SPI_BRG_L}.

Address Information for ZDI Address Match Registers

ZDI_ADDR0_L = 00h, ZDI_ADDR0_H = 01h, ZDI_ADDR0_U = 02h, ZDI_ADDR1_L = 04h, ZDI_ADDR1_H = 05h, ZDI_ADDR1_U = 06h, ZDI_ADDR2_L = 08h, ZDI_ADDR2_H = 09h, ZDI_ADDR2_U = 0Ah, ZDI_ADDR3_L = 0Ch, ZDI_ADDR3_H = 0Dh, and ZDI_ADDR3_U = 0Eh in the ZDI Register Write Only Address Space.

ZDI Break Control Register

The ZDI Break Control register is used to enable break points. ZDI asserts a break when the CPU instruction address, ADDR[23:0], matches the value in the ZDI Address Match 3 registers, {ZDI_ADDR3_U, ZDI_ADDR3_H, ZDI_ADDR3_L}. BREAKs occurs only on an instruction boundary. If the instruction address is not the beginning of an instruction (that is, for multibyte instructions), then the break occurs at the end of the current instruction. The brk_next bit is set to 1. The brk_next bit must be reset to 0 to release the break. See Table 136 on page 243.

Power Requirement to the Phase-Locked Loop Function

Regardless of whether or not you chooses to use the PLL module block as a clock source for the eZ80F91 device, the PLL_V_{DD} (pin 87) must be connected to a V_{DD} supply and the PLL_V_{SS} (pin 84) must be connected to a V_{SS} supply for proper operation of the eZ80F91 using any system clock source.

PLL Registers

PLL Divider Control Register—Low and High Bytes

This register is designed such that the 11 bit divider value is loaded into the divider module whenever the PLL_DIV_H register is written. Therefore, the procedure must be to load the PLL_DIV_L register, followed by the PLL_DIV_H register, for the divider to receive the appropriate value.

The divider is designed such that any divider value less than two is ignored; a value of two is used in its place.

The LSB of PLL divider N is set via the corresponding bits in the PLL_DIV_L register. See Table 152 and Table 153 on page 269.

Note: *The PLL divider register are written only when the PLL is disabled. A read-back of the PLL Divider registers returns 0.*

Table 152. PLL Divider Register—Low Bytes (PLL_DIV_L = 005Ch)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	1	0
CPU Access	W	W	W	W	W	W	W	W

Note: W = Write only.

Bit Position	Value	Description
[7:0] PLL_DIV_L	00h–FFh	These bits represent the Low byte of the 11 bit PLL divider value. The complete PLL divider value is returned by {PLL_DIV_H, PLL_DIV_L}.

Table 174. Arbiter Priority

Priority Level	Device Serviced	Flags
0	RxDMA High	RxFIFO > half full (FAF)
1	TxDMA High	TxFIFO < half full (FAE)
2	eZ80® CPU	
3	RxDMA Low	RxFIFO < half full (FAE)
4	TxDMA Low	TxFIFO > half full (FAF)

TxDMA

The TxDMA module moves the next packet to be transmitted from EMAC memory into the TxFIFO. Whenever the polling timer expires, the TxDMA reads the High status byte from the Tx descriptor table pointed to by the Transmit Read Pointer, TRP. Polling continues until the High status Read reaches bit 7, when the Emac_Owns ownership semaphore, bit 15 of the descriptor table (see Table 178 on page 295) is set to 1. The TxDMA then initializes the packet length counter with the size of the packet from descriptor table bytes 3 and 4. The TxDMA moves the data into the TxFIFO until the packet length counter downcounts to zero. The TxDMA then waits for Transmission Complete signal to be asserted to indicate that the packet is sent and that the Transmit status from the EMAC is valid. The TxDMA updates the descriptor table status and resets the ownership semaphore, bit 15. Finally, the Tx_DONE_STAT bit of the EMAC Interrupt Status Register is set to 1, the address field, DMA_Address, is updated from the descriptor table next pointer, NP (see Figure 62 on page 294). The High byte of the status is read to determine if the next packet is ready to be transmitted.

While the TxDMA is filling the TxFIFO, it monitors two signals from the Transmit FIFO State Machine (TxFifoSM) to detect error conditions and to determine if the packet is to be retransmitted (TxDMA_Retry asserted) or the packet is aborted (TxDMA_Abort asserted). If the packet is aborted, the TxDMA updates the descriptor status and moves to the next packet. If the packet is to be retried, the DMA_Address is reset to the start of the packet, the packet length counter is reloaded from the descriptor table, bytes 3 and 4, and the packet is moved into the TxFIFO again. When an abort or retry event occurs, the TxDMA asserts the appropriate signal to reset the TxFIFO Read and Write pointers which clears out any data that is in the FIFO. The TxFifoSM negates the TxDMA_Abort or TxDMA_Retry signal(s) or both when the TxFCWP signal is High. This handshaking maintains synchronization between the TxDMA and the TxFifoSM.

RxDMA

The RxDMA reads the data from the RxFIFO and stores it in the EMAC memory Receive buffer. When the end of the packet is detected, the RxDMA reads the next two bytes from

VLAN Packet— Maximum frame size = VLAN with 4 byte header – 4 (VLAN header) + 14 (Ethernet header) + 1500 MAC client data) + 4 (CRC) = 1522 bytes.

Table 194. EMAC Maximum Frame Length Register—Low Byte (EMAC_MAXF_L = 0030h

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: R/W = Read/Write.

Bit Position	Value	Description
[7:0] EMAC_MAXF_L	00h–FFh	These bits represent the Low byte of the 2 byte MAXF value, {EMAC_MAXF_H, EMAC_MAXF_L}. Bit 7 is bit 7 of the 16-bit value. Bit 0 is bit 0 (lsb) of the 16-bit value.

Table 195. EMAC Maximum Frame Length Register—High Byte (EMAC_MAXF_H = 0031h)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	1	1	0
CPU Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: R/W = Read/Write.

Bit Position	Value	Description
[7:0] EMAC_MAXF_H	00h–FFh	These bits represent the High byte of the 2 byte MAXF value, {EMAC_MAXF_H, EMAC_MAXF_L}. Bit 7 is bit 15 (msb) of the 16-bit value. Bit 0 is bit 8 of the 16-bit value.

Table 214. EMAC Buffer Size Register (EMAC_BUFSZ = 004Bh)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: R/W = Read/Write.

Bit Position	Value	Description
[7:6] BUFSZ	00	Set EMAC Rx/Tx buffer size to 256 bytes.
	01	Set EMAC Rx/Tx buffer size to 128 bytes.
	10	Set EMAC Rx/Tx buffer size to 64 bytes.
	11	Set EMAC Rx/Tx buffer size to 32 bytes.
[5:0] TPCF_LEV	00h–3Fh	Transmit Pause Control Frame level. 00h disables the hardware generated transmit pause control frame.

EMAC Interrupt Enable Register

Enabling the Receive Overrun interrupt allows software to detect an overrun condition as soon as it occurs. If this interrupt is not set, then an overrun cannot be detected until the software processes the Receive packet with the overrun and checks the Receive status in the Rx descriptor table. Because the receiver is disabled by an overrun error until the Rx_OVR bit is cleared in the EMAC_ISTAT register, this packet is the final packet in the Receive buffer. To re-enable the receiver before all of the Receive packets are processed and the Receive buffer is empty, software enables this interrupt to detect the overrun condition early. As it processes the Receive packets, it re-enables the receiver when the number of free buffers is greater than the number of minimum buffers. See Table 215 on page 324.

Bit Position	Value	Description
1 Tx_CF_STAT	1	Transmit Control Frame Interrupt (Transmit Interrupt) occurs.
	0	Transmit Control Frame Interrupt (Transmit Interrupt) does not occur.
0 Tx_DONE_STAT	1	Transmit Done interrupt (Transmit Interrupt) occurs.
	0	Transmit Done interrupt (Transmit Interrupt) does not occur.

EMAC PHY Read Status Data Register—Low and High Bytes

The PHY MII Management Data Register is where the data Read from the PHY is stored. See Table 217 and Table 218 on page 327.

Table 217. EMAC PHY Read Status Data Register—Low Byte (EMAC_PRSD_L = 004Eh)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	R	R	R	R	R	R	R	R

Note: R = Read Only.

Bit Position	Value	Description
[7:0] EMAC_PRSD_L	00h–FFh	These bits represent the Low byte of the 2 byte EMAC PHY Read Status Data value, {EMAC_PRSD_H, EMAC_PRSD_L}. Bit 7 is bit 7 of the 16 bit value. Bit 0 is bit 0 (lsb) of the 16 bit value.

Figure 67 displays the typical current consumption of the eZ80F91 device versus Vdd while operating in SLEEP mode (units in microamps, 10^{-6}A); all peripherals off, and VBO disabled.

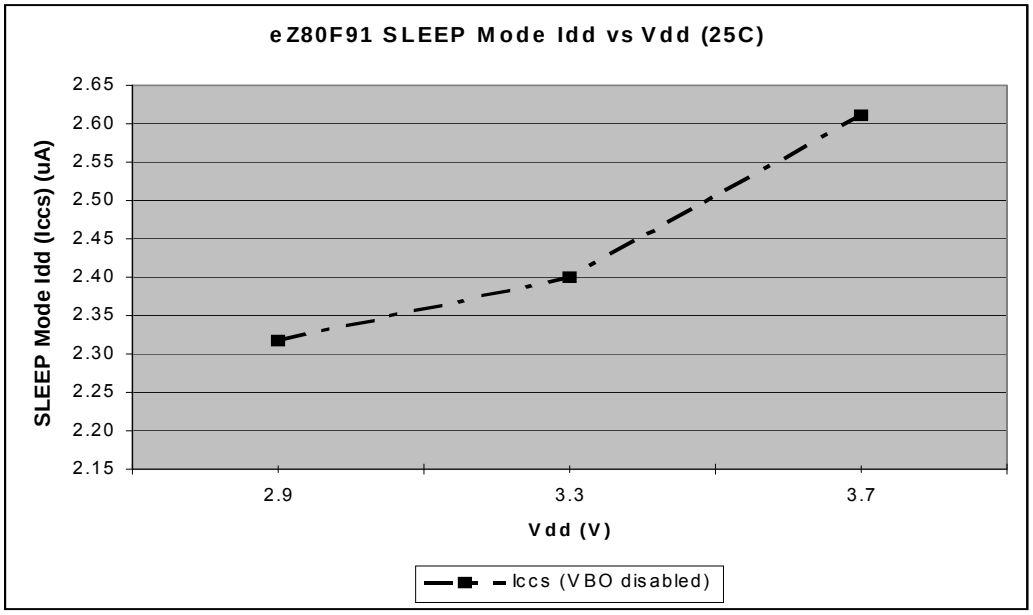

Figure 67. I_{CC} vs. Vdd During SLEEP Mode

AC Characteristics

This section provides information about the AC characteristics and timing of the eZ80F91 device. All AC timing information assumes a standard load of 50 pF on all outputs. See Table 236.

Table 236. AC Characteristics

		T_A = 0 ºC to 70 ºC		T_A = –40 ºC to 105 ºC			
Symbol	**Parameter**	**Minimum**	**Maximum**	**Minimum**	**Maximum**	**Units**	**Conditions**
T_{XIN}	System Clock Cycle Time	20	1000	20	1000	ns	V_{DD} = 3.0–3.6 V
T_{XINH}	System Clock High Time	8		8		ns	V_{DD} = 3.0–3.6 V; T_{CLK} = 20 ns
T_{XINL}	System Clock Low Time	8		8		ns	V_{DD} = 3.0–3.6 V; T_{CLK} = 20 ns