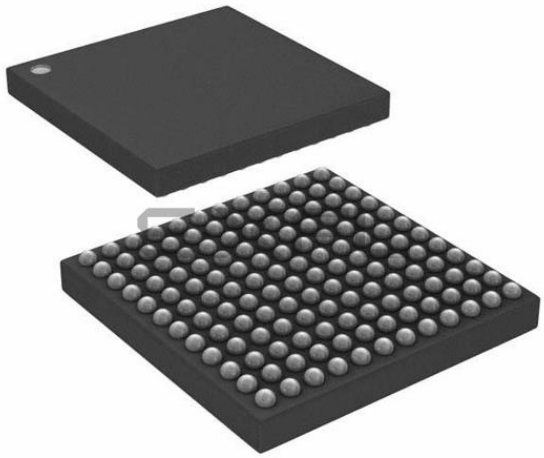

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	eZ80
Core Size	8-Bit
Speed	50MHz
Connectivity	Ethernet, I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	32
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LBGA
Supplier Device Package	144-BGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/ez80f91na050eg

Pin Description

Table 1 lists the pin configuration of the eZ80F91 device in the 144-BGA package.

Table 1. eZ80F91 144-BGA Pin Configuration

	12	11	10	9	8	7	6	5	4	3	2	1
A	SDA	SCL	PA0	PA4	PA7	COL	TxD0	V_{DD}	Rx_DV	MDC	WPn	A0
B	V_{SS}	PHI	PA1	PA3	V_{DD}	TxD3	Tx_EN	V_{SS}	RxD1	MDIO	A2	A1
C	PB6	PB7	V_{DD}	PA5	V_{SS}	TxD2	Tx_CLK	Rx_ CLK	RxD3	A3	V_{SS}	V_{DD}
D	PB1	PB3	PB5	V_{SS}	CRS	TxD1	Rx_ER	RxD2	A4	A8	A6	A7
E	PC7	V_{DD}	PB0	PB4	PA2	Tx_ER	RxD0	A5	A11	V_{SS}	V_{DD}	A10
F	PC3	PC4	PC5	V_{SS}	PB2	PA6	A9	A17	A15	A14	A13	A12
G	V_{SS}	PC0	PC1	PC2	PC6	PLL_ V_{SS}	V_{SS}	A23	A20	V_{SS}	V_{DD}	A16
H	X_{OUT}	X_{IN}	PLL_ V_{DD}	V_{DD}	PD7	TMS	V_{SS}	D5	V_{SS}	A21	A19	A18
J	V_{SS}	V_{DD}	LOOP FILT_ OUT	PD4	TRIGOUT	RTC_ V_{DD}	NMIn	WRn	D2	CS0n	V_{DD}	A22
K	PD5	PD6	PD3	TDI	V_{SS}	V_{DD}	RESETn	RDn	V_{DD}	D1	CS2n	CS1n
L	PD1	PD2	TRSTn	TCK	RTC_ XOUT	BUSACKn	WAITn	MREQn	D6	D4	D0	CS3n
M	PD0	V_{SS}	TDO	HALT _ SLPn	RTC_ XIN	BUSREQn	INSTRDn	IORQn	D7	D3	V_{SS}	V_{DD}

Note: Lowercase n suffix indicates an active-low signal in this table only

Table 2. Pin Identification on the eZ80F91 Device (Continued)

LQFP Pin No	BGA Pin No	Symbol	Function	Signal Direction	Description
92	G9	PC2	GPIO Port C	Bidirectional with Schmitt-trigger input	This pin is used for GPIO. It is individually programmed as input or output and is also used individually as an interrupt input. Each Port C pin, when programmed as output is selected to be an open-drain or open-source output. Port C is multiplexed with one UART.
		RTS1	Request to Send	Output, Active Low	Modem control signal from UART. This signal is multiplexed with PC2.
93	F12	PC3	GPIO Port C	Bidirectional with Schmitt-trigger input	This pin is used for GPIO. It is individually programmed as input or output and is also used individually as an interrupt input. Each Port C pin, when programmed as output is selected to be an open-drain or open-source output. Port C is multiplexed with one UART.
		CTS1	Clear to Send	Schmitt-trigger input, Active Low	Modem status signal to the UART. This signal is multiplexed with PC3.
94	F11	PC4	GPIO Port C	Bidirectional with Schmitt-trigger input	This pin is used for GPIO. It is individually programmed as input or output and is also used individually as an interrupt input. Each Port C pin, when programmed as output is selected to be an open-drain or open-source output. Port C is multiplexed with one UART.
		DTR1	Data Terminal Ready	Output, Active Low	Modem control signal to the UART. This signal is multiplexed with PC4.

PLL Clock—The eZ80F91 internal PLL driven by external crystals or external crystal oscillators in the range of 1 MHz to 10 MHz generates an SCLK up to 50 MHz. For more-details, see Phase-Locked Loop on page 265.

SCLK Source Selection Example

For additional SCLK source selection examples, refer to *Crystal Oscillator/Resonator Guidelines for eZ80® and eZ80Acclaim!® Devices Technical Note (TN0013)* available on www.zilog.com.

Table 3. Register Map (Continued)

Address (hex)	Mnemonic	Name	Reset (hex)	CPU Access	Page No
0085	PWM0F_H	PWM 0 Falling-Edge Register—High Byte	XX	R/W	158
	TMR3_OC1_H	Timer 3 Output Compare 1 Value Register—High Byte	XX	R/W	145
0086	PWM1F_L	PWM 1 Falling-Edge Register—Low Byte	XX	R/W	158
	TMR3_OC2_L	Timer 3 Output Compare 2 Value Register—Low Byte	XX	R/W	144
0087	PWM1F_H	PWM 1 Falling-Edge Register—High Byte	XX	R/W	158
	TMR3_OC2_H	Timer 3 Output Compare 2 Value Register—High Byte	XX	R/W	145
0088	PWM2F_L	PWM 2 Falling-Edge Register—Low Byte	XX	R/W	158
	TMR3_OC3_L	Timer 3 Output Compare 3 Value Register—Low Byte	XX	R/W	144
0089	PWM2F_H	PWM 2 Falling-Edge Register—High Byte	XX	R/W	158
	TMR3_OC3_H	Timer 3 Output Compare 3 Value Register—High Byte	XX	R/W	145
008A	PWM3F_L	PWM 3 Falling-Edge Register—Low Byte	XX	R/W	158
008B	PWM3F_H	PWM 3 Falling-Edge Register—High Byte	XX	R/W	158
Watchdog Timer					
0093	WDT_CTL	Watchdog Timer Control Register	08/28	R/W	117
0094	WDT_RR	Watchdog Timer Reset Register	XX	W	119
General-Purpose Input/Output Ports					
0096	PA_DR	Port A Data Register	XX	R/W	55
0097	PA_DDR	Port A Data Direction Register	FF	R/W	55
0098	PA_ALT1	Port A Alternate Register 1	00	R/W	56
0099	PA_ALT2	Port A Alternate Register 2	00	R/W	56

Table 42. Flash Interrupt Control Register (FLASH_IRQ = 00FBh)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	R/W	R/W	R	R	R	R	R	R

Note: R/W = Read/Write, R = Read Only. Read resets bits [5] and [3:0].

Bit Position	Value	Description
[7] DONE_IEN	0	Flash Erase/Row Program Done Interrupt is disabled.
	1	Flash Erase/Row Program Done Interrupt is enabled.
[6] ERR_IEN	0	Error Condition Interrupt is disabled.
	1	Error Condition Interrupt is enabled.
[5] DONE	0	Erase/Row Program Done Flag is not set.
	1	Erase/Row Program Done Flag is set.
[4]	0	Reserved.
[3] WR_VIO	0	The Write Violation Error Flag is not set.
	1	The Write Violation Error Flag is set.
[2] RP_TMO	0	The Row Program Time-Out Error Flag is not set.
	1	The Row Program Time-Out Error Flag is set.
[1] PG_VIO	0	The Page Erase Violation Error Flag is not set.
	1	The Page Erase Violation Error Flag is set.
[0] MASS_VIO	0	The Mass Erase Violation Error Flag is not set.
	1	The Mass Erase Violation Error Flag is set.

Note: The lower 32 KB block (00000h to 07FFFh) is called the Boot Block and is protected using the external $\overline{WP}$ pin. Attempts to page erase BLK0 or mass erase Flash when $\overline{WP}$ is asserted result in failure and signal an erase violation.

Flash Page Select Register

The msb of this register is used to select whether I/O Flash access and PAGE ERASE operations are directed to the 512-byte information page or to the main Flash memory array, and also whether the information page is included in MASS ERASE operations. The lower 7 bits are used to select one of the main 128 pages for PAGE ERASE or I/O operations.

To perform a PAGE ERASE, the software must set the proper page value prior to setting the page erase bit in the Flash Control Register. In addition, each access to the

Timer Data Register—Low Byte

The Timer x Data Register—Low Byte returns the Low byte of the current count value of the selected timer. The Timer Data Register—Low Byte (see Table 57) is read when the timer is in operation. Reading the current count value does not affect timer operation. To read the 16-bit data of the current count value, {TMR*x*_DR_H[7:0], TMR*x*_DR_L[7:0]}, first read the Timer Data Register—Low Byte, followed by the Timer Data Register—High Byte. The Timer Data Register—High Byte value is latched into temporary storage when a Read of the Timer Data Register—Low Byte occurs.

This register shares its address with the corresponding timer reload register.

Table 57. Timer Data Register—Low Byte (TMR0_DR_L = 0063h, TMR1_DR_L = 0068h, TMR2_DR_L = 0072h, TMR3_DR_L = 0077h)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	R	R	R	R	R	R	R	R

Note: R = Read only.

Bit Position	Value	Description
[7:0] TMR_DR_L	00h–FFh	These bits represent the Low byte of the 2-byte timer data value, {TMR*x*_DR_H[7:0], TMR*x*_DR_L[7:0]}. Bit 7 is bit 7 of the 16-bit timer data value. Bit 0 is bit 0 (lsb) of the 16-bit timer data value.

The inverted PWM outputs $\overline{\text{PWM0}}$, $\overline{\text{PWM1}}$, $\overline{\text{PWM2}}$, and $\overline{\text{PWM3}}$ are globally enabled by setting TMR3_PWM_CTL1[PAIR_EN] to 1. The individual PWM generators must be enabled for the associated inverted PWM signals to be output.

For each of the 4 PWM generators, there is a 16-bit rising edge value {TMR3_PWM*x*R_H[PWMxR_H], TMR3_PWM*x*R_L[PWMxR_L]} and a 16-bit falling edge value {TMR3_PWM*x*F_H[PWMxF_H], TMR3_PWM*x*F_L[PWMxF_L]} for a total of 16 registers. The rising-edge byte pairs define the timer count at which the PWM*x* output transitions from Low to High. Conversely, the falling-edge byte pairs define the timer count at which the PWM*x* output transitions from High to Low. On reset, all enabled PWM outputs begin Low and all $\overline{\text{PWMx}}$ outputs begin High. When the PWMx output is Low, the logic is looking for a match between the timer count and the rising edge value, and vice versa. Therefore, in a case in which the rising edge value is the same as the falling edge value, the PWM output frequency is one-half the rate at which the counter passes through its entire count cycle (from reload value down to 0000h).

Figure 31and Figure 32 display a simple Multi-PWM output and an expanded view of the timing, respectively. Associated control values are listed in Table 71 on page 148.

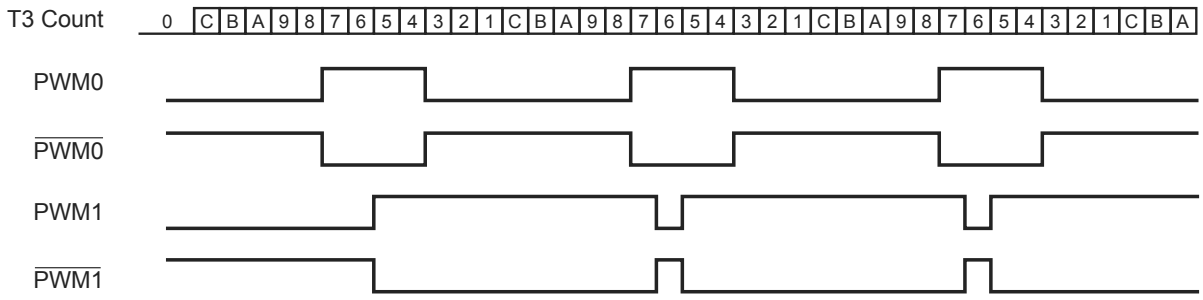

Figure 31. Multi-PWM Operation

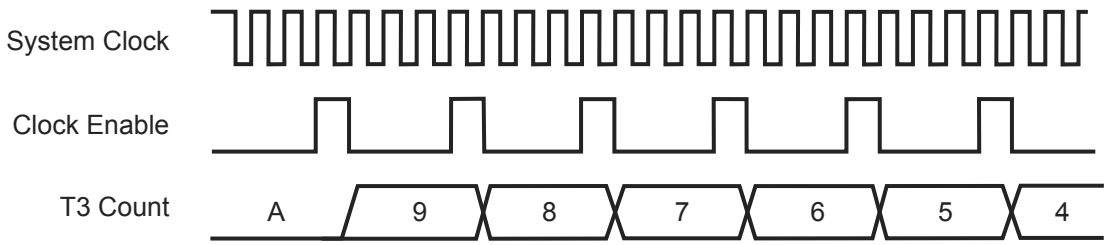

Figure 32. Multi-PWM Operation—Expanded View of Timing

Pulse-Width Modulation Control Register 2

The PWM Control Register 2 (see Table 74) controls pulse-width modulation AND/OR and edge delay functions.

Table 74. PWM Control Register 2 (PWM_CTL2 = 007Ah)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: R/W = Read/Write.

Bit Position	Value	Description
[7:6] AON_EN	00	Disable AND/OR features on $\overline{PWM}$
	01	Enable AND logic on $\overline{PWM}$
	10	Enable OR logic on $\overline{PWM}$
	11	Disable AND/OR features on $\overline{PWM}$
[5:4] AO_EN	00	Disable AND/OR features on PWM
	01	Enable AND logic on PWM
	10	Enable OR logic on PWM
	11	Disable AND/OR features on PWM

Real-Time Clock Year Register

This register contains the current year count. The value in the RTC_YR register is unchanged by a RESET. The current setting of BCD_EN determines whether the values in this register are binary (BCD_EN = 0) or binary-coded decimal (BCD_EN = 1). Access to this register is Read Only if the RTC is locked, and Read/Write if the RTC is unlocked. See Table 86.

Table 86. Real-Time Clock Year Register (RTC_YR = 00E6h)

Bit	7	6	5	4	3	2	1	0
Reset	X	X	X	X	X	X	X	X
CPU Access	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*

Note: X = Unchanged by RESET; R/W* = Read Only if RTC locked, Read/Write if RTC unlocked.

Binary-Coded Decimal Operation (BCD_EN = 1)

Bit Position	Value	Description
[7:4] TENS_YR	0–9	The tens digit of the current year count.
[3:0] YR	0–9	The ones digit of the current year count.

Binary Operation (BCD_EN = 0)

Bit Position	Value	Description
[7:0] YR	00h–63h	The current year count.

Table 95. UART Baud Rate Generator Register—High Bytes (UART0_BRG_H = 00C1h, UART1_BRG_H = 00D1h)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: R = Read only; R/W = Read/Write.

Bit Position	Value	Description
[7:0] UART_BRG_H	00h–FFh	These bits represent the High byte of the 16-bit BRG divider value. The complete BRG divisor value is returned by {UART_BRG_H, UART_BRG_L}.

UART Registers

After a system reset, all UART registers are set to their default values. Any Writes to unused registers or register bits are ignored and reads return a value of 0. For compatibility with future revisions, unused bits within a register must always be written with a value of 0. Read/Write attributes, reset conditions, and bit descriptions of all of the UART registers are provided in this section.

UART Transmit Holding Register

If less than eight bits are programmed for transmission, the lower bits of the byte written to this register are selected for transmission. The Transmit FIFO is mapped at this address. You can write up to 16 bytes for transmission at one time to this address if the FIFO is enabled by the application. If the FIFO is disabled, this buffer is only one byte deep.

These registers share the same address space as the UARTx_RBR and UARTx_BRG_L registers. See Table 96 on page 184.

UART FIFO Control Register

This register is used to monitor trigger levels, clear FIFO pointers, and enable or disable the FIFO. The UARTx_FCTL registers share the same I/O addresses as the UARTx_IIR registers. See Table 101.

Table 101. UART FIFO Control Registers (UART0_FCTL = 00C2h, UART1_FCTL = 00D2h)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	W	W	W	W	W	W	W	W

Note: W = Write Only.

Bit Position	Value	Description
[7:6] TRIG	00	Receive FIFO trigger level set to 1. Receive data interrupt is generated when there is 1 byte in the FIFO. Valid only if FIFO is enabled.
	01	Receive FIFO trigger level set to 4. Receive data interrupt is generated when there are 4bytes in the FIFO. Valid only if FIFO is enabled.
	10	Receive FIFO trigger level set to 8. Receive data interrupt is generated when there are 8 bytes in the FIFO. Valid only if FIFO is enabled.
	11	Receive FIFO trigger level set to 14. Receive data interrupt is generated when there are 14 bytes in the FIFO. Valid only if FIFO is enabled.
[5:3]	000b	Reserved—must be 000b.
2 CLRTxF	0	Transmit Disable. This register bit works differently than the standard 16550 UART. This bit must be set to transmit data. When it is reset the transmit FIFO logic is reset along with the associated transmit logic to keep them in sync. This bit is now persistent–it does not self clear and it must remain at 1 to transmit data.
	1	Transmit Enable.
1 CLRRxF	0	Receive Disable. This register bit works differently than the standard 16550 UART. This bit must be set to receive data. When it is reset the receive FIFO logic is reset along with the associated receive logic to keep them in sync and avoid the previous version's lookup problem. This bit is now persistent–it does not self clear and it must remain at 1 to receive data.
	1	Receive Enable.

period. If the data to be received is a logical 0, a delayed Low (0) pulse is output on RxD. Data transmission is displayed in Figure 39.

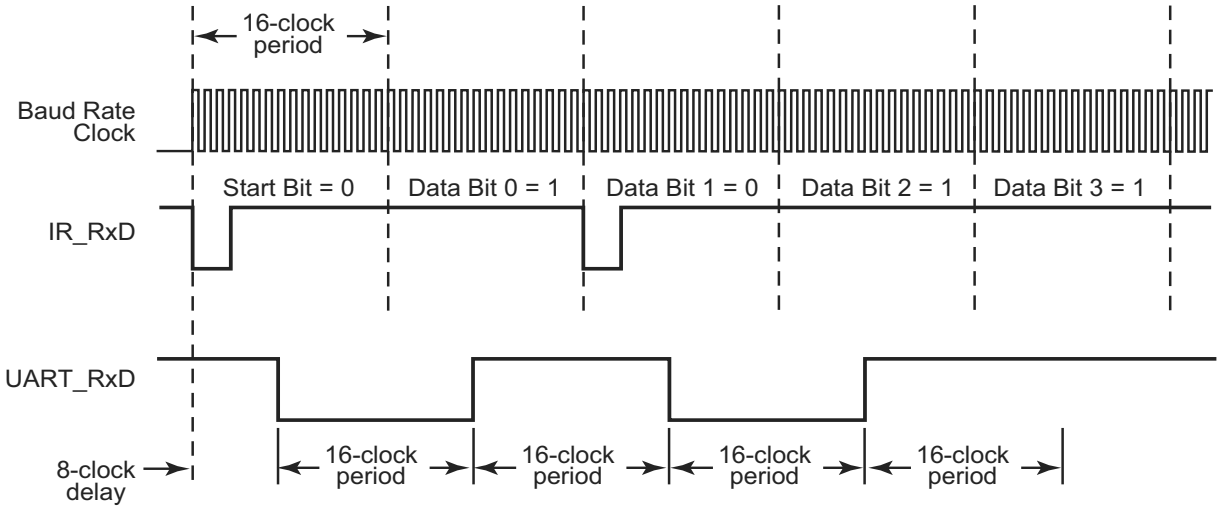

Figure 39. Infrared Data Reception

The IrDA endec is designed to ignore pulses on IR_RxD which do not comply with IrDA pulse width specifications. Input pulses wider than five baud clocks (that is, 5/16 of a bit period) are always ignored, as this would be a violation of the maximum pulse width specified for any standard baud rate up to 115.2 kbps. The check for minimum pulse widths is optional, since using a slow system clock frequency limits the ability to accurately measure narrow pulse widths near the IrDA specification minimum of 1.41 us for the 2.4–115.2 kbps rate range.

To enable checks of minimum input pulse width on IR_RxD, a non-zero value must be programmed into the MIN_PULSE field of IR_CTL (bits [7:4]). This field forms the most-significant four bits of the 6-bit down-counter used to determine if an input pulse will be ignored because it is too narrow. The lower two counter bits are hard-coded to load with 0x3, resulting in a total down-count equal to ((MIN_PULSE* 4) + 3). To be accepted, input pulses must have a width greater than or equal to the down-count value times the system clock period.

The following equation is used to determine an appropriate setting for MIN_PULSE:

$MIN\_PULSE = INT(((F_{sys} * W_{min}) - 3) / 4)$

Where,

F_{sys} is the frequency of the system clock, and,

W_{min} is the minimum width of recognized input pulses.

ZDI allows reading and writing of most internal registers without disturbing the state of the machine. Reads and Writes to memory occurs as fast as the ZDI downloads and uploads data, with a maximum supported ZDI clock frequency of 0.4 times the eZ80F91 system clock frequency. Also, regardless of the ZDI clock frequency, the duration of the low-phase of the ZDI clock (that is, ZCL = 0) must be at least 1.25 times the system clock period.

For the description on how to enable the ZDI interface on the exit of RESET, see the OCI Activation on page 258.

Table 132. Recommend ZDI Clock versus System Clock Frequency

System Clock Frequency	ZDI Clock Frequency
3–10 MHz	1 MHz
8–16 MHz	2 MHz
12–24 MHz	4 MHz
20–50 MHz	8 MHz

ZDI-Supported Protocol

ZDI supports a bidirectional serial protocol. The protocol defines any device that sends data as the *transmitter* and any receiving device as the *receiver*. The device controlling the transfer is the *master* and the device being controlled is the *slave*. The master always initiates the data transfers and provides the clock for both receive and transmit operations. The ZDI block on the eZ80F91 device is considered a slave in all data transfers.

Figure 49 on page 233 displays the schematic for building a connector on a target board. This connector allows you to connect directly to the USB Smart Cable emulator using a six-pin header.

Table 134. ZDI Read Only Registers (Continued)

ZDI Address	ZDI Register Name	ZDI Register Function	Reset Value
03h	ZDI_STAT	Status Register	00h
10h	ZDI_RD_L	Read Memory Address Low Byte Register	XXh
11h	ZDI_RD_H	Read Memory Address High Byte Register	XXh
12h	ZDI_RD_U	Read Memory Address Upper Byte Register	XXh
17h	ZDI_BUS_STAT	Bus Status Register	00h
20h	ZDI_RD_MEM	Read Memory Data Value	XXh

ZDI Register Definitions

ZDI Address Match Registers

The four sets of address match registers are used for setting the addresses for generating break points. When the accompanying BRK_ADDRX bit is set in the ZDI Break Control register to enable the particular address match, the current eZ80F91 address is compared with the 3-byte address set, {ZDI_ADDRx_U, ZDI_ADDRx_H, and ZDI_ADDR_x_L}. If the CPU is operating in ADL mode, the address is supplied by ADDR[23:0]. If the CPU is operating in Z80® mode, the address is supplied by {MBASE[7:0], ADDR[15:0]}. If a match is found, ZDI issues a break to the eZ80F91 device placing the CPU in ZDI mode pending further instructions from the ZDI interface block. If the address is not the first op-code fetch, the ZDI break is executed at the end of the instruction in which it is executed. There are four sets of address match registers. They are used in conjunction with each other to break on branching instructions. See Table 135 on page 241.

Table 135. ZDI Address Match Registers

Bit	7	6	5	4	3	2	1	0
Reset	X	X	X	X	X	X	X	X
CPU Access	W	W	W	W	W	W	W	W

Note: W = Write Only.

Bit Position	Value	Description
[7:0] zdi_addrx_l, zdi_addrx_h, or zdi_addrx_u	00h–FFh	The four sets of ZDI address match registers are used for setting the addresses for generating break points. The 24 bit addresses are supplied by {ZDI_ADDRx_U, ZDI_ADDRx_H, ZDI_ADDRx_L, where *x* is 0, 1, 2, or 3.

ZDI Read Register Low, High, and Upper

The ZDI register Read Only address space offers Low, High, and Upper functions, which contain the value read by a Read operation from the ZDI Read/Write Control register (ZDI_RW_CTL). This data is valid only while in ZDI BREAK mode and only if the instruction is read by a request from the ZDI Read/Write Control register. See Table 147.

Table 147. ZDI Read Register Low, High, and Upper (ZDI_RD_L = 10h, ZDI_RD_H = 11h, and ZDI_RD_U = 12h in the ZDI Register Read Only Address Space)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	R	R	R	R	R	R	R	R

Note: R = Read Only.

Bit Position	Value	Description
[7:0] zdi_rd_l, zdi_rd_h, or zdi_rd_u	00h–FFh	Values read from the memory location as requested by the ZDI Read Control register during a ZDI Read operation. The 24-bit value is supplied by {ZDI_RD_U, ZDI_RD_H, ZDI_RD_L}.

Phase Frequency Detector

The Phase Frequency Detector (PFD) is a digital block. The two inputs are the reference clock (XTAL oscillator; see On-Chip Oscillators on page 335) and the PLL divider output. The two outputs drive the internal charge pump and represent the error (or difference) between the falling edges of the PFD inputs.

Charge Pump

The Charge Pump is an analog block that is driven by two digital inputs from the PFD that control its programmable current sources. The internal current source contains four programmable values: 1.5 mA, 1 mA, 500 µA, and 100 µA. These values are selected by PLL_CTRL1[7:6]. The selected current drive is sinked/sourced onto the loop-filter node according to the error (or difference) between the falling edges of the PFD inputs. Ideally, when the PLL is locked, there are no errors (error = 0) and no current is sourced/sinked onto the loop-filter node.

Voltage Controlled Oscillator

The Voltage Controlled Oscillator (VCO) is an analog block that exhibits an output frequency proportional to its input voltage. The VCO input is driven from the charge pump and filtered via the off-chip loop filter.

Loop Filter

The Loop Filter comprises off-chip passive components (usually 1 resistor and 2 capacitors) that filter/integrate charge from the internal charge pump. The filtered node also drives the VCO input, which creates a proportional frequency output. When PLL is not used, the Loop Filter pin must not be connected.

Divider

The Divider is a digital, programmable downcounter. The divider input is driven by the VCO. The divider output drives the PFD. The function of the Divider is to divide the frequency of its input signal by a programmable factor *N* and supply the result in its output.

MUX/CLK Sync

The MUX/CLK Sync is a digital, software-controllable multiplexer that selects between PLL or the XTAL oscillator as the system clock (SCLK). A PLL source is selected only after the PLL is *locked* (via the lock detect block) to allow glitch-free clock switching.

Lock Detect

The Lock Detect digital block analyzes the PFD output for a locked condition. The PLL block of the eZ80F91 device is considered locked when the error (or difference) between the reference clock and divided-down VCO is less than the minimum timing lock criteria

Power Requirement to the Phase-Locked Loop Function

Regardless of whether or not you chooses to use the PLL module block as a clock source for the eZ80F91 device, the PLL_V_{DD} (pin 87) must be connected to a V_{DD} supply and the PLL_V_{SS} (pin 84) must be connected to a V_{SS} supply for proper operation of the eZ80F91 using any system clock source.

PLL Registers

PLL Divider Control Register—Low and High Bytes

This register is designed such that the 11 bit divider value is loaded into the divider module whenever the PLL_DIV_H register is written. Therefore, the procedure must be to load the PLL_DIV_L register, followed by the PLL_DIV_H register, for the divider to receive the appropriate value.

The divider is designed such that any divider value less than two is ignored; a value of two is used in its place.

The LSB of PLL divider N is set via the corresponding bits in the PLL_DIV_L register. See Table 152 and Table 153 on page 269.

Note: *The PLL divider register are written only when the PLL is disabled. A read-back of the PLL Divider registers returns 0.*

Table 152. PLL Divider Register—Low Bytes (PLL_DIV_L = 005Ch)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	1	0
CPU Access	W	W	W	W	W	W	W	W

Note: W = Write only.

Bit Position	Value	Description
[7:0] PLL_DIV_L	00h–FFh	These bits represent the Low byte of the 11 bit PLL divider value. The complete PLL divider value is returned by {PLL_DIV_H, PLL_DIV_L}.

Ethernet Media Access Controller

The Ethernet Media Access Controller (EMAC) is a full-function 10/100 Mbps media access control module with a Media-Independent Interface (MII). When communicating with an external PHY device, the eZ80F91 MCU uses the MII to gain access to the Ethernet network.

Figure 59 displays the EMAC block diagram.

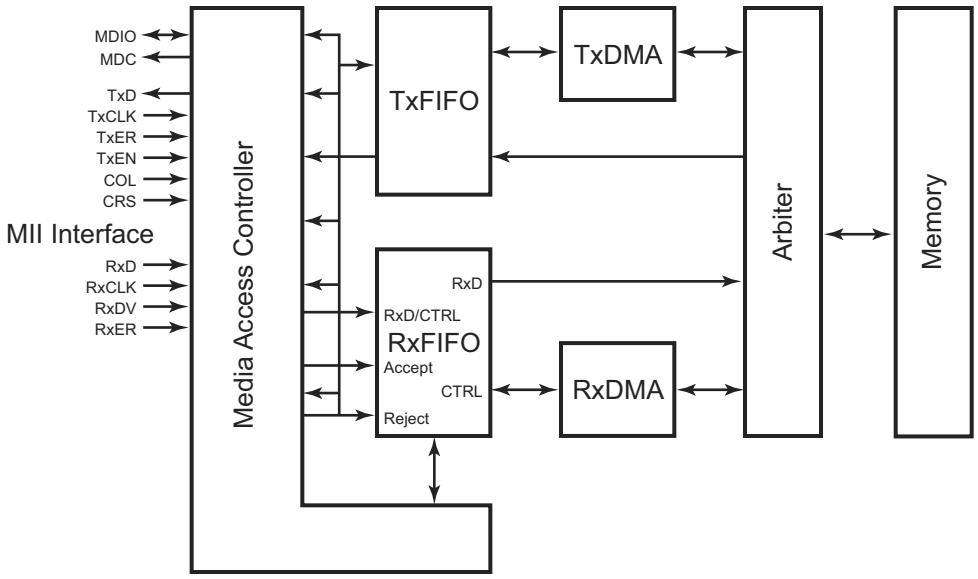

Figure 59. EMAC Block Diagram

Note: *For additional information about the Ethernet protocol and using it with the eZ80F91 MCU, refer to the IEEE 802.3 specification, 1998 edition, Section 22. The eZ80F91 MCU supports the IEEE 802.3 protocol with the following exception:*

The eZ80F91 MCU does not support the Giga Media Independent Interface (GMII) referred to in the following sections of the IEEE 802.3 1998 version: section 22.1.5, section 22.2.4, section 22.2.4.1.2, section 22.2.4.1.5, and section 22.2.4.1.6.

The EMAC is used for many different applications, including network interface, ethernet switching, and test equipment designs. The EMAC includes the following blocks:

- Central clock and reset module (not shown in the block diagram).
- Host memory interface and transmit/receiver arbiter.

the RxFIFO and writes them into the Rx descriptor status LSB and MSB. The packet-length counter is stored into the descriptor table's Packet Length field, and the descriptor table's next pointer is written into the Rx descriptor table. Additionally, the Rx_DONE_STAT bit in the EMAC Interrupt Status Register is set to 1.

Signal Termination

When the EMAC interface is not used, the MII signals must be terminated as listed in Table 175. Terminated pins are either left unconnected (float) or tied to ground.

MDIO is controlled by the MDC output signal. When the EMAC is not being used, these two pins are not driven. The RX_DV, RX_ER, and RXD[3:0] inputs are controlled by the rising edge of the RX_CLK input signal. When RX_CLK is tied to Ground, these pins do not affect the EMAC. The TX_EN, TX_ER, and TXD[3:0] outputs are controlled by the rising edge of the TX_CLK input signal. When TX_CLK is tied to Ground, these pins do not affect the EMAC. The CRS and COL input pins have no relationship to the clock, and therefore must be placed into nonactive states and tied to Ground.

Table 175. MII Signal Termination When EMAC is Not Used

Signal	Pin Type	Termination Direction
MDIO	Bidirectional	Float
MDC	Output pin	Float
RX_DV	Input pin	Float
CRS	Input pin	Ground
RX_CLK	Input pin	Ground
RX_ER	Input pin	Float
RXD[3:0]	Input pins	Float
COL	Input pin	Ground
TX_CLK	Input pin	Ground
TX_EN	Output pin	Float
TXD[3:0]	Output pins	Float
TX_ER	Output pin	Float

EMAC Reset Control Register

The bit values in the EMAC Reset Control Register are not self-clearing bits. You are responsible for controlling their state. See Table 204.

Table 204. EMAC Reset Control Register (EMAC_RST = 0041h)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	1	0	0	0	0	0
CPU Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Note: R = Read Only; R/W = Read/Write.

Bit Position	Value	Description
[7:6]	00	Reserved
5 SRST	1	Software Reset Active—resets Receive, Transmit, EMAC Control and EMAC MII_MGT functions
	0	Normal operation
4 HRTFN	1	Reset Transmit function
	0	Normal operation
3 HRRFN	1	Reset Receive function
	0	Normal operation
2 HRTMC	1	Reset EMAC Transmit Control function
	0	Normal operation
1 HRRMC	1	Reset EMAC Receive Control function
	0	Normal operation
0 HRMGT	1	Reset EMAC Management function
	0	Normal operation