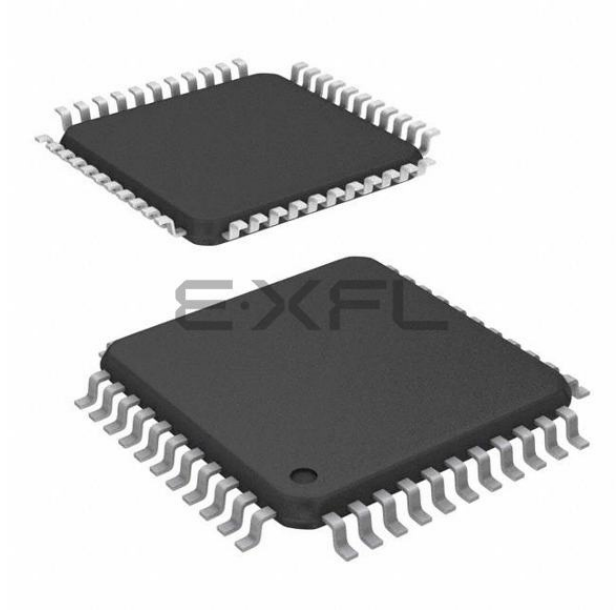

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	-
Number of Macrocells	32
Number of Gates	-
Number of I/O	30
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/la4032v-75tn44e

Table 2. LA-ispMACH 4000Z Automotive Family Selection Guide

	LA-ispMACH 4032Z	LA-ispMACH 4064Z	LA-ispMACH 4128Z
Macrocells	32	64	128
I/O + Dedicated Inputs	32+4	32+4/64+10	64+10
t_{PD} (ns)	7.5	7.5	7.5
t_S (ns)	4.5	4.5	4.5
t_{CO} (ns)	4.5	4.5	4.5
f_{MAX} (MHz)	168	168	168
Supply Voltage (V)	1.8V	1.8V	1.8V
Pins/Package	48-pin Lead-Free TQFP	48-pin Lead-Free TQFP 100-pin Lead-Free TQFP	100-pin Lead-Free TQFP

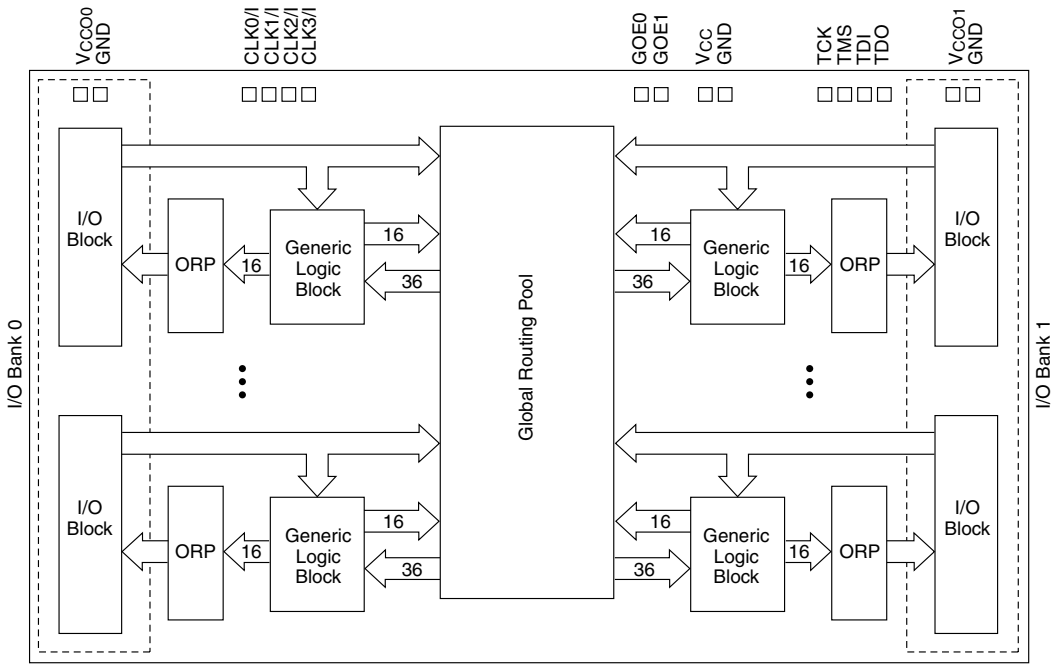
The LA-ispMACH 4000V/Z automotive family offers densities ranging from 32 to 128 macrocells. There are multiple density-I/O combinations in Thin Quad Flat Pack (TQFP) packages ranging from 44 to 144 pins. Tables 1 and 2 show the macrocell, package and I/O options, along with other key parameters.

The LA-ispMACH 4000V/Z automotive family has enhanced system integration capabilities. It supports 3.3V (4000V and 1.8V (4000Z) supply voltages and 3.3V, 2.5V and 1.8V interface voltages. Additionally, inputs can be safely driven up to 5.5V when an I/O bank is configured for 3.3V operation, making this family 5V tolerant. The LA-ispMACH 4000V/Z also offers enhanced I/O features such as slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. The LA-ispMACH 4000V/Z automotive family is in-system programmable through the IEEE Standard 1532 interface. IEEE Standard 1149.1 boundary scan testing capability also allows product testing on automated test equipment. The 1532 interface signals TCK, TMS, TDI and TDO are referenced to VCC (logic core).

Overview

The LA-ispMACH 4000V/Z automotive devices consist of multiple 36-input, 16-macrocell Generic Logic Blocks (GLBs) interconnected by a Global Routing Pool (GRP). Output Routing Pools (ORPs) connect the GLBs to the I/O Blocks (IOBs), which contain multiple I/O cells. This architecture is shown in Figure 1.

Figure 1. Functional Block Diagram



Product Term Allocator

The product term allocator assigns product terms from a cluster to either logic or control applications as required by the design being implemented. Product terms that are used as logic are steered into a 5-input OR gate associated with the cluster. Product terms that used for control are steered either to the macrocell or I/O cell associated with the cluster. Table 3 shows the available functions for each of the five product terms in the cluster. The OR gate output connects to the associated I/O cell, providing a fast path for narrow combinatorial functions, and to the logic allocator.

Table 3. Individual PT Steering

Product Term	Logic	Control
PT*n*	Logic PT	Single PT for XOR/OR
PT*n*+1	Logic PT	Individual Clock (PT Clock)
PT*n*+2	Logic PT	Individual Initialization or Individual Clock Enable (PT Initialization/CE)
PT*n*+3	Logic PT	Individual Initialization (PT Initialization)
PT*n*+4	Logic PT	Individual OE (PTOE)

Cluster Allocator

The cluster allocator allows clusters to be steered to neighboring macrocells, thus allowing the creation of functions with more product terms. Table 4 shows which clusters can be steered to which macrocells. Used in this manner, the cluster allocator can be used to form functions of up to 20 product terms. Additionally, the cluster allocator accepts inputs from the wide steering logic. Using these inputs, functions up to 80 product terms can be created.

Table 4. Available Clusters for Each Macrocell

Macrocell	Available Clusters			
M0	—	C0	C1	C2
M1	C0	C1	C2	C3
M2	C1	C2	C3	C4
M3	C2	C3	C4	C5
M4	C3	C4	C5	C6
M5	C4	C5	C6	C7
M6	C5	C6	C7	C8
M7	C6	C7	C8	C9
M8	C7	C8	C9	C10
M9	C8	C9	C10	C11
M10	C9	C10	C11	C12
M11	C10	C11	C12	C13
M12	C11	C12	C13	C14
M13	C12	C13	C14	C15
M14	C13	C14	C15	—
M15	C14	C15	—	—

Wide Steering Logic

The wide steering logic allows the output of the cluster allocator n to be connected to the input of the cluster allocator *n*+4. Thus, cluster chains can be formed with up to 80 product terms, supporting wide product term functions and allowing performance to be increased through a single GLB implementation. Table 5 shows the product term chains.

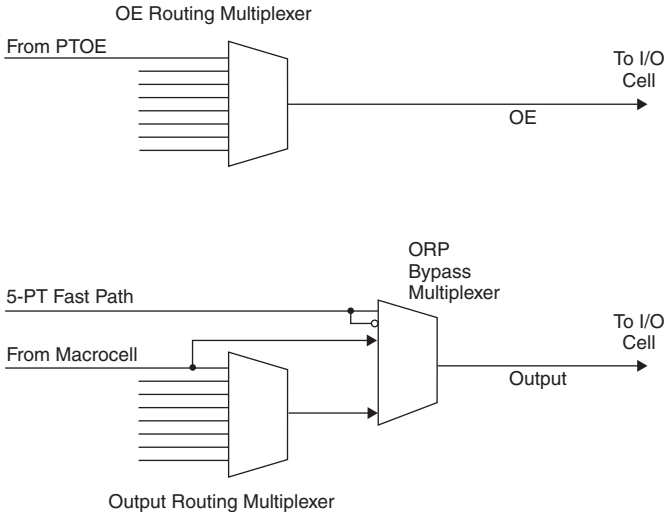
Output Routing Pool (ORP)

The Output Routing Pool allows macrocell outputs to be connected to any of several I/O cells within an I/O block. This provides greater flexibility in determining the pinout and allows design changes to occur without affecting the pinout. The output routing pool also provides a parallel capability for routing macrocell-level OE product terms. This allows the OE product term to follow the macrocell output as it is switched between I/O cells. Additionally, the output routing pool allows the macrocell output or true and complement forms of the 5-PT bypass signal to bypass the output routing multiplexers and feed the I/O cell directly. The enhanced ORP of the LA-ispMACH 4000V/Z family consists of the following elements:

- Output Routing Multiplexers
- OE Routing Multiplexers
- Output Routing Pool Bypass Multiplexers

Figure 7 shows the structure of the ORP from the I/O cell perspective. This is referred to as an ORP slice. Each ORP has as many ORP slices as there are I/O cells in the corresponding I/O block.

Figure 7. ORP Slice



Output Routing Multiplexers

The details of connections between the macrocells and the I/O cells vary across devices and within a device dependent on the maximum number of I/Os available. Tables 6-10 provide the connection details.

Table 6. ORP Combinations for I/O Blocks with 8 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M2, M3, M4, M5, M6, M7, M8, M9
I/O 2	M4, M5, M6, M7, M8, M9, M10, M11
I/O 3	M6, M7, M8, M9, M10, M11, M12, M13
I/O 4	M8, M9, M10, M11, M12, M13, M14, M15
I/O 5	M10, M11, M12, M13, M14, M15, M0, M1
I/O 6	M12, M13, M14, M15, M0, M1, M2, M3
I/O 7	M14, M15, M0, M1, M2, M3, M4, M5

Table 7. ORP Combinations for I/O Blocks with 16 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M1, M2, M3, M4, M5, M6, M7, M8
I/O 2	M2, M3, M4, M5, M6, M7, M8, M9
I/O 3	M3, M4, M5, M6, M7, M8, M9, M10
I/O 4	M4, M5, M6, M7, M8, M9, M10, M11
I/O 5	M5, M6, M7, M8, M9, M10, M11, M12
I/O 6	M6, M7, M8, M9, M10, M11, M12, M13
I/O 7	M7, M8, M9, M10, M11, M12, M13, M14
I/O 8	M8, M9, M10, M11, M12, M13, M14, M15
I/O 9	M9, M10, M11, M12, M13, M14, M15, M0
I/O 10	M10, M11, M12, M13, M14, M15, M0, M1
I/O 11	M11, M12, M13, M14, M15, M0, M1, M2
I/O 12	M12, M13, M14, M15, M0, M1, M2, M3
I/O 13	M13, M14, M15, M0, M1, M2, M3, M4
I/O 14	M14, M15, M0, M1, M2, M3, M4, M5
I/O 15	M15, M0, M1, M2, M3, M4, M5, M6

Table 8. ORP Combinations for I/O Blocks with 12 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M1, M2, M3, M4, M5, M6, M7, M8
I/O 2	M2, M3, M4, M5, M6, M7, M8, M9
I/O 3	M4, M5, M6, M7, M8, M9, M10, M11
I/O 4	M5, M6, M7, M8, M9, M10, M11, M12
I/O 5	M6, M7, M8, M9, M10, M11, M12, M13
I/O 6	M8, M9, M10, M11, M12, M13, M14, M15
I/O 7	M9, M10, M11, M12, M13, M14, M15, M0
I/O 8	M10, M11, M12, M13, M14, M15, M0, M1
I/O 9	M12, M13, M14, M15, M0, M1, M2, M3
I/O 10	M13, M14, M15, M0, M1, M2, M3, M4
I/O 11	M14, M15, M0, M1, M2, M3, M4, M5

ORP Bypass and Fast Output Multiplexers

The ORP bypass and fast-path output multiplexer is a 4:1 multiplexer and allows the 5-PT fast path to bypass the ORP and be connected directly to the pin with either the regular output or the inverted output. This multiplexer also allows the register output to bypass the ORP to achieve faster t_{CO}.

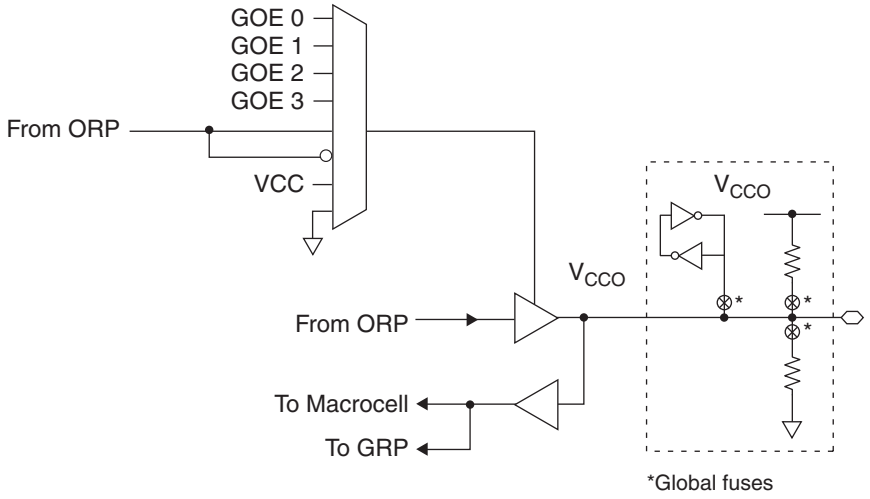
Output Enable Routing Multiplexers

The OE Routing Pool provides the corresponding local output enable (OE) product term to the I/O cell.

I/O Cell

The I/O cell contains the following programmable elements: output buffer, input buffer, OE multiplexer and bus maintenance circuitry. Figure 8 details the I/O cell.

Figure 8. I/O Cell



Each output supports a variety of output standards dependent on the V_{CCO} supplied to its I/O bank. Outputs can also be configured for open drain operation. Each input can be programmed to support a variety of standards, independent of the V_{CCO} supplied to its I/O bank. The I/O standards supported are:

- LVTTL
- LVCMOS 3.3
- LVCMOS 2.5
- LVCMOS 1.8
- 3.3V PCI Compatible

All of the I/Os and dedicated inputs have the capability to provide a bus-keeper latch, Pull-up Resistor or Pull-down Resistor. A fourth option is to provide none of these. The selection is done on a global basis. The default in both hardware and software is such that when the device is erased or if the user does not specify, the input structure is configured to be a Pull-up Resistor.

Each LA-ispMACH 4000V/Z automotive device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for fast slew or slow slew. The typical edge rate difference between fast and slow slew setting is 20%. For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed.

Global OE Generation

Most LA-ispMACH 4000V/Z automotive family devices have a 4-bit wide Global OE Bus, except the LA-ispMACH 4032V and LA-ispMACH4032Z devices that have a 2-bit wide Global OE Bus. This bus is derived from a 4-bit internal global OE PT bus and two dual purpose I/O or GOE pins. Each signal that drives the bus can optionally be inverted.

Each GLB has a block-level OE PT that connects to all bits of the Global OE PT bus with four fuses. Hence, for a 128-macrocell device (with 16 blocks), each line of the bus is driven from 8 OE product terms. Figures 9 and 10 show a graphical representation of the global OE generation.

Absolute Maximum Ratings[1, 2, 3]

	LA-ispMACH 4000V (3.3V)	LA-ispMACH 4000Z (1.8V)
Supply Voltage (V_{CC})	-0.5 to 5.5V	-0.5 to 2.5V
Output Supply Voltage (V_{CCO})	-0.5 to 4.5V	-0.5 to 4.5V
Input or I/O Tristate Voltage Applied[4, 5]	-0.5 to 5.5V	-0.5 to 5.5V
Storage Temperature	-65 to 150°C	-65 to 150°C
Junction Temperature (T_j) with Power Applied	-55 to 150°C	-55 to 150°C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Undershoot of -2V and overshoot of (V_{IH} (MAX) + 2V), up to a total pin voltage of 6.0V, is permitted for a duration of < 20ns.
5. Maximum of 64 I/Os per device with VIN > 3.6V is allowed.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V_{CC}	LA-ispMACH 4000V Supply Voltage	3.0	3.6	V
	LA-ispMACH 4000Z Supply Voltage	1.7	1.9	V
	LA-ispMACH 4000Z, Extended Functional Voltage Operations	1.6[1]	1.9	V
T_A	Ambient Temperature (Automotive)	-40	125	C

1. Devices operating at 1.6V can expect performance degradation up to 35%.

Erase Reprogram Specifications

Parameter	Min.	Max.	Units
Erase/Reprogram Cycle	1,000	—	Cycles

Note: Valid over commercial temperature range.

Hot Socketing Characteristics[1,2,3]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DK}	Input or I/O Leakage Current	$0 \le V_{IN} \le 3.0V$, Tj = 105°C	—	±30	±150	µA
		$0 \le V_{IN} \le 3.0V$, Tj = 130°C	—	±30	±200	µA

1. Insensitive to sequence of V_{CC} or V_{CCO}. However, assumes monotonic rise/fall rates for V_{CC} and V_{CCO}, provided (V_{IN} - V_{CCO}) ≤ 3.6V.
2. $0 < V_{CC} < V_{CC}$ (MAX), $0 < V_{CCO} < V_{CCO}$ (MAX).
3. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}. Device defaults to pull-up until fuse circuitry is active.

I/O Recommended Operating Conditions

Standard	V_{CCO} (V)[1]	
	Min.	Max.
LVTTL	3.0	3.6
LVCMOS 3.3	3.0	3.6
Extended LVCMOS 3.3[2]	2.7	3.6
LVCMOS 2.5	2.3	2.7
LVCMOS 1.8	1.65	1.95
PCI 3.3	3.0	3.6

1. Typical values for V_{CCO} are the average of the min. and max. values.
2. LA-ispMACH 4000Z only.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1, 4]	Input Leakage Current (LA-ispMACH 4000Z)	$0 \le V_{IN} < V_{CCO}$	—	0.5	1	µA
I_{IH}[1, 2]	Input High Leakage Current (LA-ispMACH 4000V)	$3.6V < V_{IN} \le 5.5V$, $T_j = 105°C$ $3.0V \le V_{CCO} \le 3.6V$	—	—	20	µA
		$3.6V < V_{IN} \le 5.5V$, $T_j = 130°C$ $3.0V \le V_{CCO} \le 3.6V$	—	—	50	µA
	Input High Leakage Current (LA-ispMACH 4000Z)	$V_{CCO} < V_{IN} \le 5.5V$	—	—	10	µA
I_{PU}	I/O Weak Pull-up Resistor Current (LA-ispMACH 4000V)	$0 \le V_{IN} \le 0.7V_{CCO}$	-30	—	-200	µA
	I/O Weak Pull-up Resistor Current (LA-ispMACH 4000Z)	$0 \le V_{IN} \le 0.7V_{CCO}$	-30	—	-150	µA
I_{PD}	I/O Weak Pull-down Resistor Current	V_{IL} (MAX) $\le V_{IN} \le V_{IH}$ (MIN)	30	—	150	µA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7\ V_{CCO}$	-30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive Current	$0V \le V_{IN} \le V_{BHT}$	—	—	150	µA
I_{BHHO}	Bus Hold High Overdrive Current	$V_{BHT} \le V_{IN} \le V_{CCO}$	—	—	-150	µA
V_{BHT}	Bus Hold Trip Points	—	V_{CCO} * 0.35	—	V_{CCO} * 0.65	V
C_1	I/O Capacitance[3]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	8	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	
C_2	Clock Capacitance[3]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	6	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	
C_3	Global Input Capacitance[3]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	6	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. 5V tolerant inputs and I/O should only be placed in banks where $3.0V \le V_{CCO} \le 3.6V$.
3. $T_A = 25°C$, f = 1.0MHz.
4. I_{IH} excursions of up to 1.5µA maximum per pin above the spec limit may be observed for certain voltage conditions on no more than 10% of the device's I/O pins.

Supply Current, LA-ispMACH 4000V

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
LA-ispMACH 4032V						
ICC	Operating Power Supply Current	Vcc = 3.3V	—	11.8	—	mA
	Standby Power Supply Current	Vcc = 3.3V	—	11.3	—	mA
LA-ispMACH 4064V						
ICC	Operating Power Supply Current	Vcc = 3.3V	—	12	—	mA
	Standby Power Supply Current	Vcc = 3.3V	—	11.5	—	mA
LA-ispMACH 4128V						
ICC	Operating Power Supply Current	Vcc = 3.3V	—	12	—	mA
	Standby Power Supply Current	Vcc = 3.3V	—	11.5	—	mA

Supply Current, LA-ispMACH 4000Z

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
LA-ispMACH 4032Z						
ICC[1, 2, 3, 5]	Operating Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	50	—	µA
		Vcc = 1.9V, T_A = 70°C	—	58	—	µA
		Vcc = 1.9V, T_A = 85°C	—	60	—	µA
		Vcc = 1.9V, T_A = 125°C	—	70	—	µA
ICC[4, 5]	Standby Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	10	—	µA
		Vcc = 1.9V, T_A = 70°C	—	13	20	µA
		Vcc = 1.9V, T_A = 85°C	—	15	25	µA
		Vcc = 1.9V, T_A = 125°C	—	22		µA
LA-ispMACH 4064Z						
ICC[1, 2, 3, 5]	Operating Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	80	—	µA
		Vcc = 1.9V, T_A = 70°C	—	89	—	µA
		Vcc = 1.9V, T_A = 85°C	—	92	—	µA
		Vcc = 1.9V, T_A = 125°C	—	109	—	µA
ICC[4, 5]	Standby Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	11	—	µA
		Vcc = 1.9V, T_A = 70°C	—	15	25	µA
		Vcc = 1.9V, T_A = 85°C	—	18	35	µA
		Vcc = 1.9V, T_A = 125°C	—	37		µA
LA-ispMACH 4128Z						
ICC[1, 2, 3, 5]	Operating Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	168	—	µA
		Vcc = 1.9V, T_A = 70°C	—	190	—	µA
		Vcc = 1.9V, T_A = 85°C	—	195	—	µA
		Vcc = 1.9V, T_A = 125°C	—	212	—	µA
ICC[4, 5]	Standby Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	12	—	µA
		Vcc = 1.9V, T_A = 70°C	—	16	35	µA
		Vcc = 1.9V, T_A = 85°C	—	19	50	µA
		Vcc = 1.9V, T_A = 125°C	—	42	—	µA

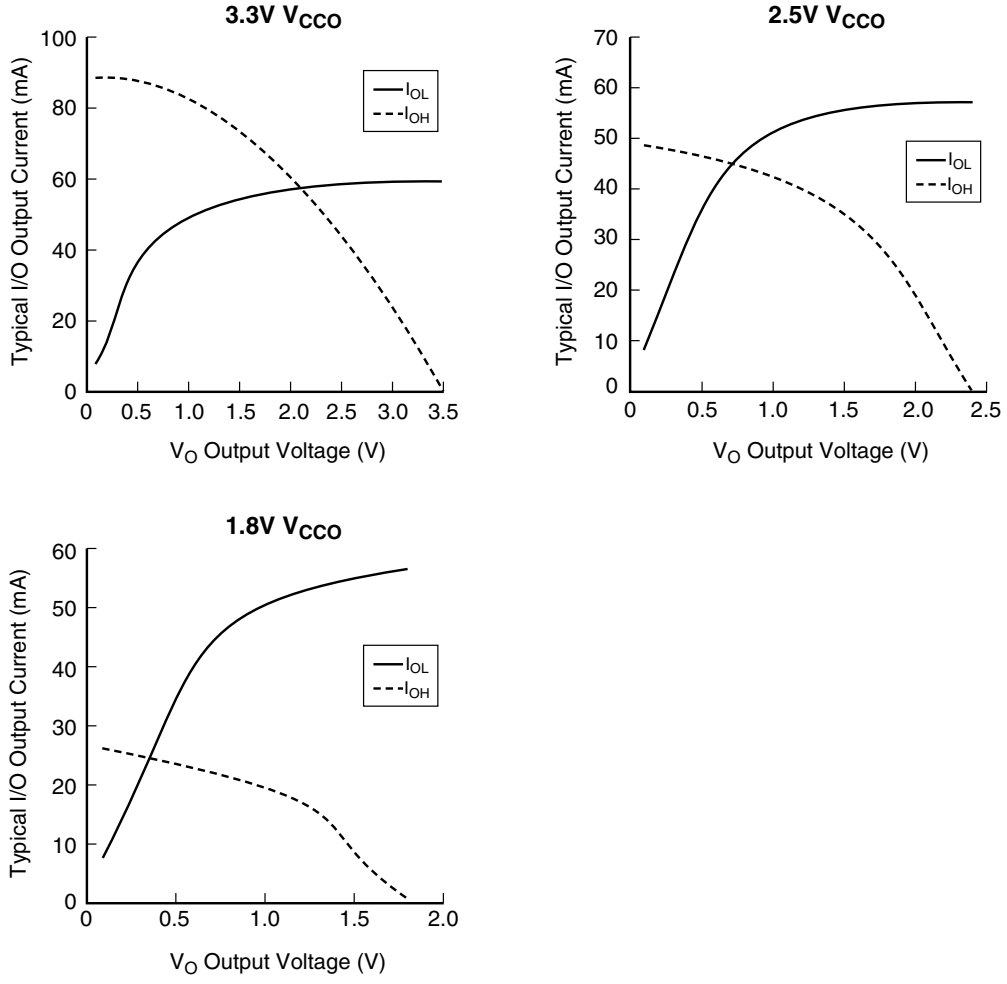
1. T_A = 25°C, frequency = 1.0 MHz.
2. Device configured with 16-bit counters.
3. I_{CC} varies with specific device configuration and operating frequency.
4. V_{CCO} = 3.6V, V_{IN} = 0V or $V_{CCO,}$ bus maintenance turned off. V_{IN} above V_{CCO} will add transient current above the specified standby I_{CC}.
5. Includes V_{CCO} current without output loading.

I/O DC Electrical Characteristics

Over Recommended Operating Conditions

Standard	V_{IL}		V_{IH}		V_{OL} Max (V)	V_{OH} Min (V)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVTTL	-0.3	0.80	2.0	5.5	0.40	V_{CCO} - 0.40	8.0	-4.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
LVCMOS 3.3	-0.3	0.80	2.0	5.5	0.40	V_{CCO} - 0.40	8.0	-4.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
LVCMOS 2.5	-0.3	0.70	1.70	3.6	0.40	V_{CCO} - 0.40	8.0	-4.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
LVCMOS 1.8 (4000V)	-0.3	0.63	1.17	3.6	0.40	V_{CCO} - 0.45	2.0	-2.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
LVCMOS 1.8 (4000Z)	-0.3	0.35 * V_{CC}	0.65 * V_{CC}	3.6	0.40	V_{CCO} - 0.45	2.0	-2.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
PCI 3.3 (4000V)	-0.3	1.08	1.5	5.5	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5
PCI 3.3 (4000Z)	-0.3	0.3 * 3.3 * (V_{CC} / 1.8)	0.5 * 3.3 * (V_{CC} / 1.8)	5.5	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5

1. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank, as shown in the logic signals connection table, shall not exceed *n**8mA. Where *n* is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.



LA-ispMACH 4000V/Z Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	LA-ispMACH 4000V -75		LA-ispMACH 4000Z -75		Units
		Min.	Max.	Min.	Max.	
t_{BSR}	GLB PT Set/Reset Delay	—	1.83	—	1.83	ns
t_{PTSR}	Macrocell PT Set/Reset Delay	—	3.41	—	2.72	ns
t_{GPTOE}	Global PT OE Delay	—	5.58	—	3.50	ns
t_{PTOE}	Macrocell PT OE Delay	—	4.28	—	2.00	ns

Timing v.3.2

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the Timing Model in this data sheet for further details.

Switching Test Conditions

Figure 12 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 9.

Figure 12. Output Test Load, LVTTL and LVCMOS Standards

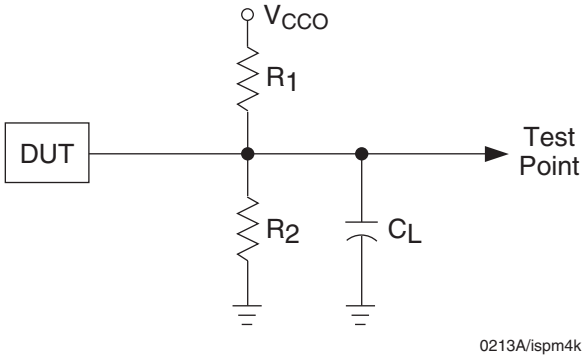


Table 9. Test Fixture Required Components

Test Condition	R_1	R_2	C_L[1]	Timing Ref.	V_{CCO}
LVCMOS I/O, (L -> H, H -> L)	106Ω	106Ω	35pF	LVCMOS 3.3 = 1.5V	LVCMOS 3.3 = 3.0V
				LVCMOS 2.5 = V_{CCO}/2	LVCMOS 2.5 = 2.3V
				LVCMOS 1.8 = V_{CCO}/2	LVCMOS 1.8 = 1.65V
LVCMOS I/O (Z -> H)	∞	106Ω	35pF	1.5V	3.0V
LVCMOS I/O (Z -> L)	106Ω	∞	35pF	1.5V	3.0V
LVCMOS I/O (H -> Z)	∞	106Ω	5pF	V_{OH} - 0.3	3.0V
LVCMOS I/O (L -> Z)	106Ω	∞	5pF	V_{OL} + 0.3	3.0V

1. C_L includes test fixtures and probe capacitance.

LA-ispMACH 4032V and 4064V Logic Signal Connections: 44-Pin TQFP

Pin Number	Bank Number	LA-ispMACH 4032V		LA-ispMACH 4064V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	TDI	-	TDI	-
2	0	A5	A^5	A10	A^5
3	0	A6	A^6	A12	A^6
4	0	A7	A^7	A14	A^7
5	0	GND (Bank 0)	-	GND (Bank 0)	-
6	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
7	0	A8	A^8	B0	B^0
8	0	A9	A^9	B2	B^1
9	0	A10	A^10	B4	B^2
10	-	TCK	-	TCK	-
11	-	VCC	-	VCC	-
12	-	GND	-	GND	-
13	0	A12	A^12	B8	B^4
14	0	A13	A^13	B10	B^5
15	0	A14	A^14	B12	B^6
16	0	A15	A^15	B14	B^7
17	1	CLK2/I	-	CLK2/I	-
18	1	B0	B^0	C0	C^0
19	1	B1	B^1	C2	C^1
20	1	B2	B^2	C4	C^2
21	1	B3	B^3	C6	C^3
22	1	B4	B^4	C8	C^4
23	-	TMS	-	TMS	-
24	1	B5	B^5	C10	C^5
25	1	B6	B^6	C12	C^6
26	1	B7	B^7	C14	C^7
27	1	GND (Bank 1)	-	GND (Bank 1)	-
28	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
29	1	B8	B^8	D0	D^0
30	1	B9	B^9	D2	D^1
31	1	B10	B^10	D4	D^2
32	-	TDO	-	TDO	-
33	-	VCC	-	VCC	-
34	-	GND	-	GND	-
35	1	B12	B^12	D8	D^4
36	1	B13	B^13	D10	D^5
37	1	B14	B^14	D12	D^6
38	1	B15/GOE1	B^15	D14/GOE1	D^7
39	0	CLK0/I	-	CLK0/I	-
40	0	A0/GOE0	A^0	A0/GOE0	A^0
41	0	A1	A^1	A2	A^1
42	0	A2	A^2	A4	A^2

LA-ispMACH 4032V and 4064V Logic Signal Connections: 44-Pin TQFP

Pin Number	Bank Number	LA-ispMACH 4032V		LA-ispMACH 4064V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
43	0	A3	A^3	A6	A^3
44	0	A4	A^4	A8	A^4

LA-ispMACH 4032V/Z and 4064V/Z Logic Signal Connections: 48-Pin TQFP

Pin Number	Bank Number	LA-ispMACH 4032V/Z		LA-ispMACH 4064V/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	TDI	-	TDI	-
2	0	A5	A^5	A10	A^5
3	0	A6	A^6	A12	A^6
4	0	A7	A^7	A14	A^7
5	0	GND (Bank 0)	-	GND (Bank 0)	-
6	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
7	0	A8	A^8	B0	B^0
8	0	A9	A^9	B2	B^1
9	0	A10	A^10	B4	B^2
10	0	A11	A^11	B6	B^3
11	-	TCK	-	TCK	-
12	-	VCC	-	VCC	-
13	-	GND	-	GND	-
14	0	A12	A^12	B8	B^4
15	0	A13	A^13	B10	B^5
16	0	A14	A^14	B12	B^6
17	0	A15	A^15	B14	B^7
18	0	CLK1/I	-	CLK1/I	-
19	1	CLK2/I	-	CLK2/I	-
20	1	B0	B^0	C0	C^0
21	1	B1	B^1	C2	C^1
22	1	B2	B^2	C4	C^2
23	1	B3	B^3	C6	C^3
24	1	B4	B^4	C8	C^4
25	-	TMS	-	TMS	-
26	1	B5	B^5	C10	C^5
27	1	B6	B^6	C12	C^6
28	1	B7	B^7	C14	C^7
29	1	GND (Bank 1)	-	GND (Bank 1)	-
30	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
31	1	B8	B^8	D0	D^0
32	1	B9	B^9	D2	D^1
33	1	B10	B^10	D4	D^2
34	1	B11	B^11	D6	D^3
35	-	TDO	-	TDO	-

LA-ispMACH 4032V/Z and 4064V/Z Logic Signal Connections: 48-Pin TQFP

Pin Number	Bank Number	LA-ispMACH 4032V/Z		LA-ispMACH 4064V/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
36	-	VCC	-	VCC	-
37	-	GND	-	GND	-
38	1	B12	B^12	D8	D^4
39	1	B13	B^13	D10	D^5
40	1	B14	B^14	D12	D^6
41	1	B15/GOE1	B^15	D14/GOE1	D^7
42	1	CLK3/I	-	CLK3/I	-
43	0	CLK0/I	-	CLK0/I	-
44	0	A0/GOE0	A^0	A0/GOE0	A^0
45	0	A1	A^1	A2	A^1
46	0	A2	A^2	A4	A^2
47	0	A3	A^3	A6	A^3
48	0	A4	A^4	A8	A^4

LA-ispMACH 4064V/Z and 4128V/Z Logic Signal Connections: 100-Pin TQFP

Pin Number	Bank Number	LA-ispMACH 4064V/Z		LA-ispMACH 4128V/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	GND	-	GND	-
2	-	TDI	-	TDI	-
3	0	A8	A^8	B0	B^0
4	0	A9	A^9	B2	B^1
5	0	A10	A^10	B4	B^2
6	0	A11	A^11	B6	B^3
7	0	GND (Bank 0)	-	GND (Bank 0)	-
8	0	A12	A^12	B8	B^4
9	0	A13	A^13	B10	B^5
10	0	A14	A^14	B12	B^6
11	0	A15	A^15	B13	B^7
12*	0	I	-	I	-
13	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
14	0	B15	B^15	C14	C^7
15	0	B14	B^14	C12	C^6
16	0	B13	B^13	C10	C^5
17	0	B12	B^12	C8	C^4
18	0	GND (Bank 0)	-	GND (Bank 0)	-
19	0	B11	B^11	C6	C^3
20	0	B10	B^10	C5	C^2
21	0	B9	B^9	C4	C^1
22	0	B8	B^8	C2	C^0
23*	0	I	-	I	-
24	-	TCK	-	TCK	-

LA-ispMACH 4064V/Z and 4128V/Z Logic Signal Connections: 100-Pin TQFP

Pin Number	Bank Number	LA-ispMACH 4064V/Z		LA-ispMACH 4128V/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
68	1	GND (Bank 1)	-	GND (Bank 1)	-
69	1	D11	D^11	G6	G^3
70	1	D10	D^10	G5	G^2
71	1	D9	D^9	G4	G^1
72	1	D8	D^8	G2	G^0
73*	1	I	-	I	-
74	-	TDO	-	TDO	-
75	-	VCC	-	VCC	-
76	-	GND	-	GND	-
77*	1	I	-	I	-
78	1	D7	D^7	H13	H^7
79	1	D6	D^6	H12	H^6
80	1	D5	D^5	H10	H^5
81	1	D4	D^4	H8	H^4
82	1	GND (Bank 1)	-	GND (Bank 1)	-
83	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
84	1	D3	D^3	H6	H^3
85	1	D2	D^2	H4	H^2
86	1	D1	D^1	H2	H^1
87	1	D0/GOE1	D^0	H0/GOE1	H^0
88	1	CLK3/I	-	CLK3/I	-
89	0	CLK0/I	-	CLK0/I	-
90	-	VCC	-	VCC	-
91	0	A0/GOE0	A^0	A0/GOE0	A^0
92	0	A1	A^1	A2	A^1
93	0	A2	A^2	A4	A^2
94	0	A3	A^3	A6	A^3
95	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
96	0	GND (Bank 0)	-	GND (Bank 0)	-
97	0	A4	A^4	A8	A^4
98	0	A5	A^5	A10	A^5
99	0	A6	A^6	A12	A^6
100	0	A7	A^7	A14	A^7

*This pin is input only.

LA-ispMACH 4128V Logic Signal Connections: 128-Pin TQFP (Cont.)

Pin Number	Bank Number	LA-ispMACH 4128V	
		GLB/MC/Pad	ORP
43	0	D5	D^4
44	0	D4	D^3
45	0	D2	D^2
46	0	D1	D^1
47	0	D0	D^0
48	0	CLK1/I	-
49	1	GND (Bank 1)	-
50	1	CLK2/I	-
51	1	VCC	-
52	1	E0	E^0
53	1	E1	E^1
54	1	E2	E^2
55	1	E4	E^3
56	1	E5	E^4
57	1	E6	E^5
58	1	VCCO (Bank 1)	-
59	1	GND (Bank 1)	-
60	1	E8	E^6
61	1	E9	E^7
62	1	E10	E^8
63	1	E12	E^9
64	1	E14	E^11
65	1	GND	-
66	1	TMS	-
67	1	VCCO (Bank 1)	-
68	1	F0	F^0
69	1	F1	F^1
70	1	F2	F^2
71	1	F4	F^3
72	1	F5	F^4
73	1	F6	F^5
74	1	GND (Bank 1)	-
75	1	F8	F^6
76	1	F9	F^7
77	1	F10	F^8
78	1	F12	F^9
79	1	F13	F^10
80	1	F14	F^11
81	1	VCCO (Bank 1)	-
82	1	G14	G^11
83	1	G13	G^10
84	1	G12	G^9
85	1	G10	G^8

LA-ispMACH 4128V Logic Signal Connections: 144-Pin TQFP

Pin Number	Bank Number	LA-ispMACH 4128V	
		GLB/MC/Pad	ORP
1	-	GND	-
2	-	TDI	-
3	0	VCCO (Bank 0)	-
4	0	B0	B^0
5	0	B1	B^1
6	0	B2	B^2
7	0	B4	B^3
8	0	B5	B^4
9	0	B6	B^5
10	0	GND (Bank 0)	-
11	0	B8	B^6
12	0	B9	B^7
13	0	B10	B^8
14	0	B12	B^9
15	0	B13	B^10
16	0	B14	B^11
17	-	NC	-
18	0	GND (Bank 0)[1]	-
19	0	VCCO (Bank 0)	-
20	0	NC	-
21	0	C14	C^11
22	0	C13	C^10
23	0	C12	C^9
24	0	C10	C^8
25	0	C9	C^7
26	0	C8	C^6
27	0	GND (Bank 0)	-
28	0	C6	C^5
29	0	C5	C^4
30	0	C4	C^3
31	0	C2	C^2
32	0	C1	C^1
33	0	C0	C^0
34	0	VCCO (Bank 0)	-
35	-	TCK	-
36	-	VCC	-
37	-	GND	-
38	0	NC	-
39	0	D14	D^11
40	0	D13	D^10
41	0	D12	D^9
42	0	D10	D^8

LA-ispMACH 4128V Logic Signal Connections: 144-Pin TQFP (Cont.)

Pin Number	Bank Number	LA-ispMACH 4128V	
		GLB/MC/Pad	ORP
86	1	F12	F^9
87	1	F13	F^10
88	1	F14	F^11
89	1	NC	-
90	1	GND (Bank 1)[1]	-
91	1	VCCO (Bank 1)	-
92	1	NC	-
93	1	G14	G^11
94	1	G13	G^10
95	1	G12	G^9
96	1	G10	G^8
97	1	G9	G^7
98	1	G8	G^6
99	1	GND (Bank 1)	-
100	1	G6	G^5
101	1	G5	G^4
102	1	G4	G^3
103	1	G2	G^2
104	1	G1	G^1
105	1	G0	G^0
106	1	VCCO (Bank 1)	-
107	-	TDO	-
108	-	VCC	-
109	-	GND	-
110	1	NC	-
111	1	H14	H^11
112	1	H13	H^10
113	1	H12	H^9
114	1	H10	H^8
115	1	H9	H^7
116	1	H8	H^6
117	1	NC	-
118	1	GND (Bank 1)	-
119	1	VCCO (Bank 1)	-
120	1	H6	H^5
121	1	H5	H^4
122	1	H4	H^3
123	1	H2	H^2
124	1	H1	H^1
125	1	H0/GOE1	H^0
126	1	CLK3/I	-
127	0	GND (Bank 0)	-
128	0	CLK0/I	-

LA-ispMACH 4128V Logic Signal Connections: 144-Pin TQFP (Cont.)

Pin Number	Bank Number	LA-ispMACH 4128V	
		GLB/MC/Pad	ORP
129	-	VCC	-
130	0	A0/GOE0	A^0
131	0	A1	A^1
132	0	A2	A^2
133	0	A4	A^3
134	0	A5	A^4
135	0	A6	A^5
136	0	VCCO (Bank 0)	-
137	0	GND (Bank 0)	-
138	0	A8	A^6
139	0	A9	A^7
140	0	A10	A^8
141	0	A12	A^9
142	0	A13	A^10
143	0	A14	A^11
144	0	NC[2]	-

1. For device migration considerations, these NC pins are GND pins for I/O banks in LA-ispMACH 4128V devices.