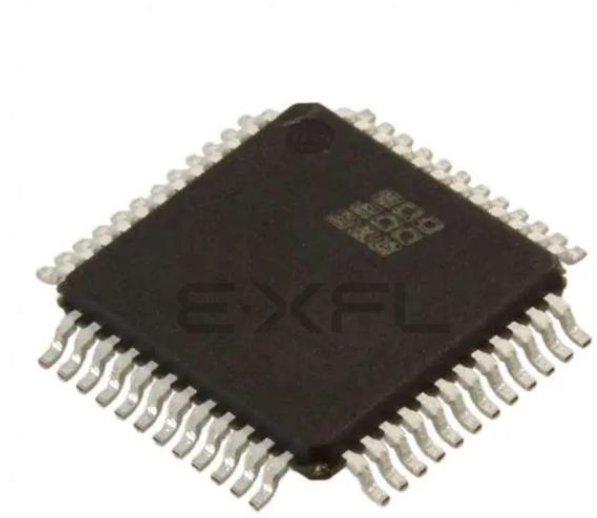

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	-
Number of Macrocells	32
Number of Gates	-
Number of I/O	32
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/la4032v-75tn48e

The I/Os in the LA-ispMACH 4000V/Z automotive devices are split into two banks. Each bank has a separate I/O power supply. Inputs can support a variety of standards independent of the chip or bank power supply. Outputs support the standards compatible with the power supply provided to the bank. Support for a variety of standards helps designers implement designs in mixed voltage environments. In addition, 5V tolerant inputs are specified within an I/O bank that is connected to V_{CCO} of 3.0V to 3.6V for LVCMOS 3.3, LVTTL and PCI interfaces.

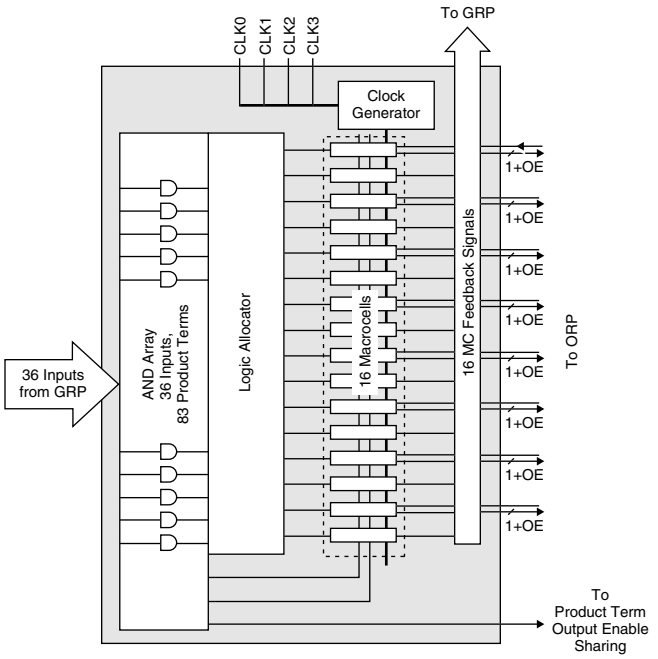
LA-ispMACH 4000V/Z Automotive Architecture

There are a total of two GLBs in the LA-ispMACH 4032V/Z, increasing to 8 GLBs in the LA-ispMACH 4128V/Z. Each GLB has 36 inputs. All GLB inputs come from the GRP and all outputs from the GLB are brought back into the GRP to be connected to the inputs of any other GLB on the device. Even if feedback signals return to the same GLB, they still must go through the GRP. This mechanism ensures that GLBs communicate with each other with consistent and predictable delays. The outputs from the GLB are also sent to the ORP. The ORP then sends them to the associated I/O cells in the I/O block.

Generic Logic Block

The LA-ispMACH 4000V/Z Automotive GLB consists of a programmable AND array, logic allocator, 16 macrocells and a GLB clock generator. Macrocells are decoupled from the product terms through the logic allocator and the I/O pins are decoupled from macrocells through the ORP. Figure 2 illustrates the GLB.

Figure 2. Generic Logic Block



AND Array

The programmable AND Array consists of 36 inputs and 83 output product terms. The 36 inputs from the GRP are used to form 72 lines in the AND Array (true and complement of the inputs). Each line in the array can be connected to any of the 83 output product terms via a wired-AND. Each of the 80 logic product terms feed the logic allocator with the remaining three control product terms feeding the Shared PT Clock, Shared PT Initialization and Shared PT OE. The Shared PT Clock and Shared PT Initialization signals can optionally be inverted before being fed to the macrocells.

Every set of five product terms from the 80 logic product terms forms a product term cluster starting with PT0. There is one product term cluster for every macrocell in the GLB. Figure 3 is a graphical representation of the AND Array.

Product Term Allocator

The product term allocator assigns product terms from a cluster to either logic or control applications as required by the design being implemented. Product terms that are used as logic are steered into a 5-input OR gate associated with the cluster. Product terms that used for control are steered either to the macrocell or I/O cell associated with the cluster. Table 3 shows the available functions for each of the five product terms in the cluster. The OR gate output connects to the associated I/O cell, providing a fast path for narrow combinatorial functions, and to the logic allocator.

Table 3. Individual PT Steering

Product Term	Logic	Control
PT*n*	Logic PT	Single PT for XOR/OR
PT*n*+1	Logic PT	Individual Clock (PT Clock)
PT*n*+2	Logic PT	Individual Initialization or Individual Clock Enable (PT Initialization/CE)
PT*n*+3	Logic PT	Individual Initialization (PT Initialization)
PT*n*+4	Logic PT	Individual OE (PTOE)

Cluster Allocator

The cluster allocator allows clusters to be steered to neighboring macrocells, thus allowing the creation of functions with more product terms. Table 4 shows which clusters can be steered to which macrocells. Used in this manner, the cluster allocator can be used to form functions of up to 20 product terms. Additionally, the cluster allocator accepts inputs from the wide steering logic. Using these inputs, functions up to 80 product terms can be created.

Table 4. Available Clusters for Each Macrocell

Macrocell	Available Clusters			
M0	—	C0	C1	C2
M1	C0	C1	C2	C3
M2	C1	C2	C3	C4
M3	C2	C3	C4	C5
M4	C3	C4	C5	C6
M5	C4	C5	C6	C7
M6	C5	C6	C7	C8
M7	C6	C7	C8	C9
M8	C7	C8	C9	C10
M9	C8	C9	C10	C11
M10	C9	C10	C11	C12
M11	C10	C11	C12	C13
M12	C11	C12	C13	C14
M13	C12	C13	C14	C15
M14	C13	C14	C15	—
M15	C14	C15	—	—

Wide Steering Logic

The wide steering logic allows the output of the cluster allocator n to be connected to the input of the cluster allocator *n*+4. Thus, cluster chains can be formed with up to 80 product terms, supporting wide product term functions and allowing performance to be increased through a single GLB implementation. Table 5 shows the product term chains.

- Block CLK3
- PT Clock
- PT Clock Inverted
- Shared PT Clock
- Ground

Clock Enable Multiplexer

Each macrocell has a 4:1 clock enable multiplexer. This allows the clock enable signal to be selected from the following four sources:

- PT Initialization/CE
- PT Initialization/CE Inverted
- Shared PT Clock
- Logic High

Initialization Control

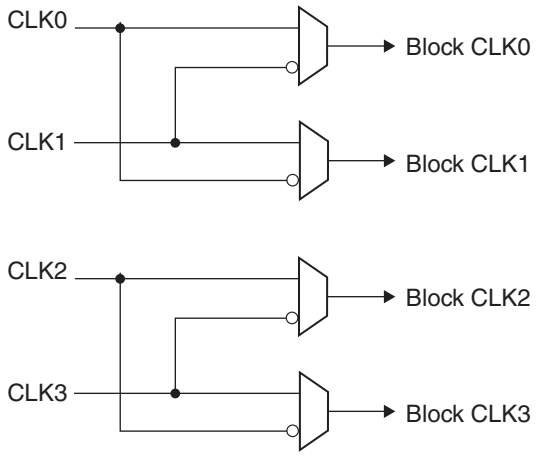
The LA-ispMACH 4000V/Z automotive family architecture accommodates both block-level and macrocell-level set and reset capability. There is one block-level initialization term that is distributed to all macrocell registers in a GLB. At the macrocell level, two product terms can be "stolen" from the cluster associated with a macrocell to be used for set/reset functionality. A reset/preset swapping feature in each macrocell allows for reset and preset to be exchanged, providing flexibility.

Note that the reset/preset swapping selection feature affects power-up reset as well. All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the block-level initialization, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the block-level initialization or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the V_{CC} rise must be monotonic, and the clock must be inactive until the reset delay time has elapsed.

GLB Clock Generator

Each LA-ispMACH 4000V/Z automotive device has up to four clock pins that are also routed to the GRP to be used as inputs. These pins drive a clock generator in each GLB, as shown in Figure 6. The clock generator provides four clock signals that can be used anywhere in the GLB. These four GLB clock signals can consist of a number of combinations of the true and complement edges of the global clock signals.

Figure 6. GLB Clock Generator



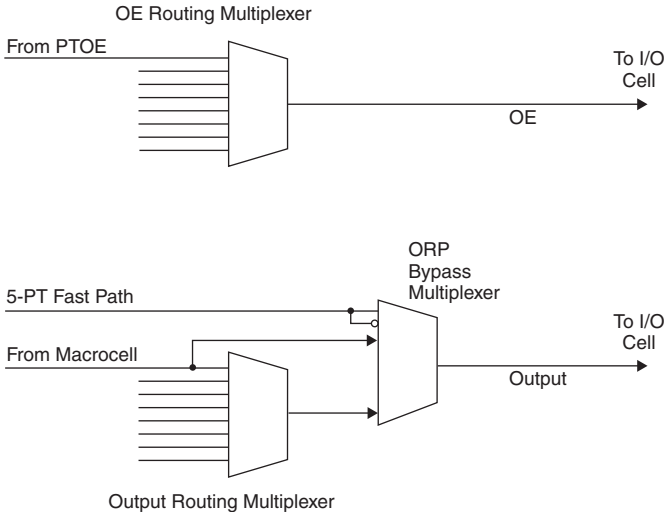
Output Routing Pool (ORP)

The Output Routing Pool allows macrocell outputs to be connected to any of several I/O cells within an I/O block. This provides greater flexibility in determining the pinout and allows design changes to occur without affecting the pinout. The output routing pool also provides a parallel capability for routing macrocell-level OE product terms. This allows the OE product term to follow the macrocell output as it is switched between I/O cells. Additionally, the output routing pool allows the macrocell output or true and complement forms of the 5-PT bypass signal to bypass the output routing multiplexers and feed the I/O cell directly. The enhanced ORP of the LA-ispMACH 4000V/Z family consists of the following elements:

- Output Routing Multiplexers
- OE Routing Multiplexers
- Output Routing Pool Bypass Multiplexers

Figure 7 shows the structure of the ORP from the I/O cell perspective. This is referred to as an ORP slice. Each ORP has as many ORP slices as there are I/O cells in the corresponding I/O block.

Figure 7. ORP Slice



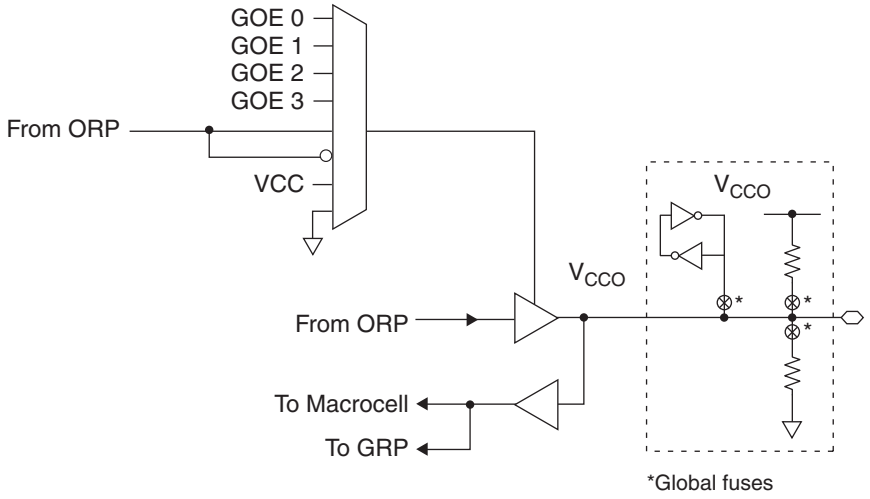
Output Routing Multiplexers

The details of connections between the macrocells and the I/O cells vary across devices and within a device dependent on the maximum number of I/Os available. Tables 6-10 provide the connection details.

Table 6. ORP Combinations for I/O Blocks with 8 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M2, M3, M4, M5, M6, M7, M8, M9
I/O 2	M4, M5, M6, M7, M8, M9, M10, M11
I/O 3	M6, M7, M8, M9, M10, M11, M12, M13
I/O 4	M8, M9, M10, M11, M12, M13, M14, M15
I/O 5	M10, M11, M12, M13, M14, M15, M0, M1
I/O 6	M12, M13, M14, M15, M0, M1, M2, M3
I/O 7	M14, M15, M0, M1, M2, M3, M4, M5

Figure 8. I/O Cell



Each output supports a variety of output standards dependent on the V_{CCO} supplied to its I/O bank. Outputs can also be configured for open drain operation. Each input can be programmed to support a variety of standards, independent of the V_{CCO} supplied to its I/O bank. The I/O standards supported are:

- LVTTL
- LVCMOS 3.3
- LVCMOS 2.5
- LVCMOS 1.8
- 3.3V PCI Compatible

All of the I/Os and dedicated inputs have the capability to provide a bus-keeper latch, Pull-up Resistor or Pull-down Resistor. A fourth option is to provide none of these. The selection is done on a global basis. The default in both hardware and software is such that when the device is erased or if the user does not specify, the input structure is configured to be a Pull-up Resistor.

Each LA-ispMACH 4000V/Z automotive device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for fast slew or slow slew. The typical edge rate difference between fast and slow slew setting is 20%. For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed.

Global OE Generation

Most LA-ispMACH 4000V/Z automotive family devices have a 4-bit wide Global OE Bus, except the LA-ispMACH 4032V and LA-ispMACH4032Z devices that have a 2-bit wide Global OE Bus. This bus is derived from a 4-bit internal global OE PT bus and two dual purpose I/O or GOE pins. Each signal that drives the bus can optionally be inverted.

Each GLB has a block-level OE PT that connects to all bits of the Global OE PT bus with four fuses. Hence, for a 128-macrocell device (with 16 blocks), each line of the bus is driven from 8 OE product terms. Figures 9 and 10 show a graphical representation of the global OE generation.

and inputs without being damaged. Additionally, it requires that the effects of I/O pin loading be minimal on active signals. The LA-ispMACH 4000V/Z automotive devices provide this capability for input voltages in the range 0V to 3.0V.

Density Migration

The LA-ispMACH 4000V/Z automotive family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is possible to shift a lower utilization design targeted for a high density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

AEC-Q100 Tested and Qualified

The Automotive Electronics Council (AEC) consists of two committees: the Quality Systems Committee and the Component Technical Committee. These committees are composed of representatives from sustaining and other associate members. The AEC Component Technical Committee is the standardization body for establishing standards for reliable, high quality electronic components. In particular, the AEC-Q100 specification “Stress Test for Qualification for Integrated Circuits” defines qualification and re-qualification requirements for electronic components. Components meeting these specifications are suitable for use in the harsh automotive environment without additional component-level qualification testing. Lattice's LA-ispMACH 4000V/Z and LA-MachXO devices completed and passed the requirements of the AEC-Q100 specification.

Supply Current, LA-ispMACH 4000V

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
LA-ispMACH 4032V						
ICC	Operating Power Supply Current	Vcc = 3.3V	—	11.8	—	mA
	Standby Power Supply Current	Vcc = 3.3V	—	11.3	—	mA
LA-ispMACH 4064V						
ICC	Operating Power Supply Current	Vcc = 3.3V	—	12	—	mA
	Standby Power Supply Current	Vcc = 3.3V	—	11.5	—	mA
LA-ispMACH 4128V						
ICC	Operating Power Supply Current	Vcc = 3.3V	—	12	—	mA
	Standby Power Supply Current	Vcc = 3.3V	—	11.5	—	mA

LA-ispMACH 4000V/Z External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description[1, 2, 3]	LA-ispMACH 4000V -75		LA-ispMACH 4000Z -75		Units
		Min.	Max.	Min.	Max.	
t_{PD}	5-PT bypass combinatorial propagation delay	—	7.5	—	7.5	ns
t_{PD_MC}	20-PT combinatorial propagation delay through macrocell	—	8.0	—	8.0	ns
t_S	GLB register setup time before clock	4.5	—	4.5	—	ns
t_{ST}	GLB register setup time before clock with T-type register	4.7	—	4.7	—	ns
t_{SIR}	GLB register setup time before clock, input register path	1.7	—	1.4	—	ns
t_{SIRZ}	GLB register setup time before clock with zero hold	2.7	—	2.7	—	ns
t_H	GLB register hold time after clock	0.0	—	0.0	—	ns
t_{HT}	GLB register hold time after clock with T-type register	0.0	—	0.0	—	ns
t_{HIR}	GLB register hold time after clock, input register path	1.0	—	1.3	—	ns
t_{HIRZ}	GLB register hold time after clock, input register path with zero hold	0.0	—	0.0	—	ns
t_{CO}	GLB register clock-to-output delay	—	4.5	—	4.5	ns
t_R	External reset pin to output delay	—	9.0	—	9.0	ns
t_{RW}	External reset pulse duration	4.0	—	4.0	—	ns
$t_{PTOE/DIS}$	Input to output local product term output enable/disable	—	9.0	—	9.0	ns
$t_{GPTOE/DIS}$	Input to output global product term output enable/disable	—	10.3	—	10.5	ns
$t_{GOE/DIS}$	Global OE input to output enable/disable	—	7.0	—	7.0	ns
t_{CW}	Global clock width, high or low	2.8	—	2.8	—	ns
t_{GW}	Global gate width low (for low transparent) or high (for high transparent)	2.8	—	2.8	—	ns
t_{WIR}	Input register clock width, high or low	2.8	—	2.8	—	ns
f_{MAX}[4]	Clock frequency with internal feedback	—	168	—	168	MHz
f_{MAX} (Ext.)	Clock frequency with external feedback, [1/ (t_S + t_{CO})]	—	111	—	111	MHz

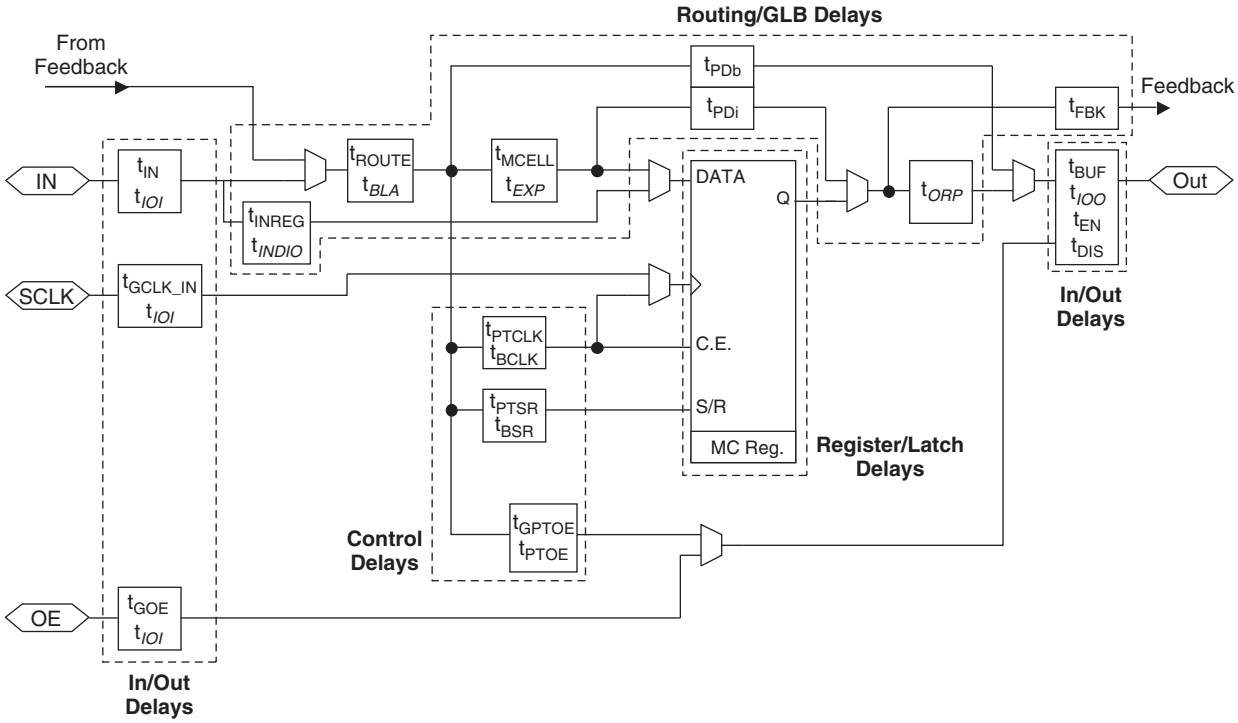
1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.
2. Measured using standard switching circuit, assuming GRP loading of 1 and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using GRP feedback.

Timing v.3.2

Timing Model

The task of determining the timing through the LA-ispMACH 4000V/Z automotive family, like any CPLD, is relatively simple. The timing model provided in Figure 11 shows the specific delay paths. Once the implementation of a given function is determined either conceptually or from the software report file, the delay path of the function can easily be determined from the timing model. The Lattice design tools report the timing delays based on the same timing model for a particular design. Note that the internal timing parameters are given for reference only, and are not tested. The external timing parameters are tested and guaranteed for every device. For more information on the timing model and usage, refer to TN1004, ispMACH 4000 Timing Model Design and Usage Guidelines.

Figure 11. LA-ispMACH 4000V/Z Automotive Timing Model



Note: Italicized items are optional delay adders.

LA-ispMACH 4000V/Z Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	LA-ispMACH 4000V -75		LA-ispMACH 4000Z -75		Units
		Min.	Max.	Min.	Max.	
t_{BSR}	GLB PT Set/Reset Delay	—	1.83	—	1.83	ns
t_{PTSR}	Macrocell PT Set/Reset Delay	—	3.41	—	2.72	ns
t_{GPTOE}	Global PT OE Delay	—	5.58	—	3.50	ns
t_{PTOE}	Macrocell PT OE Delay	—	4.28	—	2.00	ns

Timing v.3.2

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the Timing Model in this data sheet for further details.

Boundary Scan Waveforms and Timing Specifications

Symbol	Parameter	Min.	Max.	Units
t_{BTCP}	TCK [BSCAN test] clock cycle	40	—	ns
t_{BTCH}	TCK [BSCAN test] pulse width high	20	—	ns
t_{BTCL}	TCK [BSCAN test] pulse width low	20	—	ns
t_{BTSU}	TCK [BSCAN test] setup time	8	—	ns
t_{BTH}	TCK [BSCAN test] hold time	10	—	ns
t_{BRF}	TCK [BSCAN test] rise and fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
t_{BTOZ}	TAP controller falling edge of clock to data output disable	—	10	ns
t_{BTVO}	TAP controller falling edge of clock to data output enable	—	10	ns
t_{BTCPSU}	BSCAN test Capture register setup time	8	—	ns
t_{BTCPH}	BSCAN test Capture register hold time	10	—	ns
t_{BTUCO}	BSCAN test Update reg, falling edge of clock to valid output	—	25	ns
t_{BTUOZ}	BSCAN test Update reg, falling edge of clock to output disable	—	25	ns
t_{BTUOV}	BSCAN test Update reg, falling edge of clock to output enable	—	25	ns

LA-ispMACH 4000V/Z Power Supply and NC Connections[1]

Signal	44 TQFP[2]	48 TQFP[2]	100 TQFP[2]	128 TQFP[2]	144 TQFP[2]
VCC	11, 33	12, 36	25, 40, 75, 90	32, 51, 96, 115	36, 57, 108, 129
VCCO0 VCCO (Bank 0)	6	6	13, 33, 95	3, 17, 30, 41, 122	3, 19, 34, 47, 136
VCCO1 VCCO (Bank 1)	28	30	45, 63, 83	58, 67, 81, 94, 105	64, 75, 91, 106, 119
GND	12, 34	13, 37	1, 26, 51, 76	1, 33, 65, 97	1, 37, 73, 109
GND (Bank 0)	5	5	7, 18, 32, 96	10, 24, 40, 113, 123	10, 18[6], 27, 46, 127, 137
GND (Bank 1)	27	29	46, 57, 68, 82	49, 59, 74, 88, 104	55, 65, 82, 90[6], 99, 118
NC	None	None	None	None	17, 20, 38, 45, 72, 89, 92, 110, 117, 144

1. All grounds must be electrically connected at the board level. However, for the purposes of I/O current loading, grounds are associated with the bank shown.
2. Pin orientation follows the conventional order from pin 1 marking of the top side view and counter-clockwise.

LA-ispMACH 4032V and 4064V Logic Signal Connections: 44-Pin TQFP

Pin Number	Bank Number	LA-ispMACH 4032V		LA-ispMACH 4064V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	TDI	-	TDI	-
2	0	A5	A^5	A10	A^5
3	0	A6	A^6	A12	A^6
4	0	A7	A^7	A14	A^7
5	0	GND (Bank 0)	-	GND (Bank 0)	-
6	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
7	0	A8	A^8	B0	B^0
8	0	A9	A^9	B2	B^1
9	0	A10	A^10	B4	B^2
10	-	TCK	-	TCK	-
11	-	VCC	-	VCC	-
12	-	GND	-	GND	-
13	0	A12	A^12	B8	B^4
14	0	A13	A^13	B10	B^5
15	0	A14	A^14	B12	B^6
16	0	A15	A^15	B14	B^7
17	1	CLK2/I	-	CLK2/I	-
18	1	B0	B^0	C0	C^0
19	1	B1	B^1	C2	C^1
20	1	B2	B^2	C4	C^2
21	1	B3	B^3	C6	C^3
22	1	B4	B^4	C8	C^4
23	-	TMS	-	TMS	-
24	1	B5	B^5	C10	C^5
25	1	B6	B^6	C12	C^6
26	1	B7	B^7	C14	C^7
27	1	GND (Bank 1)	-	GND (Bank 1)	-
28	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
29	1	B8	B^8	D0	D^0
30	1	B9	B^9	D2	D^1
31	1	B10	B^10	D4	D^2
32	-	TDO	-	TDO	-
33	-	VCC	-	VCC	-
34	-	GND	-	GND	-
35	1	B12	B^12	D8	D^4
36	1	B13	B^13	D10	D^5
37	1	B14	B^14	D12	D^6
38	1	B15/GOE1	B^15	D14/GOE1	D^7
39	0	CLK0/I	-	CLK0/I	-
40	0	A0/GOE0	A^0	A0/GOE0	A^0
41	0	A1	A^1	A2	A^1
42	0	A2	A^2	A4	A^2

LA-ispMACH 4032V/Z and 4064V/Z Logic Signal Connections: 48-Pin TQFP

Pin Number	Bank Number	LA-ispMACH 4032V/Z		LA-ispMACH 4064V/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
36	-	VCC	-	VCC	-
37	-	GND	-	GND	-
38	1	B12	B^12	D8	D^4
39	1	B13	B^13	D10	D^5
40	1	B14	B^14	D12	D^6
41	1	B15/GOE1	B^15	D14/GOE1	D^7
42	1	CLK3/I	-	CLK3/I	-
43	0	CLK0/I	-	CLK0/I	-
44	0	A0/GOE0	A^0	A0/GOE0	A^0
45	0	A1	A^1	A2	A^1
46	0	A2	A^2	A4	A^2
47	0	A3	A^3	A6	A^3
48	0	A4	A^4	A8	A^4

LA-ispMACH 4064V/Z and 4128V/Z Logic Signal Connections: 100-Pin TQFP

Pin Number	Bank Number	LA-ispMACH 4064V/Z		LA-ispMACH 4128V/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	GND	-	GND	-
2	-	TDI	-	TDI	-
3	0	A8	A^8	B0	B^0
4	0	A9	A^9	B2	B^1
5	0	A10	A^10	B4	B^2
6	0	A11	A^11	B6	B^3
7	0	GND (Bank 0)	-	GND (Bank 0)	-
8	0	A12	A^12	B8	B^4
9	0	A13	A^13	B10	B^5
10	0	A14	A^14	B12	B^6
11	0	A15	A^15	B13	B^7
12*	0	I	-	I	-
13	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
14	0	B15	B^15	C14	C^7
15	0	B14	B^14	C12	C^6
16	0	B13	B^13	C10	C^5
17	0	B12	B^12	C8	C^4
18	0	GND (Bank 0)	-	GND (Bank 0)	-
19	0	B11	B^11	C6	C^3
20	0	B10	B^10	C5	C^2
21	0	B9	B^9	C4	C^1
22	0	B8	B^8	C2	C^0
23*	0	I	-	I	-
24	-	TCK	-	TCK	-

LA-ispMACH 4128V Logic Signal Connections: 128-Pin TQFP

Pin Number	Bank Number	LA-ispMACH 4128V	
		GLB/MC/Pad	ORP
1	0	GND	-
2	0	TDI	-
3	0	VCCO (Bank 0)	-
4	0	B0	B^0
5	0	B1	B^1
6	0	B2	B^2
7	0	B4	B^3
8	0	B5	B^4
9	0	B6	B^5
10	0	GND (Bank 0)	-
11	0	B8	B^6
12	0	B9	B^7
13	0	B10	B^8
14	0	B12	B^9
15	0	B13	B^10
16	0	B14	B^11
17	0	VCCO (Bank 0)	-
18	0	C14	C^11
19	0	C13	C^10
20	0	C12	C^9
21	0	C10	C^8
22	0	C9	C^7
23	0	C8	C^6
24	0	GND (Bank 0)	-
25	0	C6	C^5
26	0	C5	C^4
27	0	C4	C^3
28	0	C2	C^2
29	0	C0	C^0
30	0	VCCO (Bank 0)	-
31	0	TCK	-
32	0	VCC	-
33	0	GND	-
34	0	D14	D^11
35	0	D13	D^10
36	0	D12	D^9
37	0	D10	D^8
38	0	D9	D^7
39	0	D8	D^6
40	0	GND (Bank 0)	-
41	0	VCCO (Bank 0)	-
42	0	D6	D^5

LA-ispMACH 4128V Logic Signal Connections: 128-Pin TQFP (Cont.)

Pin Number	Bank Number	LA-ispMACH 4128V	
		GLB/MC/Pad	ORP
43	0	D5	D^4
44	0	D4	D^3
45	0	D2	D^2
46	0	D1	D^1
47	0	D0	D^0
48	0	CLK1/I	-
49	1	GND (Bank 1)	-
50	1	CLK2/I	-
51	1	VCC	-
52	1	E0	E^0
53	1	E1	E^1
54	1	E2	E^2
55	1	E4	E^3
56	1	E5	E^4
57	1	E6	E^5
58	1	VCCO (Bank 1)	-
59	1	GND (Bank 1)	-
60	1	E8	E^6
61	1	E9	E^7
62	1	E10	E^8
63	1	E12	E^9
64	1	E14	E^11
65	1	GND	-
66	1	TMS	-
67	1	VCCO (Bank 1)	-
68	1	F0	F^0
69	1	F1	F^1
70	1	F2	F^2
71	1	F4	F^3
72	1	F5	F^4
73	1	F6	F^5
74	1	GND (Bank 1)	-
75	1	F8	F^6
76	1	F9	F^7
77	1	F10	F^8
78	1	F12	F^9
79	1	F13	F^10
80	1	F14	F^11
81	1	VCCO (Bank 1)	-
82	1	G14	G^11
83	1	G13	G^10
84	1	G12	G^9
85	1	G10	G^8

LA-ispMACH 4128V Logic Signal Connections: 144-Pin TQFP

Pin Number	Bank Number	LA-ispMACH 4128V	
		GLB/MC/Pad	ORP
1	-	GND	-
2	-	TDI	-
3	0	VCCO (Bank 0)	-
4	0	B0	B^0
5	0	B1	B^1
6	0	B2	B^2
7	0	B4	B^3
8	0	B5	B^4
9	0	B6	B^5
10	0	GND (Bank 0)	-
11	0	B8	B^6
12	0	B9	B^7
13	0	B10	B^8
14	0	B12	B^9
15	0	B13	B^10
16	0	B14	B^11
17	-	NC	-
18	0	GND (Bank 0)[1]	-
19	0	VCCO (Bank 0)	-
20	0	NC	-
21	0	C14	C^11
22	0	C13	C^10
23	0	C12	C^9
24	0	C10	C^8
25	0	C9	C^7
26	0	C8	C^6
27	0	GND (Bank 0)	-
28	0	C6	C^5
29	0	C5	C^4
30	0	C4	C^3
31	0	C2	C^2
32	0	C1	C^1
33	0	C0	C^0
34	0	VCCO (Bank 0)	-
35	-	TCK	-
36	-	VCC	-
37	-	GND	-
38	0	NC	-
39	0	D14	D^11
40	0	D13	D^10
41	0	D12	D^9
42	0	D10	D^8

LA-ispMACH 4128V Logic Signal Connections: 144-Pin TQFP (Cont.)

Pin Number	Bank Number	LA-ispMACH 4128V	
		GLB/MC/Pad	ORP
43	0	D9	D^7
44	0	D8	D^6
45	0	NC	-
46	0	GND (Bank 0)	-
47	0	VCCO (Bank 0)	-
48	0	D6	D^5
49	0	D5	D^4
50	0	D4	D^3
51	0	D2	D^2
52	0	D1	D^1
53	0	D0	D^0
54	0	CLK1/I	-
55	1	GND (Bank 1)	-
56	1	CLK2/I	-
57	-	VCC	-
58	1	E0	E^0
59	1	E1	E^1
60	1	E2	E^2
61	1	E4	E^3
62	1	E5	E^4
63	1	E6	E^5
64	1	VCCO (Bank 1)	-
65	1	GND (Bank 1)	-
66	1	E8	E^6
67	1	E9	E^7
68	1	E10	E^8
69	1	E12	E^9
70	1	E13	E^10
71	1	E14	E^11
72	1	NC	-
73	-	GND	-
74	-	TMS	-
75	1	VCCO (Bank 1)	-
76	1	F0	F^0
77	1	F1	F^1
78	1	F2	F^2
79	1	F4	F^3
80	1	F5	F^4
81	1	F6	F^5
82	1	GND (Bank 1)	-
83	1	F8	F^6
84	1	F9	F^7
85	1	F10	F^8

LA-ispMACH 4128V Logic Signal Connections: 144-Pin TQFP (Cont.)

Pin Number	Bank Number	LA-ispMACH 4128V	
		GLB/MC/Pad	ORP
129	-	VCC	-
130	0	A0/GOE0	A^0
131	0	A1	A^1
132	0	A2	A^2
133	0	A4	A^3
134	0	A5	A^4
135	0	A6	A^5
136	0	VCCO (Bank 0)	-
137	0	GND (Bank 0)	-
138	0	A8	A^6
139	0	A9	A^7
140	0	A10	A^8
141	0	A12	A^9
142	0	A13	A^10
143	0	A14	A^11
144	0	NC[2]	-

1. For device migration considerations, these NC pins are GND pins for I/O banks in LA-ispMACH 4128V devices.

Revision History

Date	Version	Change Summary
April 2006	01.0	Initial release.
October 2006	02.0	Added LA-ispMACH 4000Z support information throughout.
March 2007	02.1	Updated ispMACH 4000 Introduction section.
		Updated Signal Descriptions table.
September 2007	02.2	DC Electrical Characteristics table, removed duplicate specifications.
July 2008	02.3	Lowered the maximum supply current at 85°C to match the commercial product values.
		Added automotive disclaimer.
May 2009	02.4	Correction to t_{CW}, tGW, t_{WIR} and f_{MAX} parameters in External Switching Characteristics table.
May 2009	02.5	Correction to t_{CW}, tGW and t_{WIR} parameters in External Switching Characteristics table.