Lattice Semiconductor Corporation - LA4064V-75TN100E Datasheet

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	-
Number of Macrocells	64
Number of Gates	-
Number of I/O	64
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/la4064v-75tn100e

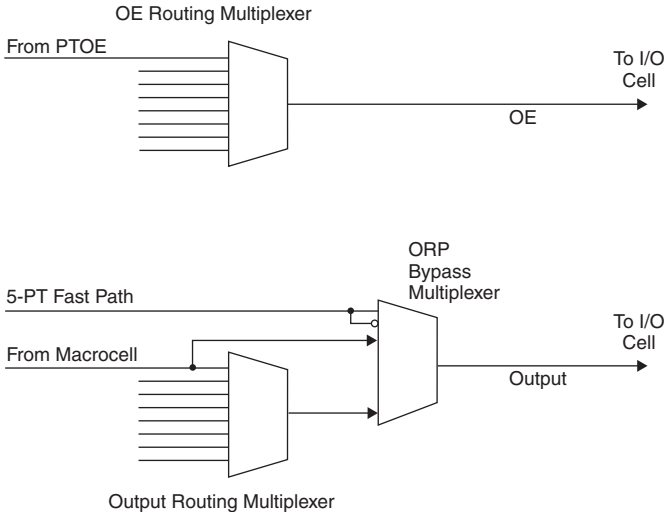
Output Routing Pool (ORP)

The Output Routing Pool allows macrocell outputs to be connected to any of several I/O cells within an I/O block. This provides greater flexibility in determining the pinout and allows design changes to occur without affecting the pinout. The output routing pool also provides a parallel capability for routing macrocell-level OE product terms. This allows the OE product term to follow the macrocell output as it is switched between I/O cells. Additionally, the output routing pool allows the macrocell output or true and complement forms of the 5-PT bypass signal to bypass the output routing multiplexers and feed the I/O cell directly. The enhanced ORP of the LA-ispMACH 4000V/Z family consists of the following elements:

- Output Routing Multiplexers
- OE Routing Multiplexers
- Output Routing Pool Bypass Multiplexers

Figure 7 shows the structure of the ORP from the I/O cell perspective. This is referred to as an ORP slice. Each ORP has as many ORP slices as there are I/O cells in the corresponding I/O block.

Figure 7. ORP Slice



Output Routing Multiplexers

The details of connections between the macrocells and the I/O cells vary across devices and within a device dependent on the maximum number of I/Os available. Tables 6-10 provide the connection details.

Table 6. ORP Combinations for I/O Blocks with 8 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M2, M3, M4, M5, M6, M7, M8, M9
I/O 2	M4, M5, M6, M7, M8, M9, M10, M11
I/O 3	M6, M7, M8, M9, M10, M11, M12, M13
I/O 4	M8, M9, M10, M11, M12, M13, M14, M15
I/O 5	M10, M11, M12, M13, M14, M15, M0, M1
I/O 6	M12, M13, M14, M15, M0, M1, M2, M3
I/O 7	M14, M15, M0, M1, M2, M3, M4, M5

Table 7. ORP Combinations for I/O Blocks with 16 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M1, M2, M3, M4, M5, M6, M7, M8
I/O 2	M2, M3, M4, M5, M6, M7, M8, M9
I/O 3	M3, M4, M5, M6, M7, M8, M9, M10
I/O 4	M4, M5, M6, M7, M8, M9, M10, M11
I/O 5	M5, M6, M7, M8, M9, M10, M11, M12
I/O 6	M6, M7, M8, M9, M10, M11, M12, M13
I/O 7	M7, M8, M9, M10, M11, M12, M13, M14
I/O 8	M8, M9, M10, M11, M12, M13, M14, M15
I/O 9	M9, M10, M11, M12, M13, M14, M15, M0
I/O 10	M10, M11, M12, M13, M14, M15, M0, M1
I/O 11	M11, M12, M13, M14, M15, M0, M1, M2
I/O 12	M12, M13, M14, M15, M0, M1, M2, M3
I/O 13	M13, M14, M15, M0, M1, M2, M3, M4
I/O 14	M14, M15, M0, M1, M2, M3, M4, M5
I/O 15	M15, M0, M1, M2, M3, M4, M5, M6

Table 8. ORP Combinations for I/O Blocks with 12 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M1, M2, M3, M4, M5, M6, M7, M8
I/O 2	M2, M3, M4, M5, M6, M7, M8, M9
I/O 3	M4, M5, M6, M7, M8, M9, M10, M11
I/O 4	M5, M6, M7, M8, M9, M10, M11, M12
I/O 5	M6, M7, M8, M9, M10, M11, M12, M13
I/O 6	M8, M9, M10, M11, M12, M13, M14, M15
I/O 7	M9, M10, M11, M12, M13, M14, M15, M0
I/O 8	M10, M11, M12, M13, M14, M15, M0, M1
I/O 9	M12, M13, M14, M15, M0, M1, M2, M3
I/O 10	M13, M14, M15, M0, M1, M2, M3, M4
I/O 11	M14, M15, M0, M1, M2, M3, M4, M5

ORP Bypass and Fast Output Multiplexers

The ORP bypass and fast-path output multiplexer is a 4:1 multiplexer and allows the 5-PT fast path to bypass the ORP and be connected directly to the pin with either the regular output or the inverted output. This multiplexer also allows the register output to bypass the ORP to achieve faster t_{CO}.

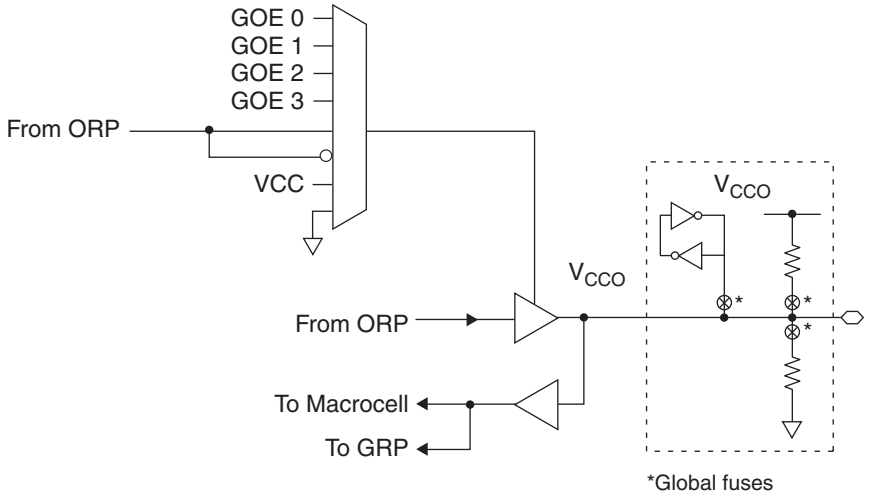
Output Enable Routing Multiplexers

The OE Routing Pool provides the corresponding local output enable (OE) product term to the I/O cell.

I/O Cell

The I/O cell contains the following programmable elements: output buffer, input buffer, OE multiplexer and bus maintenance circuitry. Figure 8 details the I/O cell.

Figure 8. I/O Cell



Each output supports a variety of output standards dependent on the V_{CCO} supplied to its I/O bank. Outputs can also be configured for open drain operation. Each input can be programmed to support a variety of standards, independent of the V_{CCO} supplied to its I/O bank. The I/O standards supported are:

- LVTTL
- LVCMOS 3.3
- LVCMOS 2.5
- LVCMOS 1.8
- 3.3V PCI Compatible

All of the I/Os and dedicated inputs have the capability to provide a bus-keeper latch, Pull-up Resistor or Pull-down Resistor. A fourth option is to provide none of these. The selection is done on a global basis. The default in both hardware and software is such that when the device is erased or if the user does not specify, the input structure is configured to be a Pull-up Resistor.

Each LA-ispMACH 4000V/Z automotive device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for fast slew or slow slew. The typical edge rate difference between fast and slow slew setting is 20%. For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed.

Global OE Generation

Most LA-ispMACH 4000V/Z automotive family devices have a 4-bit wide Global OE Bus, except the LA-ispMACH 4032V and LA-ispMACH4032Z devices that have a 2-bit wide Global OE Bus. This bus is derived from a 4-bit internal global OE PT bus and two dual purpose I/O or GOE pins. Each signal that drives the bus can optionally be inverted.

Each GLB has a block-level OE PT that connects to all bits of the Global OE PT bus with four fuses. Hence, for a 128-macrocell device (with 16 blocks), each line of the bus is driven from 8 OE product terms. Figures 9 and 10 show a graphical representation of the global OE generation.

Figure 9. Global OE Generation for All Devices Except LA-ispMACH 4032V/Z

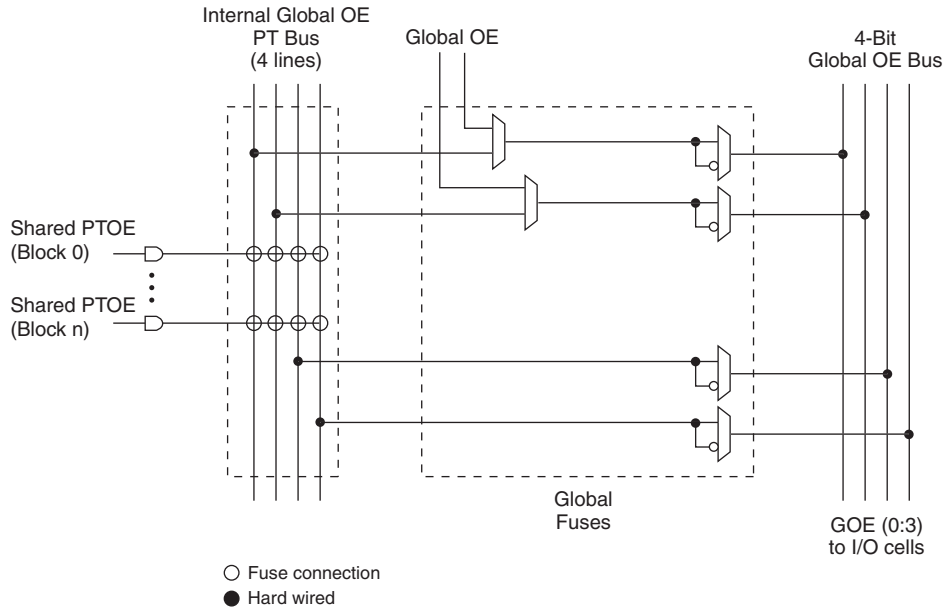
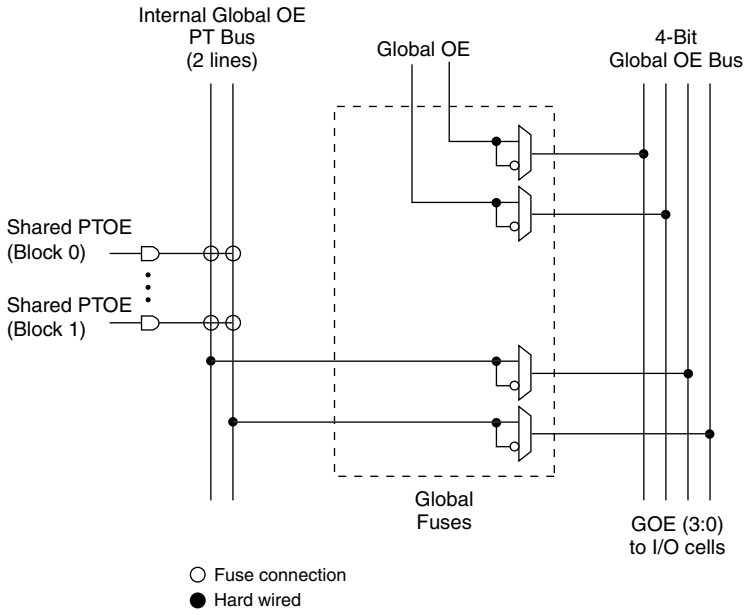


Figure 10. Global OE Generation for LA-ispMACH 4032V/Z



Zero Power/Low Power and Power Management

The LA-ispMACH 4000V/Z automotive family is designed with high speed low power design techniques to offer both high speed and low power. With an advanced E^2 low power cell and non sense-amplifier design approach (full CMOS logic approach), the LA-ispMACH 4000V/Z automotive family offers SuperFAST pin-to-pin speeds, while simultaneously delivering low standby power without needing any “turbo bits” or other power management schemes associated with a traditional sense-amplifier approach.

The zero power LA-ispMACH 4000Z is based on the 1.8V ispMACH 4000C family. With innovative circuit design changes, the LA-ispMACH 4000Z family is able to achieve the industry's "lowest static power".

IEEE 1149.1-Compliant Boundary Scan Testability

All LA-ispMACH 4000V/Z automotive devices have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic notes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more board-level testing. The test access port operates with an LVCMOS interface that corresponds to the power supply voltage.

I/O Quick Configuration

To facilitate the most efficient board test, the physical nature of the I/O cells must be set before running any continuity tests. As these tests are fast, by nature, the overhead and time that is required for configuration of the I/Os' physical nature should be minimal so that board test time is minimized. The LA-ispMACH 4000V/Z automotive family of devices allows this by offering the user the ability to quickly configure the physical nature of the I/O cells. This quick configuration takes milliseconds to complete, whereas it takes seconds for the entire device to be programmed. Lattice's ispVM™ System programming software can either perform the quick configuration through the PC parallel port, or can generate the ATE or test vectors necessary for a third-party test system.

IEEE 1532-Compliant In-System Programming

Programming devices in-system provides a number of significant benefits including: rapid prototyping, lower inventory levels, higher quality and the ability to make in-field modifications. The LA-ispMACH 4000V/Z automotive devices provide In-System Programming (ISP™) capability through the Boundary Scan Test Access Port. This capability has been implemented in a manner that ensures that the port remains complaint to the IEEE 1149.1 standard. By using IEEE 1149.1 as the communication interface through which ISP is achieved, users get the benefit of a standard, well-defined interface. All LA-ispMACH 4000V/Z automotive devices are also compliant with the IEEE 1532 standard.

The LA-ispMACH 4000V/Z automotive devices can be programmed across the commercial temperature and voltage range. The PC-based Lattice software facilitates in-system programming of LA-ispMACH 4000V/Z automotive devices. The software takes the JEDEC file output produced by the design implementation software, along with information about the scan chain, and creates a set of vectors used to drive the scan chain. The software can use these vectors to drive a scan chain via the parallel port of a PC. Alternatively, the software can output files in formats understood by common automated test equipment. This equipment can then be used to program LA-ispMACH 4000V/Z automotive devices during the testing of a circuit board.

User Electronic Signature

The User Electronic Signature (UES) allows the designer to include identification bits or serial numbers inside the device, stored in E^2CMOS memory. The LA-ispMACH 4000V/Z automotive device contains 32 UES bits that can be configured by the user to store unique data such as ID codes, revision numbers or inventory control codes.

Security Bit

A programmable security bit is provided on the LA-ispMACH 4000V/Z automotive devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

Hot Socketing

The LA-ispMACH 4000V/Z automotive devices are well-suited for applications that require hot socketing capability. Hot socketing a device requires that the device, during power-up and down, can tolerate active signals on the I/Os

and inputs without being damaged. Additionally, it requires that the effects of I/O pin loading be minimal on active signals. The LA-ispMACH 4000V/Z automotive devices provide this capability for input voltages in the range 0V to 3.0V.

Density Migration

The LA-ispMACH 4000V/Z automotive family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is possible to shift a lower utilization design targeted for a high density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

AEC-Q100 Tested and Qualified

The Automotive Electronics Council (AEC) consists of two committees: the Quality Systems Committee and the Component Technical Committee. These committees are composed of representatives from sustaining and other associate members. The AEC Component Technical Committee is the standardization body for establishing standards for reliable, high quality electronic components. In particular, the AEC-Q100 specification “Stress Test for Qualification for Integrated Circuits” defines qualification and re-qualification requirements for electronic components. Components meeting these specifications are suitable for use in the harsh automotive environment without additional component-level qualification testing. Lattice's LA-ispMACH 4000V/Z and LA-MachXO devices completed and passed the requirements of the AEC-Q100 specification.

Absolute Maximum Ratings[1, 2, 3]

	LA-ispMACH 4000V (3.3V)	LA-ispMACH 4000Z (1.8V)
Supply Voltage (V_{CC})	-0.5 to 5.5V	-0.5 to 2.5V
Output Supply Voltage (V_{CCO})	-0.5 to 4.5V	-0.5 to 4.5V
Input or I/O Tristate Voltage Applied[4, 5]	-0.5 to 5.5V	-0.5 to 5.5V
Storage Temperature	-65 to 150°C	-65 to 150°C
Junction Temperature (T_j) with Power Applied	-55 to 150°C	-55 to 150°C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Undershoot of -2V and overshoot of (V_{IH} (MAX) + 2V), up to a total pin voltage of 6.0V, is permitted for a duration of < 20ns.
5. Maximum of 64 I/Os per device with VIN > 3.6V is allowed.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V_{CC}	LA-ispMACH 4000V Supply Voltage	3.0	3.6	V
	LA-ispMACH 4000Z Supply Voltage	1.7	1.9	V
	LA-ispMACH 4000Z, Extended Functional Voltage Operations	1.6[1]	1.9	V
T_A	Ambient Temperature (Automotive)	-40	125	C

1. Devices operating at 1.6V can expect performance degradation up to 35%.

Erase Reprogram Specifications

Parameter	Min.	Max.	Units
Erase/Reprogram Cycle	1,000	—	Cycles

Note: Valid over commercial temperature range.

Hot Socketing Characteristics[1,2,3]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DK}	Input or I/O Leakage Current	$0 \le V_{IN} \le 3.0V$, Tj = 105°C	—	±30	±150	µA
		$0 \le V_{IN} \le 3.0V$, Tj = 130°C	—	±30	±200	µA

1. Insensitive to sequence of V_{CC} or V_{CCO}. However, assumes monotonic rise/fall rates for V_{CC} and V_{CCO}, provided (V_{IN} - V_{CCO}) ≤ 3.6V.
2. $0 < V_{CC} < V_{CC}$ (MAX), $0 < V_{CCO} < V_{CCO}$ (MAX).
3. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}. Device defaults to pull-up until fuse circuitry is active.

I/O Recommended Operating Conditions

Standard	V_{CCO} (V)[1]	
	Min.	Max.
LVTTL	3.0	3.6
LVCMOS 3.3	3.0	3.6
Extended LVCMOS 3.3[2]	2.7	3.6
LVCMOS 2.5	2.3	2.7
LVCMOS 1.8	1.65	1.95
PCI 3.3	3.0	3.6

1. Typical values for V_{CCO} are the average of the min. and max. values.
2. LA-ispMACH 4000Z only.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1, 4]	Input Leakage Current (LA-ispMACH 4000Z)	$0 \le V_{IN} < V_{CCO}$	—	0.5	1	µA
I_{IH}[1, 2]	Input High Leakage Current (LA-ispMACH 4000V)	$3.6V < V_{IN} \le 5.5V$, $T_j = 105°C$ $3.0V \le V_{CCO} \le 3.6V$	—	—	20	µA
		$3.6V < V_{IN} \le 5.5V$, $T_j = 130°C$ $3.0V \le V_{CCO} \le 3.6V$	—	—	50	µA
	Input High Leakage Current (LA-ispMACH 4000Z)	$V_{CCO} < V_{IN} \le 5.5V$	—	—	10	µA
I_{PU}	I/O Weak Pull-up Resistor Current (LA-ispMACH 4000V)	$0 \le V_{IN} \le 0.7V_{CCO}$	-30	—	-200	µA
	I/O Weak Pull-up Resistor Current (LA-ispMACH 4000Z)	$0 \le V_{IN} \le 0.7V_{CCO}$	-30	—	-150	µA
I_{PD}	I/O Weak Pull-down Resistor Current	V_{IL} (MAX) $\le V_{IN} \le V_{IH}$ (MIN)	30	—	150	µA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7\ V_{CCO}$	-30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive Current	$0V \le V_{IN} \le V_{BHT}$	—	—	150	µA
I_{BHHO}	Bus Hold High Overdrive Current	$V_{BHT} \le V_{IN} \le V_{CCO}$	—	—	-150	µA
V_{BHT}	Bus Hold Trip Points	—	V_{CCO} * 0.35	—	V_{CCO} * 0.65	V
C_1	I/O Capacitance[3]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	8	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	
C_2	Clock Capacitance[3]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	6	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	
C_3	Global Input Capacitance[3]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	6	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. 5V tolerant inputs and I/O should only be placed in banks where $3.0V \le V_{CCO} \le 3.6V$.
3. $T_A = 25°C$, f = 1.0MHz.
4. I_{IH} excursions of up to 1.5µA maximum per pin above the spec limit may be observed for certain voltage conditions on no more than 10% of the device's I/O pins.

Supply Current, LA-ispMACH 4000V

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
LA-ispMACH 4032V						
ICC	Operating Power Supply Current	Vcc = 3.3V	—	11.8	—	mA
	Standby Power Supply Current	Vcc = 3.3V	—	11.3	—	mA
LA-ispMACH 4064V						
ICC	Operating Power Supply Current	Vcc = 3.3V	—	12	—	mA
	Standby Power Supply Current	Vcc = 3.3V	—	11.5	—	mA
LA-ispMACH 4128V						
ICC	Operating Power Supply Current	Vcc = 3.3V	—	12	—	mA
	Standby Power Supply Current	Vcc = 3.3V	—	11.5	—	mA

Supply Current, LA-ispMACH 4000Z

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
LA-ispMACH 4032Z						
ICC[1, 2, 3, 5]	Operating Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	50	—	µA
		Vcc = 1.9V, T_A = 70°C	—	58	—	µA
		Vcc = 1.9V, T_A = 85°C	—	60	—	µA
		Vcc = 1.9V, T_A = 125°C	—	70	—	µA
ICC[4, 5]	Standby Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	10	—	µA
		Vcc = 1.9V, T_A = 70°C	—	13	20	µA
		Vcc = 1.9V, T_A = 85°C	—	15	25	µA
		Vcc = 1.9V, T_A = 125°C	—	22		µA
LA-ispMACH 4064Z						
ICC[1, 2, 3, 5]	Operating Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	80	—	µA
		Vcc = 1.9V, T_A = 70°C	—	89	—	µA
		Vcc = 1.9V, T_A = 85°C	—	92	—	µA
		Vcc = 1.9V, T_A = 125°C	—	109	—	µA
ICC[4, 5]	Standby Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	11	—	µA
		Vcc = 1.9V, T_A = 70°C	—	15	25	µA
		Vcc = 1.9V, T_A = 85°C	—	18	35	µA
		Vcc = 1.9V, T_A = 125°C	—	37		µA
LA-ispMACH 4128Z						
ICC[1, 2, 3, 5]	Operating Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	168	—	µA
		Vcc = 1.9V, T_A = 70°C	—	190	—	µA
		Vcc = 1.9V, T_A = 85°C	—	195	—	µA
		Vcc = 1.9V, T_A = 125°C	—	212	—	µA
ICC[4, 5]	Standby Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	12	—	µA
		Vcc = 1.9V, T_A = 70°C	—	16	35	µA
		Vcc = 1.9V, T_A = 85°C	—	19	50	µA
		Vcc = 1.9V, T_A = 125°C	—	42	—	µA

1. T_A = 25°C, frequency = 1.0 MHz.
2. Device configured with 16-bit counters.
3. I_{CC} varies with specific device configuration and operating frequency.
4. V_{CCO} = 3.6V, V_{IN} = 0V or $V_{CCO,}$ bus maintenance turned off. V_{IN} above V_{CCO} will add transient current above the specified standby I_{CC}.
5. Includes V_{CCO} current without output loading.

LA-ispMACH 4000V/Z External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description[1, 2, 3]	LA-ispMACH 4000V -75		LA-ispMACH 4000Z -75		Units
		Min.	Max.	Min.	Max.	
t_{PD}	5-PT bypass combinatorial propagation delay	—	7.5	—	7.5	ns
t_{PD_MC}	20-PT combinatorial propagation delay through macrocell	—	8.0	—	8.0	ns
t_S	GLB register setup time before clock	4.5	—	4.5	—	ns
t_{ST}	GLB register setup time before clock with T-type register	4.7	—	4.7	—	ns
t_{SIR}	GLB register setup time before clock, input register path	1.7	—	1.4	—	ns
t_{SIRZ}	GLB register setup time before clock with zero hold	2.7	—	2.7	—	ns
t_H	GLB register hold time after clock	0.0	—	0.0	—	ns
t_{HT}	GLB register hold time after clock with T-type register	0.0	—	0.0	—	ns
t_{HIR}	GLB register hold time after clock, input register path	1.0	—	1.3	—	ns
t_{HIRZ}	GLB register hold time after clock, input register path with zero hold	0.0	—	0.0	—	ns
t_{CO}	GLB register clock-to-output delay	—	4.5	—	4.5	ns
t_R	External reset pin to output delay	—	9.0	—	9.0	ns
t_{RW}	External reset pulse duration	4.0	—	4.0	—	ns
$t_{PTOE/DIS}$	Input to output local product term output enable/disable	—	9.0	—	9.0	ns
$t_{GPTOE/DIS}$	Input to output global product term output enable/disable	—	10.3	—	10.5	ns
$t_{GOE/DIS}$	Global OE input to output enable/disable	—	7.0	—	7.0	ns
t_{CW}	Global clock width, high or low	2.8	—	2.8	—	ns
t_{GW}	Global gate width low (for low transparent) or high (for high transparent)	2.8	—	2.8	—	ns
t_{WIR}	Input register clock width, high or low	2.8	—	2.8	—	ns
f_{MAX}[4]	Clock frequency with internal feedback	—	168	—	168	MHz
f_{MAX} (Ext.)	Clock frequency with external feedback, [1/ (t_S + t_{CO})]	—	111	—	111	MHz

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.
2. Measured using standard switching circuit, assuming GRP loading of 1 and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using GRP feedback.

Timing v.3.2

LA-ispMACH 4000V/Z Internal Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	LA-ispMACH 4000V -75		LA-ispMACH 4000Z -75		Units
		Min.	Max.	Min.	Max.	
In/Out Delays						
t_{IN}	Input Buffer Delay	—	1.50	—	1.80	ns
t_{GOE}	Global OE Pin Delay	—	6.04	—	4.30	ns
t_{GCLK_IN}	Global Clock Input Buffer Delay	—	2.28	—	2.15	ns
t_{BUF}	Delay through Output Buffer	—	1.50	—	1.30	ns
t_{EN}	Output Enable Time	—	0.96	—	2.70	ns
t_{DIS}	Output Disable Time	—	0.96	—	2.70	ns
Routing/GLB Delays						
t_{ROUTE}	Delay through GRP	—	2.26	—	2.50	ns
t_{MCELL}	Macrocell Delay	—	1.45	—	1.00	ns
t_{INREG}	Input Buffer to Macrocell Register Delay	—	0.96	—	1.00	ns
t_{FBK}	Internal Feedback Delay	—	0.00	—	0.05	ns
t_{PDb}	5-PT Bypass Propagation Delay	—	2.24	—	1.90	ns
t_{PDi}	Macrocell Propagation Delay	—	1.24	—	1.00	ns
Register/Latch Delays						
t_{S}	D-Register Setup Time (Global Clock)	1.57	—	1.35	—	ns
t_{S_PT}	D-Register Setup Time (Product Term Clock)	1.32	—	2.45	—	ns
t_{ST}	T-Register Setup Time (Global Clock)	1.77	—	1.55	—	ns
t_{ST_PT}	T-Register Setup Time (Product Term Clock)	1.32	—	2.75	—	ns
t_{H}	D-Register Hold Time	2.93	—	3.15	—	ns
t_{HT}	T-Register Hold Time	2.93	—	3.15	—	ns
t_{SIR}	D-Input Register Setup Time (Global Clock)	1.57	—	0.75	—	ns
t_{SIR_PT}	D-Input Register Setup Time (Product Term Clock)	1.45	—	1.45	—	ns
t_{HIR}	D-Input Register Hold Time (Global Clock)	1.18	—	1.95	—	ns
t_{HIR_PT}	D-Input Register Hold Time (Product Term Clock)	1.18	—	1.18	—	ns
t_{COi}	Register Clock to Output/Feedback MUX Time	—	0.67	—	1.05	ns
t_{CES}	Clock Enable Setup Time	2.25	—	2.00	—	ns
t_{CEH}	Clock Enable Hold Time	1.88	—	0.00	—	ns
t_{SL}	Latch Setup Time (Global Clock)	1.57	—	1.65	—	ns
t_{SL_PT}	Latch Setup Time (Product Term Clock)	1.32	—	2.15	—	ns
t_{HL}	Latch Hold Time	1.17	—	1.17	—	ns
t_{GOi}	Latch Gate to Output/Feedback MUX Time	—	0.33	—	0.33	ns
t_{PDLi}	Propagation Delay through Transparent Latch to Output/Feedback MUX	—	0.25	—	0.25	ns
t_{SRi}	Asynchronous Reset or Set to Output/Feedback MUX Delay	0.28	—	—	0.28	ns
t_{SRR}	Asynchronous Reset or Set Recovery Time	1.67	—	—	1.67	ns
Control Delays						
t_{BCLK}	GLB PT Clock Delay	—	1.12	—	1.25	ns
t_{PTCLK}	Macrocell PT Clock Delay	—	0.87	—	1.25	ns

LA-ispMACH 4000V/Z Timing Adders[1]

Adder Type	Base Parameter	Description	LA-ispMACH 4000V -75		LA-ispMACH 4000Z -75		Units
			Min.	Max.	Min.	Max.	
Optional Delay Adders							
t_{INDIO}	t_{INREG}	Input register delay	—	1.00	—	1.30	ns
t_{EXP}	t_{MCELL}	Product term expander delay	—	0.33	—	0.50	ns
t_{ORP}	—	Output routing pool delay	—	0.05	—	0.40	ns
t_{BLA}	t_{ROUTE}	Additional block loading adder	—	0.05	—	0.05	ns
t_{IOI} Input Adjusters							
LVTTL_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVTTL standard	—	0.60	—	0.60	ns
LVCMOS33_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 3.3 standard	—	0.60	—	0.60	ns
LVCMOS25_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 2.5 standard	—	0.60	—	0.60	ns
LVCMOS18_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 1.8 standard	—	0.00	—	0.00	ns
PCI_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using PCI compatible input	—	0.60	—	0.60	ns
t_{IOO} Output Adjusters							
LVTTL_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as TTL buffer	—	0.20	—	0.20	ns
LVCMOS33_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V buffer	—	0.20	—	0.20	ns
LVCMOS25_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 2.5V buffer	—	0.10	—	0.10	ns
LVCMOS18_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 1.8V buffer	—	0.00	—	0.00	ns
PCI_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as PCI compatible buffer	—	0.20	—	0.20	ns
Slow Slew	t_{BUF}, t_{EN}	Output configured for slow slew rate	—	1.00	—	1.00	ns

Note: Open drain timing is the same as corresponding LVCMOS timing.

Timing v.3.2

1. Refer to TN1004, ispMACH 4000 Timing Model Design and Usage Guidelines for information regarding use of these adders.

Boundary Scan Waveforms and Timing Specifications

Symbol	Parameter	Min.	Max.	Units
t_{BTCP}	TCK [BSCAN test] clock cycle	40	—	ns
t_{BTCH}	TCK [BSCAN test] pulse width high	20	—	ns
t_{BTCL}	TCK [BSCAN test] pulse width low	20	—	ns
t_{BTSU}	TCK [BSCAN test] setup time	8	—	ns
t_{BTH}	TCK [BSCAN test] hold time	10	—	ns
t_{BRF}	TCK [BSCAN test] rise and fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
t_{BTOZ}	TAP controller falling edge of clock to data output disable	—	10	ns
t_{BTVO}	TAP controller falling edge of clock to data output enable	—	10	ns
t_{BTCPSU}	BSCAN test Capture register setup time	8	—	ns
t_{BTCPH}	BSCAN test Capture register hold time	10	—	ns
t_{BTUCO}	BSCAN test Update reg, falling edge of clock to valid output	—	25	ns
t_{BTUOZ}	BSCAN test Update reg, falling edge of clock to output disable	—	25	ns
t_{BTUOV}	BSCAN test Update reg, falling edge of clock to output enable	—	25	ns

LA-ispMACH 4032V and 4064V Logic Signal Connections: 44-Pin TQFP

Pin Number	Bank Number	LA-ispMACH 4032V		LA-ispMACH 4064V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
43	0	A3	A^3	A6	A^3
44	0	A4	A^4	A8	A^4

LA-ispMACH 4032V/Z and 4064V/Z Logic Signal Connections: 48-Pin TQFP

Pin Number	Bank Number	LA-ispMACH 4032V/Z		LA-ispMACH 4064V/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	TDI	-	TDI	-
2	0	A5	A^5	A10	A^5
3	0	A6	A^6	A12	A^6
4	0	A7	A^7	A14	A^7
5	0	GND (Bank 0)	-	GND (Bank 0)	-
6	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
7	0	A8	A^8	B0	B^0
8	0	A9	A^9	B2	B^1
9	0	A10	A^10	B4	B^2
10	0	A11	A^11	B6	B^3
11	-	TCK	-	TCK	-
12	-	VCC	-	VCC	-
13	-	GND	-	GND	-
14	0	A12	A^12	B8	B^4
15	0	A13	A^13	B10	B^5
16	0	A14	A^14	B12	B^6
17	0	A15	A^15	B14	B^7
18	0	CLK1/I	-	CLK1/I	-
19	1	CLK2/I	-	CLK2/I	-
20	1	B0	B^0	C0	C^0
21	1	B1	B^1	C2	C^1
22	1	B2	B^2	C4	C^2
23	1	B3	B^3	C6	C^3
24	1	B4	B^4	C8	C^4
25	-	TMS	-	TMS	-
26	1	B5	B^5	C10	C^5
27	1	B6	B^6	C12	C^6
28	1	B7	B^7	C14	C^7
29	1	GND (Bank 1)	-	GND (Bank 1)	-
30	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
31	1	B8	B^8	D0	D^0
32	1	B9	B^9	D2	D^1
33	1	B10	B^10	D4	D^2
34	1	B11	B^11	D6	D^3
35	-	TDO	-	TDO	-

LA-ispMACH 4032V/Z and 4064V/Z Logic Signal Connections: 48-Pin TQFP

Pin Number	Bank Number	LA-ispMACH 4032V/Z		LA-ispMACH 4064V/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
36	-	VCC	-	VCC	-
37	-	GND	-	GND	-
38	1	B12	B^12	D8	D^4
39	1	B13	B^13	D10	D^5
40	1	B14	B^14	D12	D^6
41	1	B15/GOE1	B^15	D14/GOE1	D^7
42	1	CLK3/I	-	CLK3/I	-
43	0	CLK0/I	-	CLK0/I	-
44	0	A0/GOE0	A^0	A0/GOE0	A^0
45	0	A1	A^1	A2	A^1
46	0	A2	A^2	A4	A^2
47	0	A3	A^3	A6	A^3
48	0	A4	A^4	A8	A^4

LA-ispMACH 4064V/Z and 4128V/Z Logic Signal Connections: 100-Pin TQFP

Pin Number	Bank Number	LA-ispMACH 4064V/Z		LA-ispMACH 4128V/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	GND	-	GND	-
2	-	TDI	-	TDI	-
3	0	A8	A^8	B0	B^0
4	0	A9	A^9	B2	B^1
5	0	A10	A^10	B4	B^2
6	0	A11	A^11	B6	B^3
7	0	GND (Bank 0)	-	GND (Bank 0)	-
8	0	A12	A^12	B8	B^4
9	0	A13	A^13	B10	B^5
10	0	A14	A^14	B12	B^6
11	0	A15	A^15	B13	B^7
12*	0	I	-	I	-
13	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
14	0	B15	B^15	C14	C^7
15	0	B14	B^14	C12	C^6
16	0	B13	B^13	C10	C^5
17	0	B12	B^12	C8	C^4
18	0	GND (Bank 0)	-	GND (Bank 0)	-
19	0	B11	B^11	C6	C^3
20	0	B10	B^10	C5	C^2
21	0	B9	B^9	C4	C^1
22	0	B8	B^8	C2	C^0
23*	0	I	-	I	-
24	-	TCK	-	TCK	-

LA-ispMACH 4128V Logic Signal Connections: 128-Pin TQFP (Cont.)

Pin Number	Bank Number	LA-ispMACH 4128V	
		GLB/MC/Pad	ORP
43	0	D5	D^4
44	0	D4	D^3
45	0	D2	D^2
46	0	D1	D^1
47	0	D0	D^0
48	0	CLK1/I	-
49	1	GND (Bank 1)	-
50	1	CLK2/I	-
51	1	VCC	-
52	1	E0	E^0
53	1	E1	E^1
54	1	E2	E^2
55	1	E4	E^3
56	1	E5	E^4
57	1	E6	E^5
58	1	VCCO (Bank 1)	-
59	1	GND (Bank 1)	-
60	1	E8	E^6
61	1	E9	E^7
62	1	E10	E^8
63	1	E12	E^9
64	1	E14	E^11
65	1	GND	-
66	1	TMS	-
67	1	VCCO (Bank 1)	-
68	1	F0	F^0
69	1	F1	F^1
70	1	F2	F^2
71	1	F4	F^3
72	1	F5	F^4
73	1	F6	F^5
74	1	GND (Bank 1)	-
75	1	F8	F^6
76	1	F9	F^7
77	1	F10	F^8
78	1	F12	F^9
79	1	F13	F^10
80	1	F14	F^11
81	1	VCCO (Bank 1)	-
82	1	G14	G^11
83	1	G13	G^10
84	1	G12	G^9
85	1	G10	G^8

LA-ispMACH 4128V Logic Signal Connections: 128-Pin TQFP (Cont.)

Pin Number	Bank Number	LA-ispMACH 4128V	
		GLB/MC/Pad	ORP
86	1	G9	G^7
87	1	G8	G^6
88	1	GND (Bank 1)	-
89	1	G6	G^5
90	1	G5	G^4
91	1	G4	G^3
92	1	G2	G^2
93	1	G0	G^0
94	1	VCCO (Bank 1)	-
95	1	TDO	-
96	1	VCC	-
97	1	GND	-
98	1	H14	H^11
99	1	H13	H^10
100	1	H12	H^9
101	1	H10	H^8
102	1	H9	H^7
103	1	H8	H^6
104	1	GND (Bank 1)	-
105	1	VCCO (Bank 1)	-
106	1	H6	H^5
107	1	H5	H^4
108	1	H4	H^3
109	1	H2	H^2
110	1	H1	H^1
111	1	H0/GOE1	H^0
112	1	CLK3/I	-
113	0	GND (Bank 0)	-
114	0	CLK0/I	-
115	0	VCC	-
116	0	A0/GOE0	A^0
117	0	A1	A^1
118	0	A2	A^2
119	0	A4	A^3
120	0	A5	A^4
121	0	A6	A^5
122	0	VCCO (Bank 0)	-
123	0	GND (Bank 0)	-
124	0	A8	A^6
125	0	A9	A^7
126	0	A10	A^8
127	0	A12	A^9
128	0	A14	A^11

LA-ispMACH 4128V Logic Signal Connections: 144-Pin TQFP (Cont.)

Pin Number	Bank Number	LA-ispMACH 4128V	
		GLB/MC/Pad	ORP
86	1	F12	F^9
87	1	F13	F^10
88	1	F14	F^11
89	1	NC	-
90	1	GND (Bank 1)[1]	-
91	1	VCCO (Bank 1)	-
92	1	NC	-
93	1	G14	G^11
94	1	G13	G^10
95	1	G12	G^9
96	1	G10	G^8
97	1	G9	G^7
98	1	G8	G^6
99	1	GND (Bank 1)	-
100	1	G6	G^5
101	1	G5	G^4
102	1	G4	G^3
103	1	G2	G^2
104	1	G1	G^1
105	1	G0	G^0
106	1	VCCO (Bank 1)	-
107	-	TDO	-
108	-	VCC	-
109	-	GND	-
110	1	NC	-
111	1	H14	H^11
112	1	H13	H^10
113	1	H12	H^9
114	1	H10	H^8
115	1	H9	H^7
116	1	H8	H^6
117	1	NC	-
118	1	GND (Bank 1)	-
119	1	VCCO (Bank 1)	-
120	1	H6	H^5
121	1	H5	H^4
122	1	H4	H^3
123	1	H2	H^2
124	1	H1	H^1
125	1	H0/GOE1	H^0
126	1	CLK3/I	-
127	0	GND (Bank 0)	-
128	0	CLK0/I	-

LA-ispMACH 4128V Logic Signal Connections: 144-Pin TQFP (Cont.)

Pin Number	Bank Number	LA-ispMACH 4128V	
		GLB/MC/Pad	ORP
129	-	VCC	-
130	0	A0/GOE0	A^0
131	0	A1	A^1
132	0	A2	A^2
133	0	A4	A^3
134	0	A5	A^4
135	0	A6	A^5
136	0	VCCO (Bank 0)	-
137	0	GND (Bank 0)	-
138	0	A8	A^6
139	0	A9	A^7
140	0	A10	A^8
141	0	A12	A^9
142	0	A13	A^10
143	0	A14	A^11
144	0	NC[2]	-

1. For device migration considerations, these NC pins are GND pins for I/O banks in LA-ispMACH 4128V devices.