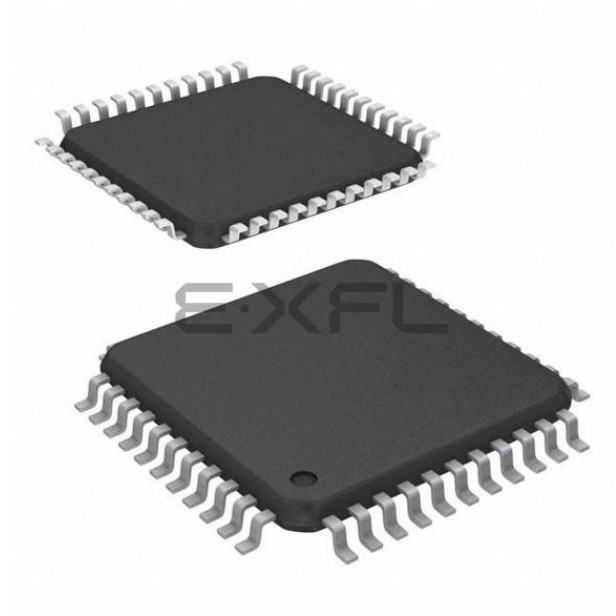
Lattice Semiconductor Corporation - LA4064V-75TN44E Datasheet



Welcome to E-XFL.COM

Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	-
Number of Macrocells	64
Number of Gates	-
Number of I/O	30
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/la4064v-75tn44e

The I/Os in the LA-ispMACH 4000V/Z automotive devices are split into two banks. Each bank has a separate I/O power supply. Inputs can support a variety of standards independent of the chip or bank power supply. Outputs support the standards compatible with the power supply provided to the bank. Support for a variety of standards helps designers implement designs in mixed voltage environments. In addition, 5V tolerant inputs are specified within an I/O bank that is connected to V_{CCO} of 3.0V to 3.6V for LVCMOS 3.3, LVTTL and PCI interfaces.

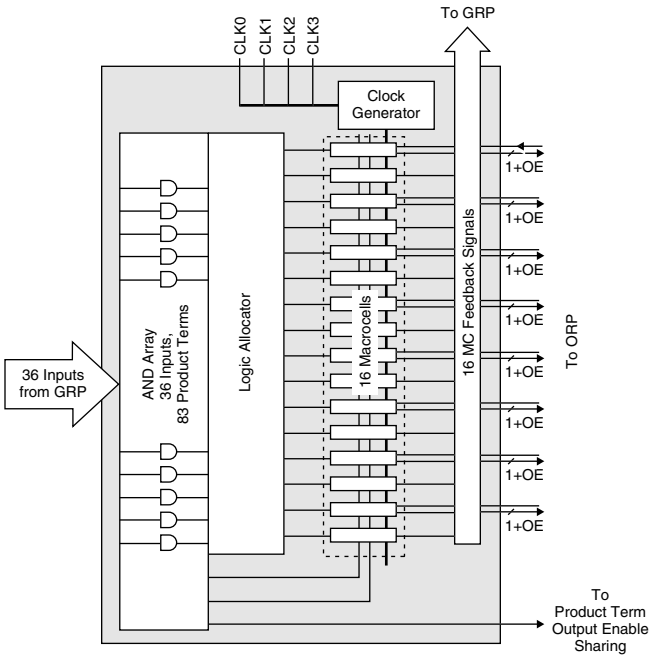
LA-ispMACH 4000V/Z Automotive Architecture

There are a total of two GLBs in the LA-ispMACH 4032V/Z, increasing to 8 GLBs in the LA-ispMACH 4128V/Z. Each GLB has 36 inputs. All GLB inputs come from the GRP and all outputs from the GLB are brought back into the GRP to be connected to the inputs of any other GLB on the device. Even if feedback signals return to the same GLB, they still must go through the GRP. This mechanism ensures that GLBs communicate with each other with consistent and predictable delays. The outputs from the GLB are also sent to the ORP. The ORP then sends them to the associated I/O cells in the I/O block.

Generic Logic Block

The LA-ispMACH 4000V/Z Automotive GLB consists of a programmable AND array, logic allocator, 16 macrocells and a GLB clock generator. Macrocells are decoupled from the product terms through the logic allocator and the I/O pins are decoupled from macrocells through the ORP. Figure 2 illustrates the GLB.

Figure 2. Generic Logic Block



AND Array

The programmable AND Array consists of 36 inputs and 83 output product terms. The 36 inputs from the GRP are used to form 72 lines in the AND Array (true and complement of the inputs). Each line in the array can be connected to any of the 83 output product terms via a wired-AND. Each of the 80 logic product terms feed the logic allocator with the remaining three control product terms feeding the Shared PT Clock, Shared PT Initialization and Shared PT OE. The Shared PT Clock and Shared PT Initialization signals can optionally be inverted before being fed to the macrocells.

Every set of five product terms from the 80 logic product terms forms a product term cluster starting with PT0. There is one product term cluster for every macrocell in the GLB. Figure 3 is a graphical representation of the AND Array.

Table 5. Product Term Expansion Capability

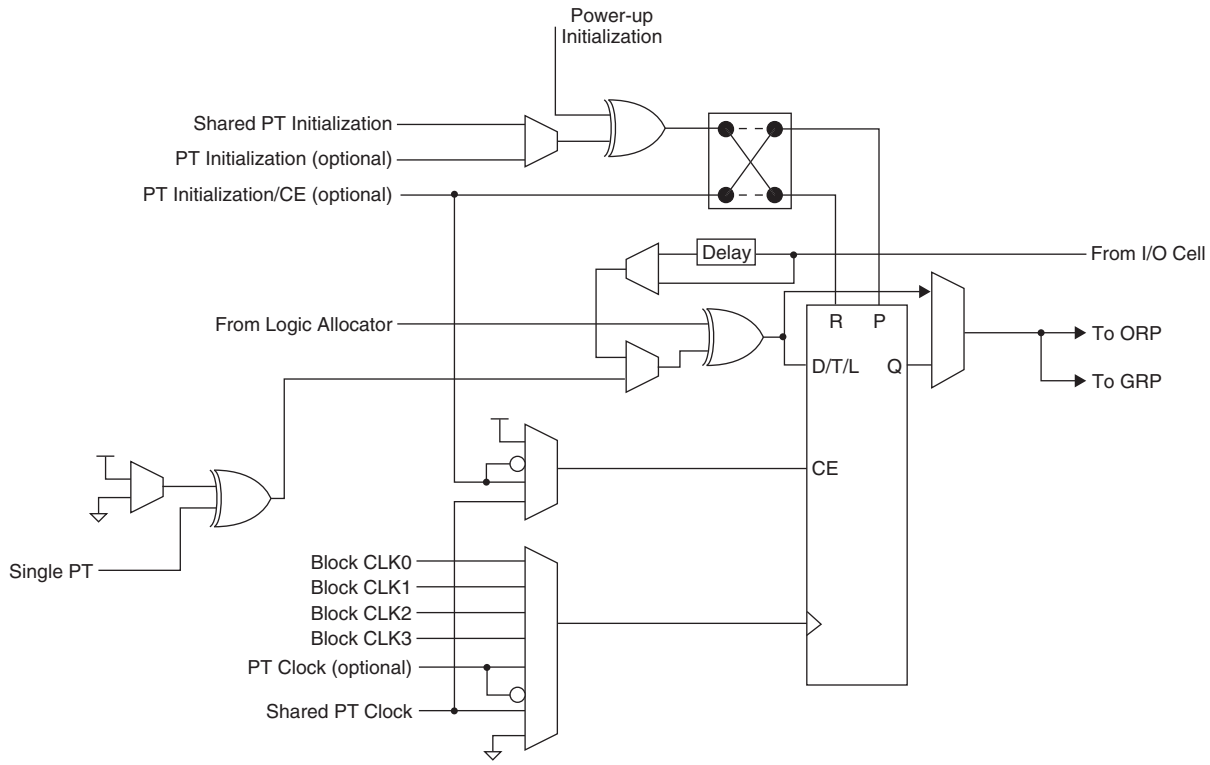
Expansion Chains	Macrocells Associated with Expansion Chain (with Wrap Around)	Max PT/Macrocell
Chain-0	M0 → M4 → M8 → M12 → M0	75
Chain-1	M1 → M5 → M9 → M13 → M1	80
Chain-2	M2 → M6 → M10 → M14 → M2	75
Chain-3	M3 → M7 → M11 → M15 → M3	70

Every time the super cluster allocator is used, there is an incremental delay of t_{EXP}. When the super cluster allocator is used, all destinations other than the one being steered to, are given the value of ground (i.e., if the super cluster is steered to M (n+4), then M (n) is ground).

Macrocell

The 16 macrocells in the GLB are driven by the 16 outputs from the logic allocator. Each macrocell contains a programmable XOR gate, a programmable register/latch, along with routing for the logic and control functions. Figure 5 shows a graphical representation of the macrocell. The macrocells feed the ORP and GRP. A direct input from the I/O cell allows designers to use the macrocell to construct high-speed input registers. A programmable delay in this path allows designers to choose between the fastest possible set-up time and zero hold time.

Figure 5. Macrocell



Enhanced Clock Multiplexer

The clock input to the flip-flop can select any of the four block clocks along with the shared PT clock, and true and complement forms of the optional individual term clock. An 8:1 multiplexer structure is used to select the clock. The eight sources for the clock multiplexer are as follows:

- Block CLK0
- Block CLK1
- Block CLK2

- Block CLK3
- PT Clock
- PT Clock Inverted
- Shared PT Clock
- Ground

Clock Enable Multiplexer

Each macrocell has a 4:1 clock enable multiplexer. This allows the clock enable signal to be selected from the following four sources:

- PT Initialization/CE
- PT Initialization/CE Inverted
- Shared PT Clock
- Logic High

Initialization Control

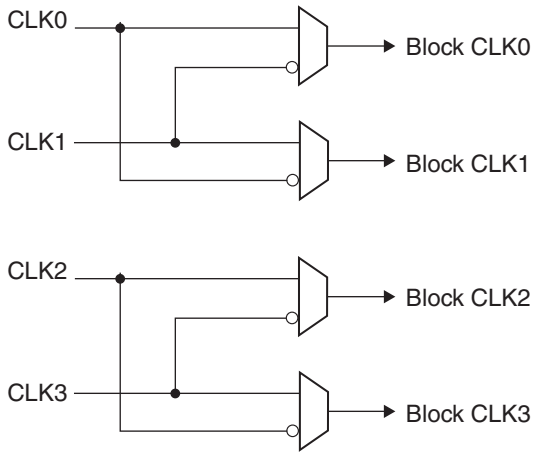
The LA-ispMACH 4000V/Z automotive family architecture accommodates both block-level and macrocell-level set and reset capability. There is one block-level initialization term that is distributed to all macrocell registers in a GLB. At the macrocell level, two product terms can be "stolen" from the cluster associated with a macrocell to be used for set/reset functionality. A reset/preset swapping feature in each macrocell allows for reset and preset to be exchanged, providing flexibility.

Note that the reset/preset swapping selection feature affects power-up reset as well. All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the block-level initialization, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the block-level initialization or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the V_{CC} rise must be monotonic, and the clock must be inactive until the reset delay time has elapsed.

GLB Clock Generator

Each LA-ispMACH 4000V/Z automotive device has up to four clock pins that are also routed to the GRP to be used as inputs. These pins drive a clock generator in each GLB, as shown in Figure 6. The clock generator provides four clock signals that can be used anywhere in the GLB. These four GLB clock signals can consist of a number of combinations of the true and complement edges of the global clock signals.

Figure 6. GLB Clock Generator



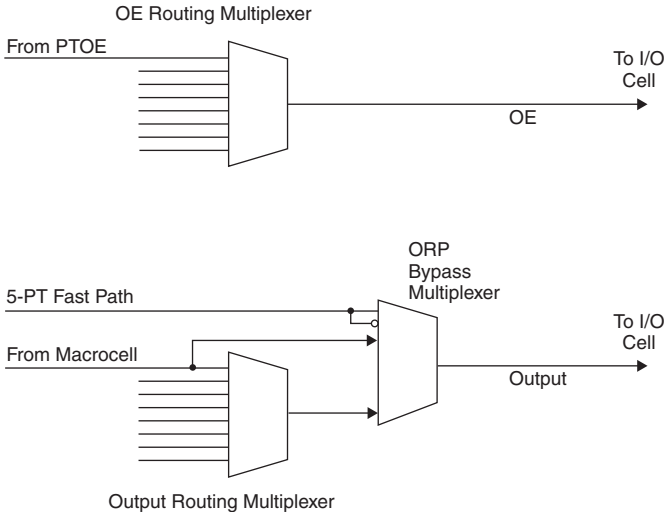
Output Routing Pool (ORP)

The Output Routing Pool allows macrocell outputs to be connected to any of several I/O cells within an I/O block. This provides greater flexibility in determining the pinout and allows design changes to occur without affecting the pinout. The output routing pool also provides a parallel capability for routing macrocell-level OE product terms. This allows the OE product term to follow the macrocell output as it is switched between I/O cells. Additionally, the output routing pool allows the macrocell output or true and complement forms of the 5-PT bypass signal to bypass the output routing multiplexers and feed the I/O cell directly. The enhanced ORP of the LA-ispMACH 4000V/Z family consists of the following elements:

- Output Routing Multiplexers
- OE Routing Multiplexers
- Output Routing Pool Bypass Multiplexers

Figure 7 shows the structure of the ORP from the I/O cell perspective. This is referred to as an ORP slice. Each ORP has as many ORP slices as there are I/O cells in the corresponding I/O block.

Figure 7. ORP Slice



Output Routing Multiplexers

The details of connections between the macrocells and the I/O cells vary across devices and within a device dependent on the maximum number of I/Os available. Tables 6-10 provide the connection details.

Table 6. ORP Combinations for I/O Blocks with 8 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M2, M3, M4, M5, M6, M7, M8, M9
I/O 2	M4, M5, M6, M7, M8, M9, M10, M11
I/O 3	M6, M7, M8, M9, M10, M11, M12, M13
I/O 4	M8, M9, M10, M11, M12, M13, M14, M15
I/O 5	M10, M11, M12, M13, M14, M15, M0, M1
I/O 6	M12, M13, M14, M15, M0, M1, M2, M3
I/O 7	M14, M15, M0, M1, M2, M3, M4, M5

Table 7. ORP Combinations for I/O Blocks with 16 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M1, M2, M3, M4, M5, M6, M7, M8
I/O 2	M2, M3, M4, M5, M6, M7, M8, M9
I/O 3	M3, M4, M5, M6, M7, M8, M9, M10
I/O 4	M4, M5, M6, M7, M8, M9, M10, M11
I/O 5	M5, M6, M7, M8, M9, M10, M11, M12
I/O 6	M6, M7, M8, M9, M10, M11, M12, M13
I/O 7	M7, M8, M9, M10, M11, M12, M13, M14
I/O 8	M8, M9, M10, M11, M12, M13, M14, M15
I/O 9	M9, M10, M11, M12, M13, M14, M15, M0
I/O 10	M10, M11, M12, M13, M14, M15, M0, M1
I/O 11	M11, M12, M13, M14, M15, M0, M1, M2
I/O 12	M12, M13, M14, M15, M0, M1, M2, M3
I/O 13	M13, M14, M15, M0, M1, M2, M3, M4
I/O 14	M14, M15, M0, M1, M2, M3, M4, M5
I/O 15	M15, M0, M1, M2, M3, M4, M5, M6

Table 8. ORP Combinations for I/O Blocks with 12 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M1, M2, M3, M4, M5, M6, M7, M8
I/O 2	M2, M3, M4, M5, M6, M7, M8, M9
I/O 3	M4, M5, M6, M7, M8, M9, M10, M11
I/O 4	M5, M6, M7, M8, M9, M10, M11, M12
I/O 5	M6, M7, M8, M9, M10, M11, M12, M13
I/O 6	M8, M9, M10, M11, M12, M13, M14, M15
I/O 7	M9, M10, M11, M12, M13, M14, M15, M0
I/O 8	M10, M11, M12, M13, M14, M15, M0, M1
I/O 9	M12, M13, M14, M15, M0, M1, M2, M3
I/O 10	M13, M14, M15, M0, M1, M2, M3, M4
I/O 11	M14, M15, M0, M1, M2, M3, M4, M5

ORP Bypass and Fast Output Multiplexers

The ORP bypass and fast-path output multiplexer is a 4:1 multiplexer and allows the 5-PT fast path to bypass the ORP and be connected directly to the pin with either the regular output or the inverted output. This multiplexer also allows the register output to bypass the ORP to achieve faster t_{CO}.

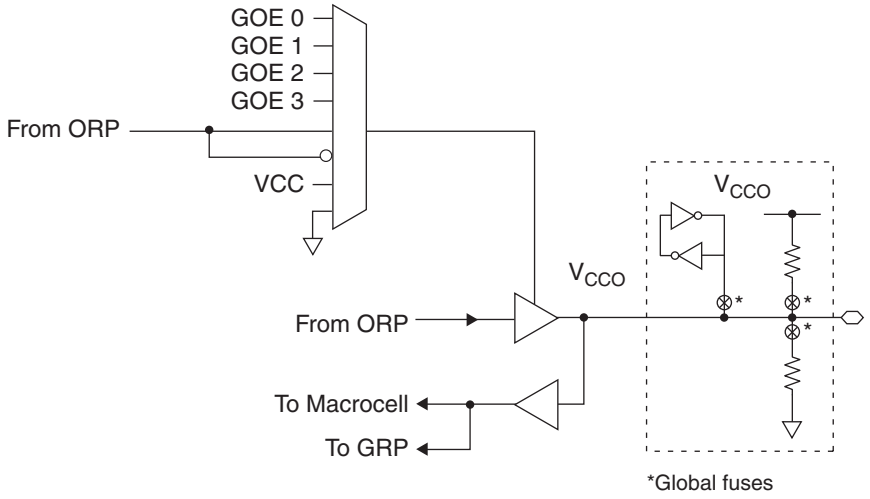
Output Enable Routing Multiplexers

The OE Routing Pool provides the corresponding local output enable (OE) product term to the I/O cell.

I/O Cell

The I/O cell contains the following programmable elements: output buffer, input buffer, OE multiplexer and bus maintenance circuitry. Figure 8 details the I/O cell.

Figure 8. I/O Cell



Each output supports a variety of output standards dependent on the V_{CCO} supplied to its I/O bank. Outputs can also be configured for open drain operation. Each input can be programmed to support a variety of standards, independent of the V_{CCO} supplied to its I/O bank. The I/O standards supported are:

- LVTTL
- LVCMOS 3.3
- LVCMOS 2.5
- LVCMOS 1.8
- 3.3V PCI Compatible

All of the I/Os and dedicated inputs have the capability to provide a bus-keeper latch, Pull-up Resistor or Pull-down Resistor. A fourth option is to provide none of these. The selection is done on a global basis. The default in both hardware and software is such that when the device is erased or if the user does not specify, the input structure is configured to be a Pull-up Resistor.

Each LA-ispMACH 4000V/Z automotive device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for fast slew or slow slew. The typical edge rate difference between fast and slow slew setting is 20%. For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed.

Global OE Generation

Most LA-ispMACH 4000V/Z automotive family devices have a 4-bit wide Global OE Bus, except the LA-ispMACH 4032V and LA-ispMACH4032Z devices that have a 2-bit wide Global OE Bus. This bus is derived from a 4-bit internal global OE PT bus and two dual purpose I/O or GOE pins. Each signal that drives the bus can optionally be inverted.

Each GLB has a block-level OE PT that connects to all bits of the Global OE PT bus with four fuses. Hence, for a 128-macrocell device (with 16 blocks), each line of the bus is driven from 8 OE product terms. Figures 9 and 10 show a graphical representation of the global OE generation.

Supply Current, LA-ispMACH 4000Z

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
LA-ispMACH 4032Z						
ICC[1, 2, 3, 5]	Operating Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	50	—	µA
		Vcc = 1.9V, T_A = 70°C	—	58	—	µA
		Vcc = 1.9V, T_A = 85°C	—	60	—	µA
		Vcc = 1.9V, T_A = 125°C	—	70	—	µA
ICC[4, 5]	Standby Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	10	—	µA
		Vcc = 1.9V, T_A = 70°C	—	13	20	µA
		Vcc = 1.9V, T_A = 85°C	—	15	25	µA
		Vcc = 1.9V, T_A = 125°C	—	22		µA
LA-ispMACH 4064Z						
ICC[1, 2, 3, 5]	Operating Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	80	—	µA
		Vcc = 1.9V, T_A = 70°C	—	89	—	µA
		Vcc = 1.9V, T_A = 85°C	—	92	—	µA
		Vcc = 1.9V, T_A = 125°C	—	109	—	µA
ICC[4, 5]	Standby Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	11	—	µA
		Vcc = 1.9V, T_A = 70°C	—	15	25	µA
		Vcc = 1.9V, T_A = 85°C	—	18	35	µA
		Vcc = 1.9V, T_A = 125°C	—	37		µA
LA-ispMACH 4128Z						
ICC[1, 2, 3, 5]	Operating Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	168	—	µA
		Vcc = 1.9V, T_A = 70°C	—	190	—	µA
		Vcc = 1.9V, T_A = 85°C	—	195	—	µA
		Vcc = 1.9V, T_A = 125°C	—	212	—	µA
ICC[4, 5]	Standby Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	12	—	µA
		Vcc = 1.9V, T_A = 70°C	—	16	35	µA
		Vcc = 1.9V, T_A = 85°C	—	19	50	µA
		Vcc = 1.9V, T_A = 125°C	—	42	—	µA

1. T_A = 25°C, frequency = 1.0 MHz.
2. Device configured with 16-bit counters.
3. I_{CC} varies with specific device configuration and operating frequency.
4. V_{CCO} = 3.6V, V_{IN} = 0V or $V_{CCO,}$ bus maintenance turned off. V_{IN} above V_{CCO} will add transient current above the specified standby I_{CC}.
5. Includes V_{CCO} current without output loading.

LA-ispMACH 4000V/Z External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description[1, 2, 3]	LA-ispMACH 4000V -75		LA-ispMACH 4000Z -75		Units
		Min.	Max.	Min.	Max.	
t_{PD}	5-PT bypass combinatorial propagation delay	—	7.5	—	7.5	ns
t_{PD_MC}	20-PT combinatorial propagation delay through macrocell	—	8.0	—	8.0	ns
t_S	GLB register setup time before clock	4.5	—	4.5	—	ns
t_{ST}	GLB register setup time before clock with T-type register	4.7	—	4.7	—	ns
t_{SIR}	GLB register setup time before clock, input register path	1.7	—	1.4	—	ns
t_{SIRZ}	GLB register setup time before clock with zero hold	2.7	—	2.7	—	ns
t_H	GLB register hold time after clock	0.0	—	0.0	—	ns
t_{HT}	GLB register hold time after clock with T-type register	0.0	—	0.0	—	ns
t_{HIR}	GLB register hold time after clock, input register path	1.0	—	1.3	—	ns
t_{HIRZ}	GLB register hold time after clock, input register path with zero hold	0.0	—	0.0	—	ns
t_{CO}	GLB register clock-to-output delay	—	4.5	—	4.5	ns
t_R	External reset pin to output delay	—	9.0	—	9.0	ns
t_{RW}	External reset pulse duration	4.0	—	4.0	—	ns
$t_{PTOE/DIS}$	Input to output local product term output enable/disable	—	9.0	—	9.0	ns
$t_{GPTOE/DIS}$	Input to output global product term output enable/disable	—	10.3	—	10.5	ns
$t_{GOE/DIS}$	Global OE input to output enable/disable	—	7.0	—	7.0	ns
t_{CW}	Global clock width, high or low	2.8	—	2.8	—	ns
t_{GW}	Global gate width low (for low transparent) or high (for high transparent)	2.8	—	2.8	—	ns
t_{WIR}	Input register clock width, high or low	2.8	—	2.8	—	ns
f_{MAX}[4]	Clock frequency with internal feedback	—	168	—	168	MHz
f_{MAX} (Ext.)	Clock frequency with external feedback, [1/ (t_S + t_{CO})]	—	111	—	111	MHz

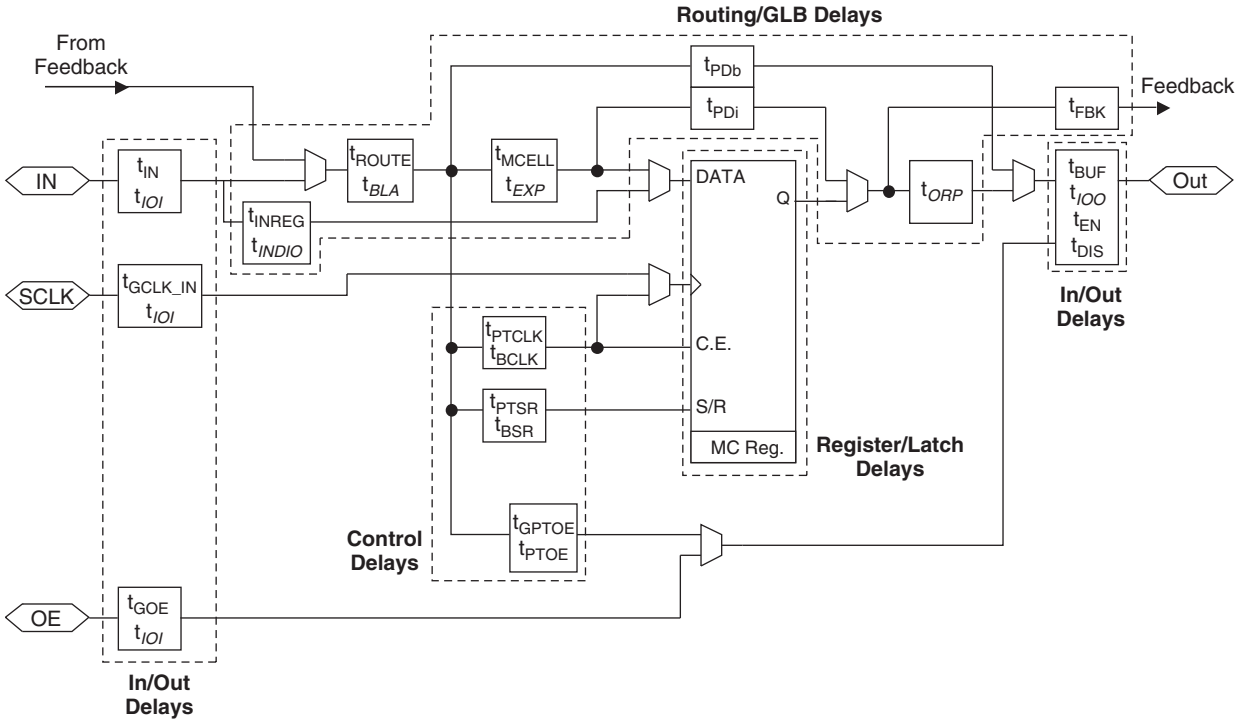
1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.
2. Measured using standard switching circuit, assuming GRP loading of 1 and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using GRP feedback.

Timing v.3.2

Timing Model

The task of determining the timing through the LA-ispMACH 4000V/Z automotive family, like any CPLD, is relatively simple. The timing model provided in Figure 11 shows the specific delay paths. Once the implementation of a given function is determined either conceptually or from the software report file, the delay path of the function can easily be determined from the timing model. The Lattice design tools report the timing delays based on the same timing model for a particular design. Note that the internal timing parameters are given for reference only, and are not tested. The external timing parameters are tested and guaranteed for every device. For more information on the timing model and usage, refer to TN1004, ispMACH 4000 Timing Model Design and Usage Guidelines.

Figure 11. LA-ispMACH 4000V/Z Automotive Timing Model



Note: Italicized items are optional delay adders.

LA-ispMACH 4000V/Z Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	LA-ispMACH 4000V -75		LA-ispMACH 4000Z -75		Units
		Min.	Max.	Min.	Max.	
t_{BSR}	GLB PT Set/Reset Delay	—	1.83	—	1.83	ns
t_{PTSR}	Macrocell PT Set/Reset Delay	—	3.41	—	2.72	ns
t_{GPTOE}	Global PT OE Delay	—	5.58	—	3.50	ns
t_{PTOE}	Macrocell PT OE Delay	—	4.28	—	2.00	ns

Timing v.3.2

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the Timing Model in this data sheet for further details.

LA-ispMACH 4000V/Z Timing Adders[1]

Adder Type	Base Parameter	Description	LA-ispMACH 4000V -75		LA-ispMACH 4000Z -75		Units
			Min.	Max.	Min.	Max.	
Optional Delay Adders							
t_{INDIO}	t_{INREG}	Input register delay	—	1.00	—	1.30	ns
t_{EXP}	t_{MCELL}	Product term expander delay	—	0.33	—	0.50	ns
t_{ORP}	—	Output routing pool delay	—	0.05	—	0.40	ns
t_{BLA}	t_{ROUTE}	Additional block loading adder	—	0.05	—	0.05	ns
t_{IOI} Input Adjusters							
LVTTL_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVTTL standard	—	0.60	—	0.60	ns
LVCMOS33_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 3.3 standard	—	0.60	—	0.60	ns
LVCMOS25_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 2.5 standard	—	0.60	—	0.60	ns
LVCMOS18_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 1.8 standard	—	0.00	—	0.00	ns
PCI_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using PCI compatible input	—	0.60	—	0.60	ns
t_{IOO} Output Adjusters							
LVTTL_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as TTL buffer	—	0.20	—	0.20	ns
LVCMOS33_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V buffer	—	0.20	—	0.20	ns
LVCMOS25_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 2.5V buffer	—	0.10	—	0.10	ns
LVCMOS18_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 1.8V buffer	—	0.00	—	0.00	ns
PCI_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as PCI compatible buffer	—	0.20	—	0.20	ns
Slow Slew	t_{BUF}, t_{EN}	Output configured for slow slew rate	—	1.00	—	1.00	ns

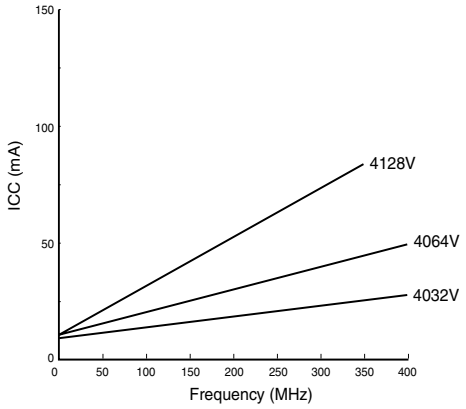
Note: Open drain timing is the same as corresponding LVCMOS timing.

Timing v.3.2

1. Refer to TN1004, ispMACH 4000 Timing Model Design and Usage Guidelines for information regarding use of these adders.

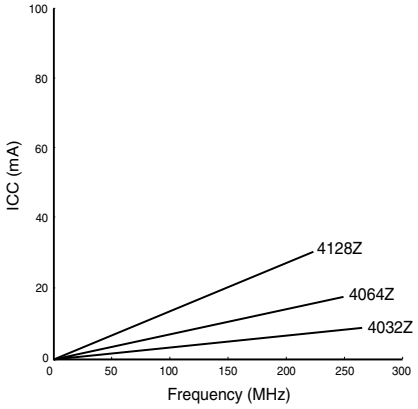
Power Consumption

LA-ispMACH 4000V
Typical I_{CC} vs. Frequency



Note: The devices are configured with the maximum number of 16-bit counters, typical current at 3.3V, 2.5V, 25°C.

LA-ispMACH 4000Z
Typical I_{CC} vs. Frequency
(Preliminary Information)



Note: The devices are configured with the maximum number of 16-bit counters, typical current at 1.8V, 25°C.

Power Estimation Coefficients[1]

Device	A	B
LA-ispMACH 4032V	11.3	0.010
LA-ispMACH 4064V	11.5	0.010
LA-ispMACH 4128V	11.5	0.011
LA-ispMACH 4032Z	0.010	0.010
LA-ispMACH 4064Z	0.011	0.010
LA-ispMACH 4128Z	0.012	0.010

1. For further information about the use of these coefficients, refer to TN1005, Power Estimation in ispMACH 4000V/B/C/Z Devices.

LA-ispMACH 4032V and 4064V Logic Signal Connections: 44-Pin TQFP

Pin Number	Bank Number	LA-ispMACH 4032V		LA-ispMACH 4064V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	TDI	-	TDI	-
2	0	A5	A^5	A10	A^5
3	0	A6	A^6	A12	A^6
4	0	A7	A^7	A14	A^7
5	0	GND (Bank 0)	-	GND (Bank 0)	-
6	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
7	0	A8	A^8	B0	B^0
8	0	A9	A^9	B2	B^1
9	0	A10	A^10	B4	B^2
10	-	TCK	-	TCK	-
11	-	VCC	-	VCC	-
12	-	GND	-	GND	-
13	0	A12	A^12	B8	B^4
14	0	A13	A^13	B10	B^5
15	0	A14	A^14	B12	B^6
16	0	A15	A^15	B14	B^7
17	1	CLK2/I	-	CLK2/I	-
18	1	B0	B^0	C0	C^0
19	1	B1	B^1	C2	C^1
20	1	B2	B^2	C4	C^2
21	1	B3	B^3	C6	C^3
22	1	B4	B^4	C8	C^4
23	-	TMS	-	TMS	-
24	1	B5	B^5	C10	C^5
25	1	B6	B^6	C12	C^6
26	1	B7	B^7	C14	C^7
27	1	GND (Bank 1)	-	GND (Bank 1)	-
28	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
29	1	B8	B^8	D0	D^0
30	1	B9	B^9	D2	D^1
31	1	B10	B^10	D4	D^2
32	-	TDO	-	TDO	-
33	-	VCC	-	VCC	-
34	-	GND	-	GND	-
35	1	B12	B^12	D8	D^4
36	1	B13	B^13	D10	D^5
37	1	B14	B^14	D12	D^6
38	1	B15/GOE1	B^15	D14/GOE1	D^7
39	0	CLK0/I	-	CLK0/I	-
40	0	A0/GOE0	A^0	A0/GOE0	A^0
41	0	A1	A^1	A2	A^1
42	0	A2	A^2	A4	A^2

LA-ispMACH 4032V and 4064V Logic Signal Connections: 44-Pin TQFP

Pin Number	Bank Number	LA-ispMACH 4032V		LA-ispMACH 4064V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
43	0	A3	A^3	A6	A^3
44	0	A4	A^4	A8	A^4

LA-ispMACH 4032V/Z and 4064V/Z Logic Signal Connections: 48-Pin TQFP

Pin Number	Bank Number	LA-ispMACH 4032V/Z		LA-ispMACH 4064V/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	TDI	-	TDI	-
2	0	A5	A^5	A10	A^5
3	0	A6	A^6	A12	A^6
4	0	A7	A^7	A14	A^7
5	0	GND (Bank 0)	-	GND (Bank 0)	-
6	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
7	0	A8	A^8	B0	B^0
8	0	A9	A^9	B2	B^1
9	0	A10	A^10	B4	B^2
10	0	A11	A^11	B6	B^3
11	-	TCK	-	TCK	-
12	-	VCC	-	VCC	-
13	-	GND	-	GND	-
14	0	A12	A^12	B8	B^4
15	0	A13	A^13	B10	B^5
16	0	A14	A^14	B12	B^6
17	0	A15	A^15	B14	B^7
18	0	CLK1/I	-	CLK1/I	-
19	1	CLK2/I	-	CLK2/I	-
20	1	B0	B^0	C0	C^0
21	1	B1	B^1	C2	C^1
22	1	B2	B^2	C4	C^2
23	1	B3	B^3	C6	C^3
24	1	B4	B^4	C8	C^4
25	-	TMS	-	TMS	-
26	1	B5	B^5	C10	C^5
27	1	B6	B^6	C12	C^6
28	1	B7	B^7	C14	C^7
29	1	GND (Bank 1)	-	GND (Bank 1)	-
30	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
31	1	B8	B^8	D0	D^0
32	1	B9	B^9	D2	D^1
33	1	B10	B^10	D4	D^2
34	1	B11	B^11	D6	D^3
35	-	TDO	-	TDO	-

LA-ispMACH 4032V/Z and 4064V/Z Logic Signal Connections: 48-Pin TQFP

Pin Number	Bank Number	LA-ispMACH 4032V/Z		LA-ispMACH 4064V/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
36	-	VCC	-	VCC	-
37	-	GND	-	GND	-
38	1	B12	B^12	D8	D^4
39	1	B13	B^13	D10	D^5
40	1	B14	B^14	D12	D^6
41	1	B15/GOE1	B^15	D14/GOE1	D^7
42	1	CLK3/I	-	CLK3/I	-
43	0	CLK0/I	-	CLK0/I	-
44	0	A0/GOE0	A^0	A0/GOE0	A^0
45	0	A1	A^1	A2	A^1
46	0	A2	A^2	A4	A^2
47	0	A3	A^3	A6	A^3
48	0	A4	A^4	A8	A^4

LA-ispMACH 4064V/Z and 4128V/Z Logic Signal Connections: 100-Pin TQFP

Pin Number	Bank Number	LA-ispMACH 4064V/Z		LA-ispMACH 4128V/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	GND	-	GND	-
2	-	TDI	-	TDI	-
3	0	A8	A^8	B0	B^0
4	0	A9	A^9	B2	B^1
5	0	A10	A^10	B4	B^2
6	0	A11	A^11	B6	B^3
7	0	GND (Bank 0)	-	GND (Bank 0)	-
8	0	A12	A^12	B8	B^4
9	0	A13	A^13	B10	B^5
10	0	A14	A^14	B12	B^6
11	0	A15	A^15	B13	B^7
12*	0	I	-	I	-
13	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
14	0	B15	B^15	C14	C^7
15	0	B14	B^14	C12	C^6
16	0	B13	B^13	C10	C^5
17	0	B12	B^12	C8	C^4
18	0	GND (Bank 0)	-	GND (Bank 0)	-
19	0	B11	B^11	C6	C^3
20	0	B10	B^10	C5	C^2
21	0	B9	B^9	C4	C^1
22	0	B8	B^8	C2	C^0
23*	0	I	-	I	-
24	-	TCK	-	TCK	-

LA-ispMACH 4064V/Z and 4128V/Z Logic Signal Connections: 100-Pin TQFP

Pin Number	Bank Number	LA-ispMACH 4064V/Z		LA-ispMACH 4128V/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
25	-	VCC	-	VCC	-
26	-	GND	-	GND	-
27*	0	I	-	I	-
28	0	B7	B^7	D13	D^7
29	0	B6	B^6	D12	D^6
30	0	B5	B^5	D10	D^5
31	0	B4	B^4	D8	D^4
32	0	GND (Bank 0)	-	GND (Bank 0)	-
33	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
34	0	B3	B^3	D6	D^3
35	0	B2	B^2	D4	D^2
36	0	B1	B^1	D2	D^1
37	0	B0	B^0	D0	D^0
38	0	CLK1/I	-	CLK1/I	-
39	1	CLK2/I	-	CLK2/I	-
40	-	VCC	-	VCC	-
41	1	C0	C^0	E0	E^0
42	1	C1	C^1	E2	E^1
43	1	C2	C^2	E4	E^2
44	1	C3	C^3	E6	E^3
45	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
46	1	GND (Bank 1)	-	GND (Bank 1)	-
47	1	C4	C^4	E8	E^4
48	1	C5	C^5	E10	E^5
49	1	C6	C^6	E12	E^6
50	1	C7	C^7	E14	E^7
51	-	GND	-	GND	-
52	-	TMS	-	TMS	-
53	1	C8	C^8	F0	F^0
54	1	C9	C^9	F2	F^1
55	1	C10	C^10	F4	F^2
56	1	C11	C^11	F6	F^3
57	1	GND (Bank 1)	-	GND (Bank 1)	-
58	1	C12	C^12	F8	F^4
59	1	C13	C^13	F10	F^5
60	1	C14	C^14	F12	F^6
61	1	C15	C^15	F13	F^7
62*	1	I	-	I	-
63	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
64	1	D15	D^15	G14	G^7
65	1	D14	D^14	G12	G^6
66	1	D13	D^13	G10	G^5
67	1	D12	D^12	G8	G^4

LA-ispMACH 4064V/Z and 4128V/Z Logic Signal Connections: 100-Pin TQFP

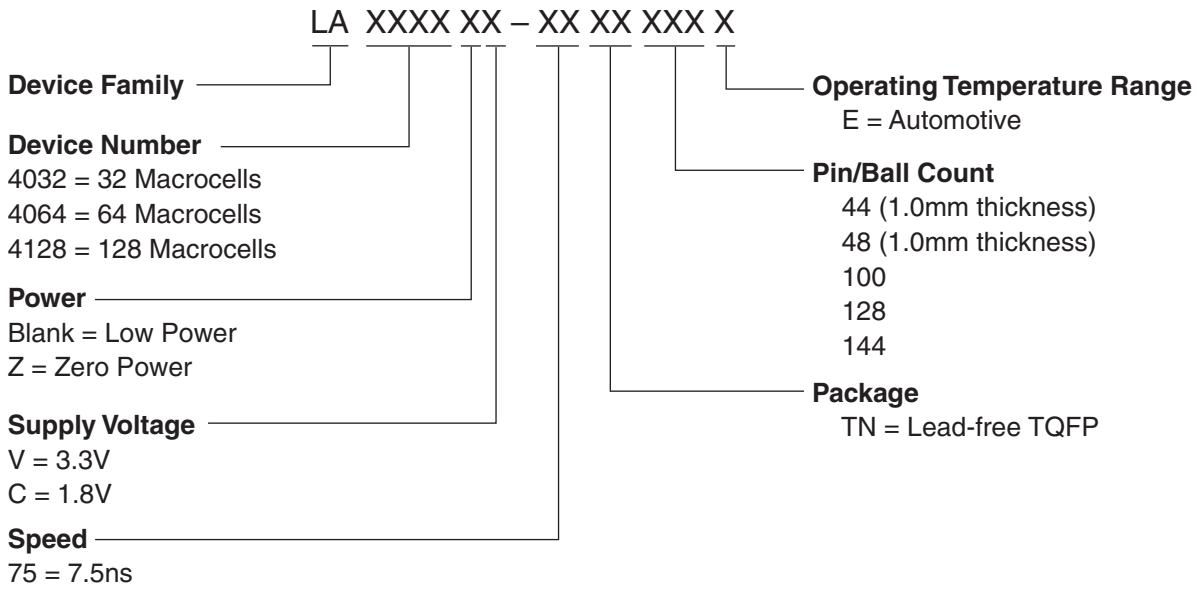
Pin Number	Bank Number	LA-ispMACH 4064V/Z		LA-ispMACH 4128V/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
68	1	GND (Bank 1)	-	GND (Bank 1)	-
69	1	D11	D^11	G6	G^3
70	1	D10	D^10	G5	G^2
71	1	D9	D^9	G4	G^1
72	1	D8	D^8	G2	G^0
73*	1	I	-	I	-
74	-	TDO	-	TDO	-
75	-	VCC	-	VCC	-
76	-	GND	-	GND	-
77*	1	I	-	I	-
78	1	D7	D^7	H13	H^7
79	1	D6	D^6	H12	H^6
80	1	D5	D^5	H10	H^5
81	1	D4	D^4	H8	H^4
82	1	GND (Bank 1)	-	GND (Bank 1)	-
83	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
84	1	D3	D^3	H6	H^3
85	1	D2	D^2	H4	H^2
86	1	D1	D^1	H2	H^1
87	1	D0/GOE1	D^0	H0/GOE1	H^0
88	1	CLK3/I	-	CLK3/I	-
89	0	CLK0/I	-	CLK0/I	-
90	-	VCC	-	VCC	-
91	0	A0/GOE0	A^0	A0/GOE0	A^0
92	0	A1	A^1	A2	A^1
93	0	A2	A^2	A4	A^2
94	0	A3	A^3	A6	A^3
95	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
96	0	GND (Bank 0)	-	GND (Bank 0)	-
97	0	A4	A^4	A8	A^4
98	0	A5	A^5	A10	A^5
99	0	A6	A^6	A12	A^6
100	0	A7	A^7	A14	A^7

*This pin is input only.

LA-ispMACH 4128V Logic Signal Connections: 128-Pin TQFP (Cont.)

Pin Number	Bank Number	LA-ispMACH 4128V	
		GLB/MC/Pad	ORP
86	1	G9	G^7
87	1	G8	G^6
88	1	GND (Bank 1)	-
89	1	G6	G^5
90	1	G5	G^4
91	1	G4	G^3
92	1	G2	G^2
93	1	G0	G^0
94	1	VCCO (Bank 1)	-
95	1	TDO	-
96	1	VCC	-
97	1	GND	-
98	1	H14	H^11
99	1	H13	H^10
100	1	H12	H^9
101	1	H10	H^8
102	1	H9	H^7
103	1	H8	H^6
104	1	GND (Bank 1)	-
105	1	VCCO (Bank 1)	-
106	1	H6	H^5
107	1	H5	H^4
108	1	H4	H^3
109	1	H2	H^2
110	1	H1	H^1
111	1	H0/GOE1	H^0
112	1	CLK3/I	-
113	0	GND (Bank 0)	-
114	0	CLK0/I	-
115	0	VCC	-
116	0	A0/GOE0	A^0
117	0	A1	A^1
118	0	A2	A^2
119	0	A4	A^3
120	0	A5	A^4
121	0	A6	A^5
122	0	VCCO (Bank 0)	-
123	0	GND (Bank 0)	-
124	0	A8	A^6
125	0	A9	A^7
126	0	A10	A^8
127	0	A12	A^9
128	0	A14	A^11

Part Number Description



Ordering Information

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LA4032V	LA4032V-75TN48E	32	3.3	7.5	Lead-free TQFP	48	32	E
	LA4032V-75TN44E	32	3.3	7.5	Lead-free TQFP	44	30	E
LA4064V	LA4064V-75TN100E	64	3.3	7.5	Lead-free TQFP	100	64	E
	LA4064V-75TN48E	64	3.3	7.5	Lead-free TQFP	48	32	E
	LA4064V-75TN44E	64	3.3	7.5	Lead-free TQFP	44	30	E
LA4128V	LA4128V-75TN144E	128	3.3	7.5	Lead-free TQFP	144	96	E
	LA4128V-75TN128E	128	3.3	7.5	Lead-free TQFP	128	92	E
	LA4128V-75TN100E	128	3.3	7.5	Lead-free TQFP	100	64	E
LA4032Z	LA4032ZC-75TN48E	32	1.8	7.5	Lead-free TQFP	48	32	E
LA4064Z	LA4064ZC-75TN100E	64	1.8	7.5	Lead-free TQFP	100	64	E
	LA4064ZC-75TN48E	64	1.8	7.5	Lead-free TQFP	48	32	E
LA4128Z	LA4128ZC-75TN100E	128	1.8	7.5	Lead-free TQFP	100	64	E

Automotive Disclaimer

Products are not designed, intended or warranted to be fail-safe and are not designed, intended or warranted for use in applications related to the deployment of airbags. Further, products are not intended to be used, designed or warranted for use in applications that affect the control of the vehicle unless there is a fail-safe or redundancy feature and also a warning signal to the operator of the vehicle upon failure. Use of products in such applications is fully at the risk of the customer, subject to applicable laws and regulations governing limitations on product liability.

For Further Information

In addition to this data sheet, the following technical notes may be helpful when designing with the LA-ispMACH 4000V/Z automotive family:

- TN1004, ispMACH 4000 Timing Model Design and Usage Guidelines
- TN1005, Power Estimation in ispMACH 4000V/B/C/Z Devices

Revision History

Date	Version	Change Summary
April 2006	01.0	Initial release.
October 2006	02.0	Added LA-ispMACH 4000Z support information throughout.
March 2007	02.1	Updated ispMACH 4000 Introduction section.
		Updated Signal Descriptions table.
September 2007	02.2	DC Electrical Characteristics table, removed duplicate specifications.
July 2008	02.3	Lowered the maximum supply current at 85°C to match the commercial product values.
		Added automotive disclaimer.
May 2009	02.4	Correction to t_{CW}, tGW, t_{WIR} and f_{MAX} parameters in External Switching Characteristics table.
May 2009	02.5	Correction to t_{CW}, tGW and t_{WIR} parameters in External Switching Characteristics table.