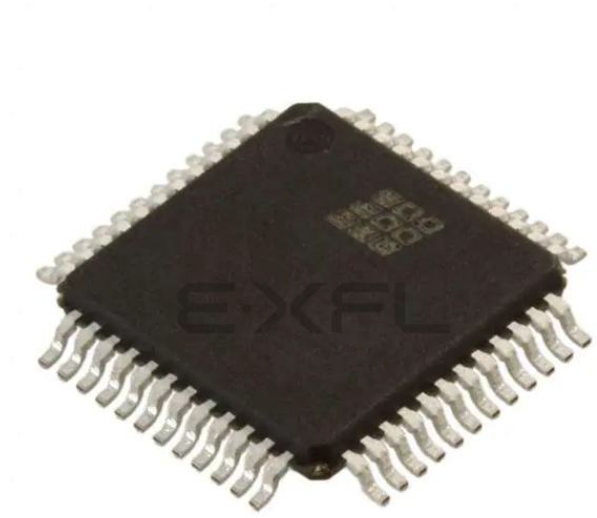
# Lattice Semiconductor Corporation - LA4064ZC-75TN48E Datasheet



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## Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

| Details | |
|---|---|
| Product Status | Active |
| Programmable Type | In System Programmable |
| Delay Time tpd(1) Max | 7.5 ns |
| Voltage Supply - Internal | 1.7V ~ 1.9V |
| Number of Logic Elements/Blocks | - |
| Number of Macrocells | 64 |
| Number of Gates | - |
| Number of I/O | 32 |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-TQFP |
| Supplier Device Package | 48-TQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/la4064zc-75tn48e |

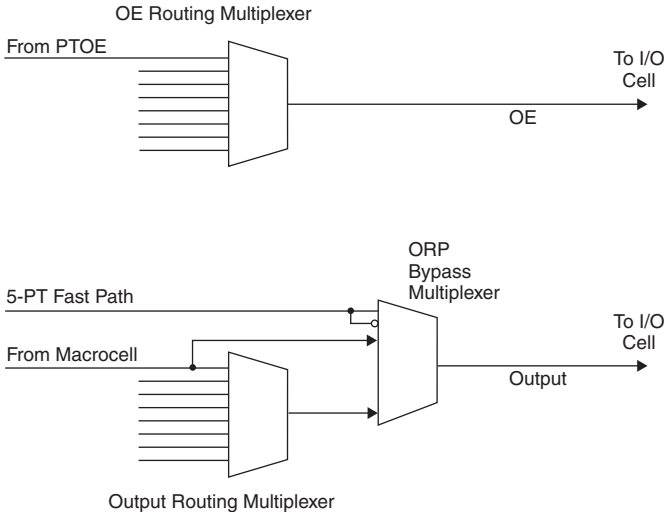
## Output Routing Pool (ORP)

The Output Routing Pool allows macrocell outputs to be connected to any of several I/O cells within an I/O block. This provides greater flexibility in determining the pinout and allows design changes to occur without affecting the pinout. The output routing pool also provides a parallel capability for routing macrocell-level OE product terms. This allows the OE product term to follow the macrocell output as it is switched between I/O cells. Additionally, the output routing pool allows the macrocell output or true and complement forms of the 5-PT bypass signal to bypass the output routing multiplexers and feed the I/O cell directly. The enhanced ORP of the LA-ispMACH 4000V/Z family consists of the following elements:

- Output Routing Multiplexers
- OE Routing Multiplexers
- Output Routing Pool Bypass Multiplexers

Figure 7 shows the structure of the ORP from the I/O cell perspective. This is referred to as an ORP slice. Each ORP has as many ORP slices as there are I/O cells in the corresponding I/O block.

***Figure 7. ORP Slice***



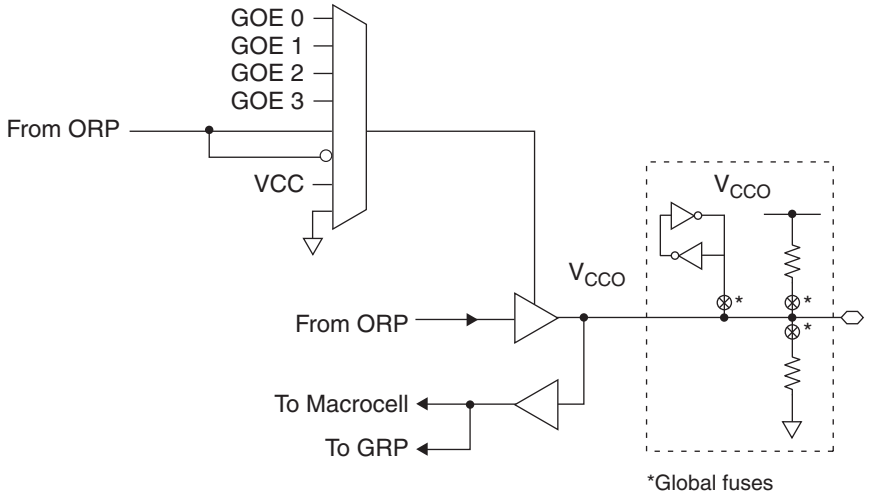

## Output Routing Multiplexers

The details of connections between the macrocells and the I/O cells vary across devices and within a device dependent on the maximum number of I/Os available. Tables 6-10 provide the connection details.

***Table 6. ORP Combinations for I/O Blocks with 8 I/Os***

| I/O Cell | Available Macrocells |
|---|---|
| I/O 0 | M0, M1, M2, M3, M4, M5, M6, M7 |
| I/O 1 | M2, M3, M4, M5, M6, M7, M8, M9 |
| I/O 2 | M4, M5, M6, M7, M8, M9, M10, M11 |
| I/O 3 | M6, M7, M8, M9, M10, M11, M12, M13 |
| I/O 4 | M8, M9, M10, M11, M12, M13, M14, M15 |
| I/O 5 | M10, M11, M12, M13, M14, M15, M0, M1 |
| I/O 6 | M12, M13, M14, M15, M0, M1, M2, M3 |
| I/O 7 | M14, M15, M0, M1, M2, M3, M4, M5 |

***Figure 8. I/O Cell***




Each output supports a variety of output standards dependent on the $V_{CCO}$ supplied to its I/O bank. Outputs can also be configured for open drain operation. Each input can be programmed to support a variety of standards, independent of the $V_{CCO}$ supplied to its I/O bank. The I/O standards supported are:

- LVTTL
- LVCMOS 3.3
- LVCMOS 2.5
- LVCMOS 1.8
- 3.3V PCI Compatible

All of the I/Os and dedicated inputs have the capability to provide a bus-keeper latch, Pull-up Resistor or Pull-down Resistor. A fourth option is to provide none of these. The selection is done on a global basis. The default in both hardware and software is such that when the device is erased or if the user does not specify, the input structure is configured to be a Pull-up Resistor.

Each LA-ispMACH 4000V/Z automotive device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for fast slew or slow slew. The typical edge rate difference between fast and slow slew setting is 20%. For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed.

## Global OE Generation

Most LA-ispMACH 4000V/Z automotive family devices have a 4-bit wide Global OE Bus, except the LA-ispMACH 4032V and LA-ispMACH4032Z devices that have a 2-bit wide Global OE Bus. This bus is derived from a 4-bit internal global OE PT bus and two dual purpose I/O or GOE pins. Each signal that drives the bus can optionally be inverted.

Each GLB has a block-level OE PT that connects to all bits of the Global OE PT bus with four fuses. Hence, for a 128-macrocell device (with 16 blocks), each line of the bus is driven from 8 OE product terms. Figures 9 and 10 show a graphical representation of the global OE generation.

***Figure 9. Global OE Generation for All Devices Except LA-ispMACH 4032V/Z***

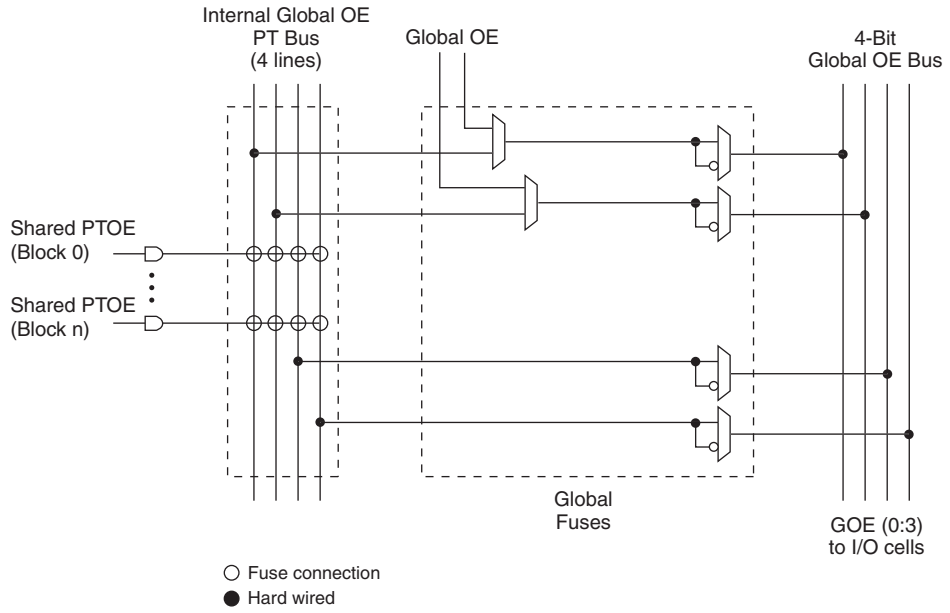
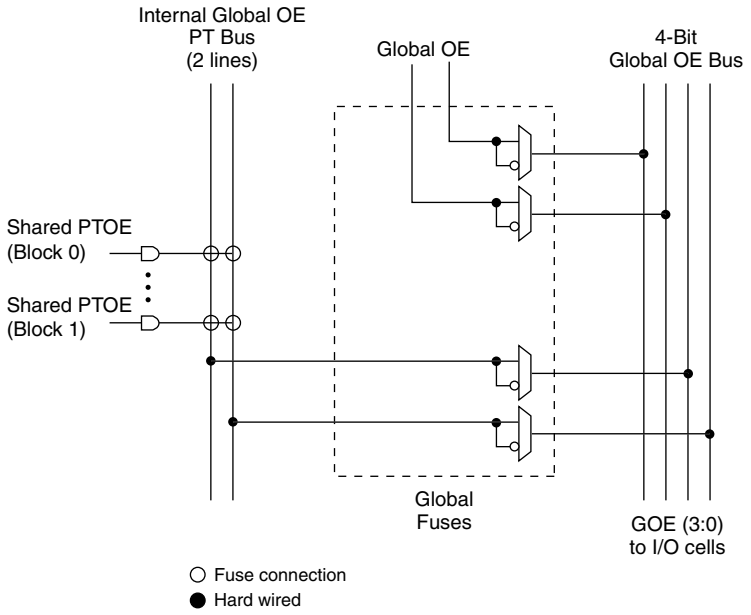



***Figure 10. Global OE Generation for LA-ispMACH 4032V/Z***




## Zero Power/Low Power and Power Management

The LA-ispMACH 4000V/Z automotive family is designed with high speed low power design techniques to offer both high speed and low power. With an advanced $E^2$ low power cell and non sense-amplifier design approach (full CMOS logic approach), the LA-ispMACH 4000V/Z automotive family offers SuperFAST pin-to-pin speeds, while simultaneously delivering low standby power without needing any “turbo bits” or other power management schemes associated with a traditional sense-amplifier approach.

The zero power LA-ispMACH 4000Z is based on the 1.8V ispMACH 4000C family. With innovative circuit design changes, the LA-ispMACH 4000Z family is able to achieve the industry's "lowest static power".

## IEEE 1149.1-Compliant Boundary Scan Testability

All LA-ispMACH 4000V/Z automotive devices have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic notes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more board-level testing. The test access port operates with an LVCMOS interface that corresponds to the power supply voltage.

## I/O Quick Configuration

To facilitate the most efficient board test, the physical nature of the I/O cells must be set before running any continuity tests. As these tests are fast, by nature, the overhead and time that is required for configuration of the I/Os' physical nature should be minimal so that board test time is minimized. The LA-ispMACH 4000V/Z automotive family of devices allows this by offering the user the ability to quickly configure the physical nature of the I/O cells. This quick configuration takes milliseconds to complete, whereas it takes seconds for the entire device to be programmed. Lattice's ispVM™ System programming software can either perform the quick configuration through the PC parallel port, or can generate the ATE or test vectors necessary for a third-party test system.

## IEEE 1532-Compliant In-System Programming

Programming devices in-system provides a number of significant benefits including: rapid prototyping, lower inventory levels, higher quality and the ability to make in-field modifications. The LA-ispMACH 4000V/Z automotive devices provide In-System Programming (ISP™) capability through the Boundary Scan Test Access Port. This capability has been implemented in a manner that ensures that the port remains complaint to the IEEE 1149.1 standard. By using IEEE 1149.1 as the communication interface through which ISP is achieved, users get the benefit of a standard, well-defined interface. All LA-ispMACH 4000V/Z automotive devices are also compliant with the IEEE 1532 standard.

The LA-ispMACH 4000V/Z automotive devices can be programmed across the commercial temperature and voltage range. The PC-based Lattice software facilitates in-system programming of LA-ispMACH 4000V/Z automotive devices. The software takes the JEDEC file output produced by the design implementation software, along with information about the scan chain, and creates a set of vectors used to drive the scan chain. The software can use these vectors to drive a scan chain via the parallel port of a PC. Alternatively, the software can output files in formats understood by common automated test equipment. This equipment can then be used to program LA-ispMACH 4000V/Z automotive devices during the testing of a circuit board.

## User Electronic Signature

The User Electronic Signature (UES) allows the designer to include identification bits or serial numbers inside the device, stored in $E^2$CMOS memory. The LA-ispMACH 4000V/Z automotive device contains 32 UES bits that can be configured by the user to store unique data such as ID codes, revision numbers or inventory control codes.

## Security Bit

A programmable security bit is provided on the LA-ispMACH 4000V/Z automotive devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

## Hot Socketing

The LA-ispMACH 4000V/Z automotive devices are well-suited for applications that require hot socketing capability. Hot socketing a device requires that the device, during power-up and down, can tolerate active signals on the I/Os

# I/O Recommended Operating Conditions

| Standard | $V_{CCO}$ (V)[1] | |
|---|---|---|
| | Min. | Max. |
| LVTTL | 3.0 | 3.6 |
| LVCMOS 3.3 | 3.0 | 3.6 |
| Extended LVCMOS 3.3[2] | 2.7 | 3.6 |
| LVCMOS 2.5 | 2.3 | 2.7 |
| LVCMOS 1.8 | 1.65 | 1.95 |
| PCI 3.3 | 3.0 | 3.6 |

1. Typical values for $V_{CCO}$ are the average of the min. and max. values.
2. LA-ispMACH 4000Z only.

# DC Electrical Characteristics

**Over Recommended Operating Conditions**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{IL}$, $I_{IH}$[1, 4] | Input Leakage Current (LA-ispMACH 4000Z) | $0 \le V_{IN} < V_{CCO}$ | — | 0.5 | 1 | µA |
| $I_{IH}$[1, 2] | Input High Leakage Current (LA-ispMACH 4000V) | $3.6V < V_{IN} \le 5.5V$, $T_j = 105°C$<br>$3.0V \le V_{CCO} \le 3.6V$ | — | — | 20 | µA |
| | | $3.6V < V_{IN} \le 5.5V$, $T_j = 130°C$<br>$3.0V \le V_{CCO} \le 3.6V$ | — | — | 50 | µA |
| | Input High Leakage Current (LA-ispMACH 4000Z) | $V_{CCO} < V_{IN} \le 5.5V$ | — | — | 10 | µA |
| $I_{PU}$ | I/O Weak Pull-up Resistor Current (LA-ispMACH 4000V) | $0 \le V_{IN} \le 0.7V_{CCO}$ | -30 | — | -200 | µA |
| | I/O Weak Pull-up Resistor Current (LA-ispMACH 4000Z) | $0 \le V_{IN} \le 0.7V_{CCO}$ | -30 | — | -150 | µA |
| $I_{PD}$ | I/O Weak Pull-down Resistor Current | $V_{IL}$ (MAX) $\le V_{IN} \le V_{IH}$ (MIN) | 30 | — | 150 | µA |
| $I_{BHLS}$ | Bus Hold Low Sustaining Current | $V_{IN} = V_{IL}$ (MAX) | 30 | — | — | µA |
| $I_{BHHS}$ | Bus Hold High Sustaining Current | $V_{IN} = 0.7\ V_{CCO}$ | -30 | — | — | µA |
| $I_{BHLO}$ | Bus Hold Low Overdrive Current | $0V \le V_{IN} \le V_{BHT}$ | — | — | 150 | µA |
| $I_{BHHO}$ | Bus Hold High Overdrive Current | $V_{BHT} \le V_{IN} \le V_{CCO}$ | — | — | -150 | µA |
| $V_{BHT}$ | Bus Hold Trip Points | — | $V_{CCO}$ * 0.35 | — | $V_{CCO}$ * 0.65 | V |
| $C_1$ | I/O Capacitance[3] | $V_{CCO}$ = 3.3V, 2.5V, 1.8V | — | 8 | — | pf |
| | | $V_{CC}$ = 1.8V, $V_{IO}$ = 0 to $V_{IH}$ (MAX) | — | | — | |
| $C_2$ | Clock Capacitance[3] | $V_{CCO}$ = 3.3V, 2.5V, 1.8V | — | 6 | — | pf |
| | | $V_{CC}$ = 1.8V, $V_{IO}$ = 0 to $V_{IH}$ (MAX) | — | | — | |
| $C_3$ | Global Input Capacitance[3] | $V_{CCO}$ = 3.3V, 2.5V, 1.8V | — | 6 | — | pf |
| | | $V_{CC}$ = 1.8V, $V_{IO}$ = 0 to $V_{IH}$ (MAX) | — | | — | |

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. 5V tolerant inputs and I/O should only be placed in banks where $3.0V \le V_{CCO} \le 3.6V$.
3. $T_A = 25°C$, f = 1.0MHz.
4. $I_{IH}$ excursions of up to 1.5µA maximum per pin above the spec limit may be observed for certain voltage conditions on no more than 10% of the device's I/O pins.

## Supply Current, LA-ispMACH 4000V

**Over Recommended Operating Conditions**

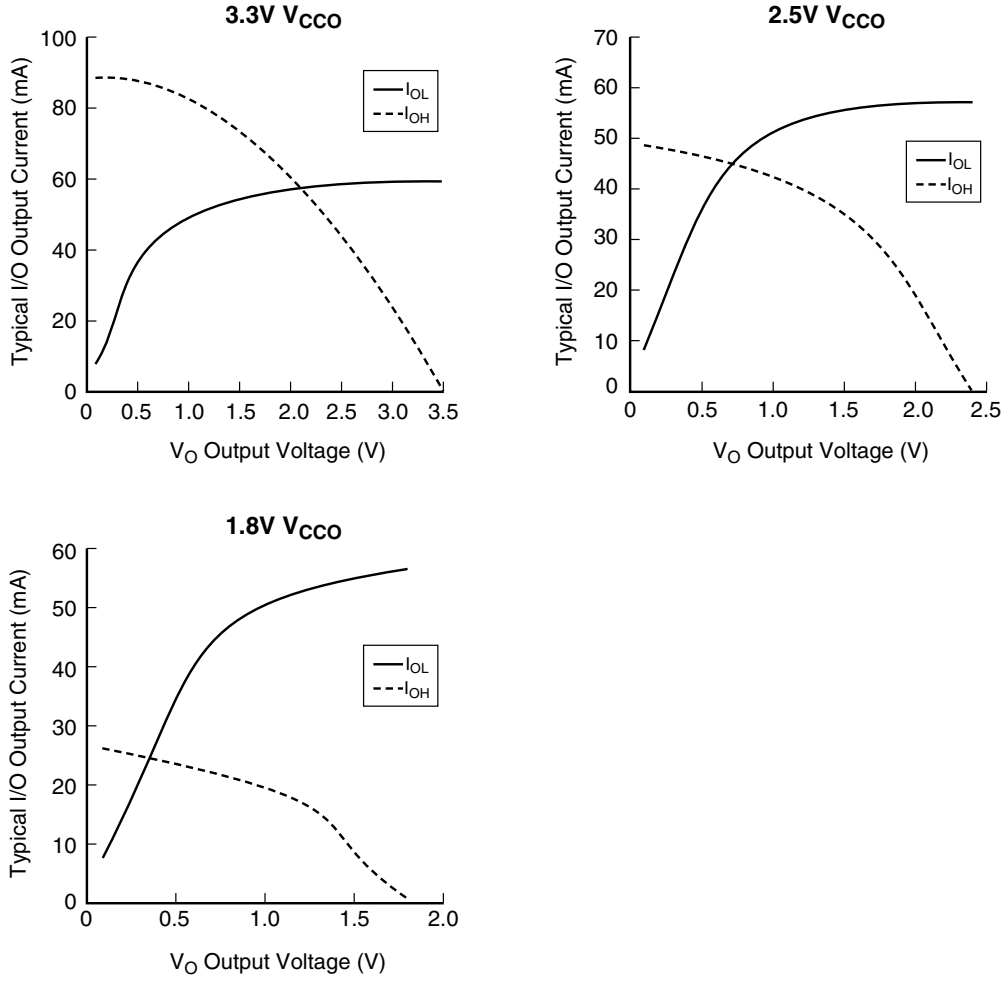
| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **LA-ispMACH 4032V** | | | | | | |
| ICC | Operating Power Supply Current | Vcc = 3.3V | — | 11.8 | — | mA |
| | Standby Power Supply Current | Vcc = 3.3V | — | 11.3 | — | mA |
| **LA-ispMACH 4064V** | | | | | | |
| ICC | Operating Power Supply Current | Vcc = 3.3V | — | 12 | — | mA |
| | Standby Power Supply Current | Vcc = 3.3V | — | 11.5 | — | mA |
| **LA-ispMACH 4128V** | | | | | | |
| ICC | Operating Power Supply Current | Vcc = 3.3V | — | 12 | — | mA |
| | Standby Power Supply Current | Vcc = 3.3V | — | 11.5 | — | mA |

# I/O DC Electrical Characteristics

**Over Recommended Operating Conditions**

| Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ Max (V) | $V_{OH}$ Min (V) | $I_{OL}$[1] (mA) | $I_{OH}$[1] (mA) |
|---|---|---|---|---|---|---|---|---|
| | Min (V) | Max (V) | Min (V) | Max (V) | | | | |
| LVTTL | -0.3 | 0.80 | 2.0 | 5.5 | 0.40 | $V_{CCO}$ - 0.40 | 8.0 | -4.0 |
| | | | | | 0.20 | $V_{CCO}$ - 0.20 | 0.1 | -0.1 |
| LVCMOS 3.3 | -0.3 | 0.80 | 2.0 | 5.5 | 0.40 | $V_{CCO}$ - 0.40 | 8.0 | -4.0 |
| | | | | | 0.20 | $V_{CCO}$ - 0.20 | 0.1 | -0.1 |
| LVCMOS 2.5 | -0.3 | 0.70 | 1.70 | 3.6 | 0.40 | $V_{CCO}$ - 0.40 | 8.0 | -4.0 |
| | | | | | 0.20 | $V_{CCO}$ - 0.20 | 0.1 | -0.1 |
| LVCMOS 1.8 (4000V) | -0.3 | 0.63 | 1.17 | 3.6 | 0.40 | $V_{CCO}$ - 0.45 | 2.0 | -2.0 |
| | | | | | 0.20 | $V_{CCO}$ - 0.20 | 0.1 | -0.1 |
| LVCMOS 1.8 (4000Z) | -0.3 | 0.35 * $V_{CC}$ | 0.65 * $V_{CC}$ | 3.6 | 0.40 | $V_{CCO}$ - 0.45 | 2.0 | -2.0 |
| | | | | | 0.20 | $V_{CCO}$ - 0.20 | 0.1 | -0.1 |
| PCI 3.3 (4000V) | -0.3 | 1.08 | 1.5 | 5.5 | 0.1 $V_{CCO}$ | 0.9 $V_{CCO}$ | 1.5 | -0.5 |
| PCI 3.3 (4000Z) | -0.3 | 0.3 * 3.3 * ($V_{CC}$ / 1.8) | 0.5 * 3.3 * ($V_{CC}$ / 1.8) | 5.5 | 0.1 $V_{CCO}$ | 0.9 $V_{CCO}$ | 1.5 | -0.5 |

1. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank, as shown in the logic signals connection table, shall not exceed *n**8mA. Where *n* is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.



# LA-ispMACH 4000V/Z External Switching Characteristics

**Over Recommended Operating Conditions**

| Parameter | Description[1, 2, 3] | LA-ispMACH 4000V -75 | | LA-ispMACH 4000Z -75 | | Units |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $t_{PD}$ | 5-PT bypass combinatorial propagation delay | — | 7.5 | — | 7.5 | ns |
| $t_{PD\_MC}$ | 20-PT combinatorial propagation delay through macrocell | — | 8.0 | — | 8.0 | ns |
| $t_S$ | GLB register setup time before clock | 4.5 | — | 4.5 | — | ns |
| $t_{ST}$ | GLB register setup time before clock with T-type register | 4.7 | — | 4.7 | — | ns |
| $t_{SIR}$ | GLB register setup time before clock, input register path | 1.7 | — | 1.4 | — | ns |
| $t_{SIRZ}$ | GLB register setup time before clock with zero hold | 2.7 | — | 2.7 | — | ns |
| $t_H$ | GLB register hold time after clock | 0.0 | — | 0.0 | — | ns |
| $t_{HT}$ | GLB register hold time after clock with T-type register | 0.0 | — | 0.0 | — | ns |
| $t_{HIR}$ | GLB register hold time after clock, input register path | 1.0 | — | 1.3 | — | ns |
| $t_{HIRZ}$ | GLB register hold time after clock, input register path with zero hold | 0.0 | — | 0.0 | — | ns |
| $t_{CO}$ | GLB register clock-to-output delay | — | 4.5 | — | 4.5 | ns |
| $t_R$ | External reset pin to output delay | — | 9.0 | — | 9.0 | ns |
| $t_{RW}$ | External reset pulse duration | 4.0 | — | 4.0 | — | ns |
| $t_{PTOE/DIS}$ | Input to output local product term output enable/disable | — | 9.0 | — | 9.0 | ns |
| $t_{GPTOE/DIS}$ | Input to output global product term output enable/disable | — | 10.3 | — | 10.5 | ns |
| $t_{GOE/DIS}$ | Global OE input to output enable/disable | — | 7.0 | — | 7.0 | ns |
| $t_{CW}$ | Global clock width, high or low | 2.8 | — | 2.8 | — | ns |
| $t_{GW}$ | Global gate width low (for low transparent) or high (for high transparent) | 2.8 | — | 2.8 | — | ns |
| $t_{WIR}$ | Input register clock width, high or low | 2.8 | — | 2.8 | — | ns |
| $f_{MAX}$[4] | Clock frequency with internal feedback | — | 168 | — | 168 | MHz |
| $f_{MAX}$ (Ext.) | Clock frequency with external feedback, [1/ ($t_S$ + $t_{CO}$)] | — | 111 | — | 111 | MHz |

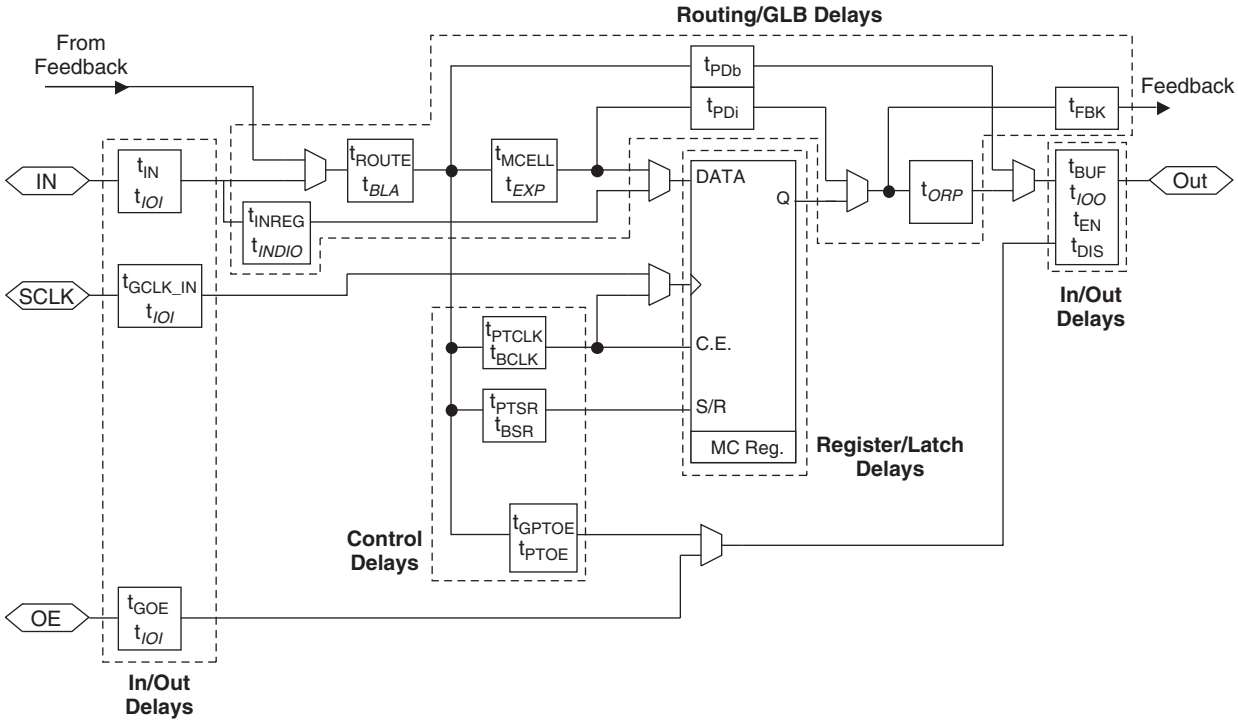
1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.
2. Measured using standard switching circuit, assuming GRP loading of 1 and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using GRP feedback.

Timing v.3.2

## Timing Model

The task of determining the timing through the LA-ispMACH 4000V/Z automotive family, like any CPLD, is relatively simple. The timing model provided in Figure 11 shows the specific delay paths. Once the implementation of a given function is determined either conceptually or from the software report file, the delay path of the function can easily be determined from the timing model. The Lattice design tools report the timing delays based on the same timing model for a particular design. Note that the internal timing parameters are given for reference only, and are not tested. The external timing parameters are tested and guaranteed for every device. For more information on the timing model and usage, refer to TN1004, ispMACH 4000 Timing Model Design and Usage Guidelines.

***Figure 11. LA-ispMACH 4000V/Z Automotive Timing Model***




Note: Italicized items are optional delay adders.

# LA-ispMACH 4000V/Z Timing Adders[1]

| Adder Type | Base Parameter | Description | LA-ispMACH 4000V -75 | | LA-ispMACH 4000Z -75 | | Units |
|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | |
| **Optional Delay Adders** | | | | | | | |
| $t_{INDIO}$ | $t_{INREG}$ | Input register delay | — | 1.00 | — | 1.30 | ns |
| $t_{EXP}$ | $t_{MCELL}$ | Product term expander delay | — | 0.33 | — | 0.50 | ns |
| $t_{ORP}$ | — | Output routing pool delay | — | 0.05 | — | 0.40 | ns |
| $t_{BLA}$ | $t_{ROUTE}$ | Additional block loading adder | — | 0.05 | — | 0.05 | ns |
| **$t_{IOI}$ Input Adjusters** | | | | | | | |
| LVTTL_in | $t_{IN}$, $t_{GCLK\_IN}$, $t_{GOE}$ | Using LVTTL standard | — | 0.60 | — | 0.60 | ns |
| LVCMOS33_in | $t_{IN}$, $t_{GCLK\_IN}$, $t_{GOE}$ | Using LVCMOS 3.3 standard | — | 0.60 | — | 0.60 | ns |
| LVCMOS25_in | $t_{IN}$, $t_{GCLK\_IN}$, $t_{GOE}$ | Using LVCMOS 2.5 standard | — | 0.60 | — | 0.60 | ns |
| LVCMOS18_in | $t_{IN}$, $t_{GCLK\_IN}$, $t_{GOE}$ | Using LVCMOS 1.8 standard | — | 0.00 | — | 0.00 | ns |
| PCI_in | $t_{IN}$, $t_{GCLK\_IN}$, $t_{GOE}$ | Using PCI compatible input | — | 0.60 | — | 0.60 | ns |
| **$t_{IOO}$ Output Adjusters** | | | | | | | |
| LVTTL_out | $t_{BUF}$, $t_{EN}$, $t_{DIS}$ | Output configured as TTL buffer | — | 0.20 | — | 0.20 | ns |
| LVCMOS33_out | $t_{BUF}$, $t_{EN}$, $t_{DIS}$ | Output configured as 3.3V buffer | — | 0.20 | — | 0.20 | ns |
| LVCMOS25_out | $t_{BUF}$, $t_{EN}$, $t_{DIS}$ | Output configured as 2.5V buffer | — | 0.10 | — | 0.10 | ns |
| LVCMOS18_out | $t_{BUF}$, $t_{EN}$, $t_{DIS}$ | Output configured as 1.8V buffer | — | 0.00 | — | 0.00 | ns |
| PCI_out | $t_{BUF}$, $t_{EN}$, $t_{DIS}$ | Output configured as PCI compatible buffer | — | 0.20 | — | 0.20 | ns |
| Slow Slew | $t_{BUF}$, $t_{EN}$ | Output configured for slow slew rate | — | 1.00 | — | 1.00 | ns |

Note: Open drain timing is the same as corresponding LVCMOS timing.

Timing v.3.2

1. Refer to TN1004, ispMACH 4000 Timing Model Design and Usage Guidelines for information regarding use of these adders.

## Boundary Scan Waveforms and Timing Specifications

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $t_{BTCP}$ | TCK [BSCAN test] clock cycle | 40 | — | ns |
| $t_{BTCH}$ | TCK [BSCAN test] pulse width high | 20 | — | ns |
| $t_{BTCL}$ | TCK [BSCAN test] pulse width low | 20 | — | ns |
| $t_{BTSU}$ | TCK [BSCAN test] setup time | 8 | — | ns |
| $t_{BTH}$ | TCK [BSCAN test] hold time | 10 | — | ns |
| $t_{BRF}$ | TCK [BSCAN test] rise and fall time | 50 | — | mV/ns |
| $t_{BTCO}$ | TAP controller falling edge of clock to valid output | — | 10 | ns |
| $t_{BTOZ}$ | TAP controller falling edge of clock to data output disable | — | 10 | ns |
| $t_{BTVO}$ | TAP controller falling edge of clock to data output enable | — | 10 | ns |
| $t_{BTCPSU}$ | BSCAN test Capture register setup time | 8 | — | ns |
| $t_{BTCPH}$ | BSCAN test Capture register hold time | 10 | — | ns |
| $t_{BTUCO}$ | BSCAN test Update reg, falling edge of clock to valid output | — | 25 | ns |
| $t_{BTUOZ}$ | BSCAN test Update reg, falling edge of clock to output disable | — | 25 | ns |
| $t_{BTUOV}$ | BSCAN test Update reg, falling edge of clock to output enable | — | 25 | ns |

## Switching Test Conditions

Figure 12 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 9.

***Figure 12. Output Test Load, LVTTL and LVCMOS Standards***

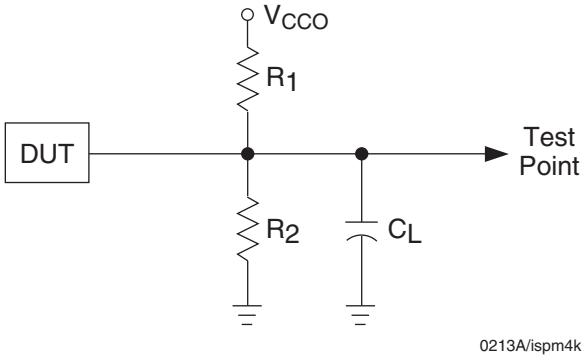



***Table 9. Test Fixture Required Components***

| Test Condition | $R_1$ | $R_2$ | $C_L$[1] | Timing Ref. | $V_{CCO}$ |
|---|---|---|---|---|---|
| LVCMOS I/O, (L -> H, H -> L) | 106Ω | 106Ω | 35pF | LVCMOS 3.3 = 1.5V | LVCMOS 3.3 = 3.0V |
| | | | | LVCMOS 2.5 = $V_{CCO}$/2 | LVCMOS 2.5 = 2.3V |
| | | | | LVCMOS 1.8 = $V_{CCO}$/2 | LVCMOS 1.8 = 1.65V |
| LVCMOS I/O (Z -> H) | ∞ | 106Ω | 35pF | 1.5V | 3.0V |
| LVCMOS I/O (Z -> L) | 106Ω | ∞ | 35pF | 1.5V | 3.0V |
| LVCMOS I/O (H -> Z) | ∞ | 106Ω | 5pF | $V_{OH}$ - 0.3 | 3.0V |
| LVCMOS I/O (L -> Z) | 106Ω | ∞ | 5pF | $V_{OL}$ + 0.3 | 3.0V |

1. $C_L$ includes test fixtures and probe capacitance.

## LA-ispMACH 4000V/Z Power Supply and NC Connections[1]

| Signal | 44 TQFP[2] | 48 TQFP[2] | 100 TQFP[2] | 128 TQFP[2] | 144 TQFP[2] |
|---|---|---|---|---|---|
| VCC | 11, 33 | 12, 36 | 25, 40, 75, 90 | 32, 51, 96, 115 | 36, 57, 108, 129 |
| VCCO0<br>VCCO (Bank 0) | 6 | 6 | 13, 33, 95 | 3, 17, 30, 41, 122 | 3, 19, 34, 47, 136 |
| VCCO1<br>VCCO (Bank 1) | 28 | 30 | 45, 63, 83 | 58, 67, 81, 94, 105 | 64, 75, 91, 106, 119 |
| GND | 12, 34 | 13, 37 | 1, 26, 51, 76 | 1, 33, 65, 97 | 1, 37, 73, 109 |
| GND (Bank 0) | 5 | 5 | 7, 18, 32, 96 | 10, 24, 40, 113, 123 | 10, 18[6], 27, 46, 127, 137 |
| GND (Bank 1) | 27 | 29 | 46, 57, 68, 82 | 49, 59, 74, 88, 104 | 55, 65, 82, 90[6], 99, 118 |
| NC | None | None | None | None | 17, 20, 38, 45, 72, 89, 92, 110, 117, 144 |

1. All grounds must be electrically connected at the board level. However, for the purposes of I/O current loading, grounds are associated with the bank shown.
2. Pin orientation follows the conventional order from pin 1 marking of the top side view and counter-clockwise.

## LA-ispMACH 4032V/Z and 4064V/Z Logic Signal Connections: 48-Pin TQFP

| Pin Number | Bank Number | LA-ispMACH 4032V/Z | | LA-ispMACH 4064V/Z | |
|---|---|---|---|---|---|
| | | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP |
| 36 | - | VCC | - | VCC | - |
| 37 | - | GND | - | GND | - |
| 38 | 1 | B12 | B^12 | D8 | D^4 |
| 39 | 1 | B13 | B^13 | D10 | D^5 |
| 40 | 1 | B14 | B^14 | D12 | D^6 |
| 41 | 1 | B15/GOE1 | B^15 | D14/GOE1 | D^7 |
| 42 | 1 | CLK3/I | - | CLK3/I | - |
| 43 | 0 | CLK0/I | - | CLK0/I | - |
| 44 | 0 | A0/GOE0 | A^0 | A0/GOE0 | A^0 |
| 45 | 0 | A1 | A^1 | A2 | A^1 |
| 46 | 0 | A2 | A^2 | A4 | A^2 |
| 47 | 0 | A3 | A^3 | A6 | A^3 |
| 48 | 0 | A4 | A^4 | A8 | A^4 |

## LA-ispMACH 4064V/Z and 4128V/Z Logic Signal Connections: 100-Pin TQFP

| Pin Number | Bank Number | LA-ispMACH 4064V/Z | | LA-ispMACH 4128V/Z | |
|---|---|---|---|---|---|
| | | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP |
| 1 | - | GND | - | GND | - |
| 2 | - | TDI | - | TDI | - |
| 3 | 0 | A8 | A^8 | B0 | B^0 |
| 4 | 0 | A9 | A^9 | B2 | B^1 |
| 5 | 0 | A10 | A^10 | B4 | B^2 |
| 6 | 0 | A11 | A^11 | B6 | B^3 |
| 7 | 0 | GND (Bank 0) | - | GND (Bank 0) | - |
| 8 | 0 | A12 | A^12 | B8 | B^4 |
| 9 | 0 | A13 | A^13 | B10 | B^5 |
| 10 | 0 | A14 | A^14 | B12 | B^6 |
| 11 | 0 | A15 | A^15 | B13 | B^7 |
| 12* | 0 | I | - | I | - |
| 13 | 0 | VCCO (Bank 0) | - | VCCO (Bank 0) | - |
| 14 | 0 | B15 | B^15 | C14 | C^7 |
| 15 | 0 | B14 | B^14 | C12 | C^6 |
| 16 | 0 | B13 | B^13 | C10 | C^5 |
| 17 | 0 | B12 | B^12 | C8 | C^4 |
| 18 | 0 | GND (Bank 0) | - | GND (Bank 0) | - |
| 19 | 0 | B11 | B^11 | C6 | C^3 |
| 20 | 0 | B10 | B^10 | C5 | C^2 |
| 21 | 0 | B9 | B^9 | C4 | C^1 |
| 22 | 0 | B8 | B^8 | C2 | C^0 |
| 23* | 0 | I | - | I | - |
| 24 | - | TCK | - | TCK | - |

## LA-ispMACH 4128V Logic Signal Connections: 128-Pin TQFP

| Pin Number | Bank Number | LA-ispMACH 4128V | |
|---|---|---|---|
| | | GLB/MC/Pad | ORP |
| 1 | 0 | GND | - |
| 2 | 0 | TDI | - |
| 3 | 0 | VCCO (Bank 0) | - |
| 4 | 0 | B0 | B^0 |
| 5 | 0 | B1 | B^1 |
| 6 | 0 | B2 | B^2 |
| 7 | 0 | B4 | B^3 |
| 8 | 0 | B5 | B^4 |
| 9 | 0 | B6 | B^5 |
| 10 | 0 | GND (Bank 0) | - |
| 11 | 0 | B8 | B^6 |
| 12 | 0 | B9 | B^7 |
| 13 | 0 | B10 | B^8 |
| 14 | 0 | B12 | B^9 |
| 15 | 0 | B13 | B^10 |
| 16 | 0 | B14 | B^11 |
| 17 | 0 | VCCO (Bank 0) | - |
| 18 | 0 | C14 | C^11 |
| 19 | 0 | C13 | C^10 |
| 20 | 0 | C12 | C^9 |
| 21 | 0 | C10 | C^8 |
| 22 | 0 | C9 | C^7 |
| 23 | 0 | C8 | C^6 |
| 24 | 0 | GND (Bank 0) | - |
| 25 | 0 | C6 | C^5 |
| 26 | 0 | C5 | C^4 |
| 27 | 0 | C4 | C^3 |
| 28 | 0 | C2 | C^2 |
| 29 | 0 | C0 | C^0 |
| 30 | 0 | VCCO (Bank 0) | - |
| 31 | 0 | TCK | - |
| 32 | 0 | VCC | - |
| 33 | 0 | GND | - |
| 34 | 0 | D14 | D^11 |
| 35 | 0 | D13 | D^10 |
| 36 | 0 | D12 | D^9 |
| 37 | 0 | D10 | D^8 |
| 38 | 0 | D9 | D^7 |
| 39 | 0 | D8 | D^6 |
| 40 | 0 | GND (Bank 0) | - |
| 41 | 0 | VCCO (Bank 0) | - |
| 42 | 0 | D6 | D^5 |

## LA-ispMACH 4128V Logic Signal Connections: 128-Pin TQFP (Cont.)

| Pin Number | Bank Number | LA-ispMACH 4128V | |
|---|---|---|---|
| | | GLB/MC/Pad | ORP |
| 86 | 1 | G9 | G^7 |
| 87 | 1 | G8 | G^6 |
| 88 | 1 | GND (Bank 1) | - |
| 89 | 1 | G6 | G^5 |
| 90 | 1 | G5 | G^4 |
| 91 | 1 | G4 | G^3 |
| 92 | 1 | G2 | G^2 |
| 93 | 1 | G0 | G^0 |
| 94 | 1 | VCCO (Bank 1) | - |
| 95 | 1 | TDO | - |
| 96 | 1 | VCC | - |
| 97 | 1 | GND | - |
| 98 | 1 | H14 | H^11 |
| 99 | 1 | H13 | H^10 |
| 100 | 1 | H12 | H^9 |
| 101 | 1 | H10 | H^8 |
| 102 | 1 | H9 | H^7 |
| 103 | 1 | H8 | H^6 |
| 104 | 1 | GND (Bank 1) | - |
| 105 | 1 | VCCO (Bank 1) | - |
| 106 | 1 | H6 | H^5 |
| 107 | 1 | H5 | H^4 |
| 108 | 1 | H4 | H^3 |
| 109 | 1 | H2 | H^2 |
| 110 | 1 | H1 | H^1 |
| 111 | 1 | H0/GOE1 | H^0 |
| 112 | 1 | CLK3/I | - |
| 113 | 0 | GND (Bank 0) | - |
| 114 | 0 | CLK0/I | - |
| 115 | 0 | VCC | - |
| 116 | 0 | A0/GOE0 | A^0 |
| 117 | 0 | A1 | A^1 |
| 118 | 0 | A2 | A^2 |
| 119 | 0 | A4 | A^3 |
| 120 | 0 | A5 | A^4 |
| 121 | 0 | A6 | A^5 |
| 122 | 0 | VCCO (Bank 0) | - |
| 123 | 0 | GND (Bank 0) | - |
| 124 | 0 | A8 | A^6 |
| 125 | 0 | A9 | A^7 |
| 126 | 0 | A10 | A^8 |
| 127 | 0 | A12 | A^9 |
| 128 | 0 | A14 | A^11 |

## LA-ispMACH 4128V Logic Signal Connections: 144-Pin TQFP (Cont.)

| Pin Number | Bank Number | LA-ispMACH 4128V | |
|---|---|---|---|
| | | GLB/MC/Pad | ORP |
| 43 | 0 | D9 | D^7 |
| 44 | 0 | D8 | D^6 |
| 45 | 0 | NC | - |
| 46 | 0 | GND (Bank 0) | - |
| 47 | 0 | VCCO (Bank 0) | - |
| 48 | 0 | D6 | D^5 |
| 49 | 0 | D5 | D^4 |
| 50 | 0 | D4 | D^3 |
| 51 | 0 | D2 | D^2 |
| 52 | 0 | D1 | D^1 |
| 53 | 0 | D0 | D^0 |
| 54 | 0 | CLK1/I | - |
| 55 | 1 | GND (Bank 1) | - |
| 56 | 1 | CLK2/I | - |
| 57 | - | VCC | - |
| 58 | 1 | E0 | E^0 |
| 59 | 1 | E1 | E^1 |
| 60 | 1 | E2 | E^2 |
| 61 | 1 | E4 | E^3 |
| 62 | 1 | E5 | E^4 |
| 63 | 1 | E6 | E^5 |
| 64 | 1 | VCCO (Bank 1) | - |
| 65 | 1 | GND (Bank 1) | - |
| 66 | 1 | E8 | E^6 |
| 67 | 1 | E9 | E^7 |
| 68 | 1 | E10 | E^8 |
| 69 | 1 | E12 | E^9 |
| 70 | 1 | E13 | E^10 |
| 71 | 1 | E14 | E^11 |
| 72 | 1 | NC | - |
| 73 | - | GND | - |
| 74 | - | TMS | - |
| 75 | 1 | VCCO (Bank 1) | - |
| 76 | 1 | F0 | F^0 |
| 77 | 1 | F1 | F^1 |
| 78 | 1 | F2 | F^2 |
| 79 | 1 | F4 | F^3 |
| 80 | 1 | F5 | F^4 |
| 81 | 1 | F6 | F^5 |
| 82 | 1 | GND (Bank 1) | - |
| 83 | 1 | F8 | F^6 |
| 84 | 1 | F9 | F^7 |
| 85 | 1 | F10 | F^8 |

## LA-ispMACH 4128V Logic Signal Connections: 144-Pin TQFP (Cont.)

| Pin Number | Bank Number | LA-ispMACH 4128V | |
|---|---|---|---|
| | | GLB/MC/Pad | ORP |
| 86 | 1 | F12 | F^9 |
| 87 | 1 | F13 | F^10 |
| 88 | 1 | F14 | F^11 |
| 89 | 1 | NC | - |
| 90 | 1 | GND (Bank 1)[1] | - |
| 91 | 1 | VCCO (Bank 1) | - |
| 92 | 1 | NC | - |
| 93 | 1 | G14 | G^11 |
| 94 | 1 | G13 | G^10 |
| 95 | 1 | G12 | G^9 |
| 96 | 1 | G10 | G^8 |
| 97 | 1 | G9 | G^7 |
| 98 | 1 | G8 | G^6 |
| 99 | 1 | GND (Bank 1) | - |
| 100 | 1 | G6 | G^5 |
| 101 | 1 | G5 | G^4 |
| 102 | 1 | G4 | G^3 |
| 103 | 1 | G2 | G^2 |
| 104 | 1 | G1 | G^1 |
| 105 | 1 | G0 | G^0 |
| 106 | 1 | VCCO (Bank 1) | - |
| 107 | - | TDO | - |
| 108 | - | VCC | - |
| 109 | - | GND | - |
| 110 | 1 | NC | - |
| 111 | 1 | H14 | H^11 |
| 112 | 1 | H13 | H^10 |
| 113 | 1 | H12 | H^9 |
| 114 | 1 | H10 | H^8 |
| 115 | 1 | H9 | H^7 |
| 116 | 1 | H8 | H^6 |
| 117 | 1 | NC | - |
| 118 | 1 | GND (Bank 1) | - |
| 119 | 1 | VCCO (Bank 1) | - |
| 120 | 1 | H6 | H^5 |
| 121 | 1 | H5 | H^4 |
| 122 | 1 | H4 | H^3 |
| 123 | 1 | H2 | H^2 |
| 124 | 1 | H1 | H^1 |
| 125 | 1 | H0/GOE1 | H^0 |
| 126 | 1 | CLK3/I | - |
| 127 | 0 | GND (Bank 0) | - |
| 128 | 0 | CLK0/I | - |

## LA-ispMACH 4128V Logic Signal Connections: 144-Pin TQFP (Cont.)

| Pin Number | Bank Number | LA-ispMACH 4128V | |
|---|---|---|---|
| | | GLB/MC/Pad | ORP |
| 129 | - | VCC | - |
| 130 | 0 | A0/GOE0 | A^0 |
| 131 | 0 | A1 | A^1 |
| 132 | 0 | A2 | A^2 |
| 133 | 0 | A4 | A^3 |
| 134 | 0 | A5 | A^4 |
| 135 | 0 | A6 | A^5 |
| 136 | 0 | VCCO (Bank 0) | - |
| 137 | 0 | GND (Bank 0) | - |
| 138 | 0 | A8 | A^6 |
| 139 | 0 | A9 | A^7 |
| 140 | 0 | A10 | A^8 |
| 141 | 0 | A12 | A^9 |
| 142 | 0 | A13 | A^10 |
| 143 | 0 | A14 | A^11 |
| 144 | 0 | NC[2] | - |

1. For device migration considerations, these NC pins are GND pins for I/O banks in LA-ispMACH 4128V devices.

# Revision History

| Date | Version | Change Summary |
|---|---|---|
| April 2006 | 01.0 | Initial release. |
| October 2006 | 02.0 | Added LA-ispMACH 4000Z support information throughout. |
| March 2007 | 02.1 | Updated ispMACH 4000 Introduction section. |
| | | Updated Signal Descriptions table. |
| September 2007 | 02.2 | DC Electrical Characteristics table, removed duplicate specifications. |
| July 2008 | 02.3 | Lowered the maximum supply current at 85°C to match the commercial product values. |
| | | Added automotive disclaimer. |
| May 2009 | 02.4 | Correction to $t_{CW}$, tGW, $t_{WIR}$ and $f_{MAX}$ parameters in External Switching Characteristics table. |
| May 2009 | 02.5 | Correction to $t_{CW}$, tGW and $t_{WIR}$ parameters in External Switching Characteristics table. |