Lattice Semiconductor Corporation - LA4128ZC-75TN100E Datasheet

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	1.7V ~ 1.9V
Number of Logic Elements/Blocks	-
Number of Macrocells	128
Number of Gates	-
Number of I/O	64
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/la4128zc-75tn100e

The I/Os in the LA-ispMACH 4000V/Z automotive devices are split into two banks. Each bank has a separate I/O power supply. Inputs can support a variety of standards independent of the chip or bank power supply. Outputs support the standards compatible with the power supply provided to the bank. Support for a variety of standards helps designers implement designs in mixed voltage environments. In addition, 5V tolerant inputs are specified within an I/O bank that is connected to V_{CCO} of 3.0V to 3.6V for LVCMOS 3.3, LVTTL and PCI interfaces.

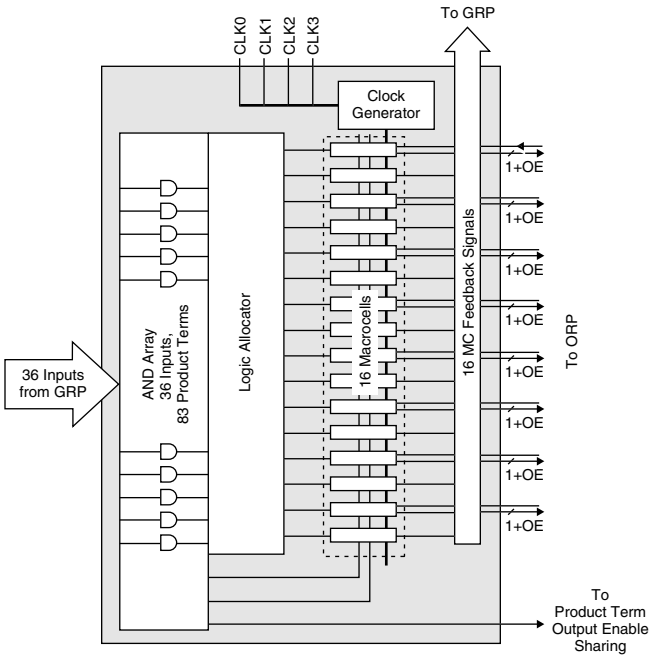
LA-ispMACH 4000V/Z Automotive Architecture

There are a total of two GLBs in the LA-ispMACH 4032V/Z, increasing to 8 GLBs in the LA-ispMACH 4128V/Z. Each GLB has 36 inputs. All GLB inputs come from the GRP and all outputs from the GLB are brought back into the GRP to be connected to the inputs of any other GLB on the device. Even if feedback signals return to the same GLB, they still must go through the GRP. This mechanism ensures that GLBs communicate with each other with consistent and predictable delays. The outputs from the GLB are also sent to the ORP. The ORP then sends them to the associated I/O cells in the I/O block.

Generic Logic Block

The LA-ispMACH 4000V/Z Automotive GLB consists of a programmable AND array, logic allocator, 16 macrocells and a GLB clock generator. Macrocells are decoupled from the product terms through the logic allocator and the I/O pins are decoupled from macrocells through the ORP. Figure 2 illustrates the GLB.

Figure 2. Generic Logic Block



AND Array

The programmable AND Array consists of 36 inputs and 83 output product terms. The 36 inputs from the GRP are used to form 72 lines in the AND Array (true and complement of the inputs). Each line in the array can be connected to any of the 83 output product terms via a wired-AND. Each of the 80 logic product terms feed the logic allocator with the remaining three control product terms feeding the Shared PT Clock, Shared PT Initialization and Shared PT OE. The Shared PT Clock and Shared PT Initialization signals can optionally be inverted before being fed to the macrocells.

Every set of five product terms from the 80 logic product terms forms a product term cluster starting with PT0. There is one product term cluster for every macrocell in the GLB. Figure 3 is a graphical representation of the AND Array.

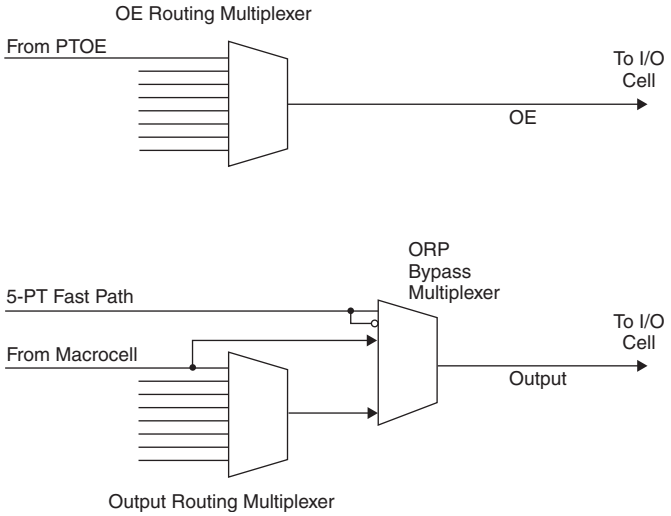
Output Routing Pool (ORP)

The Output Routing Pool allows macrocell outputs to be connected to any of several I/O cells within an I/O block. This provides greater flexibility in determining the pinout and allows design changes to occur without affecting the pinout. The output routing pool also provides a parallel capability for routing macrocell-level OE product terms. This allows the OE product term to follow the macrocell output as it is switched between I/O cells. Additionally, the output routing pool allows the macrocell output or true and complement forms of the 5-PT bypass signal to bypass the output routing multiplexers and feed the I/O cell directly. The enhanced ORP of the LA-ispMACH 4000V/Z family consists of the following elements:

- Output Routing Multiplexers
- OE Routing Multiplexers
- Output Routing Pool Bypass Multiplexers

Figure 7 shows the structure of the ORP from the I/O cell perspective. This is referred to as an ORP slice. Each ORP has as many ORP slices as there are I/O cells in the corresponding I/O block.

Figure 7. ORP Slice



Output Routing Multiplexers

The details of connections between the macrocells and the I/O cells vary across devices and within a device dependent on the maximum number of I/Os available. Tables 6-10 provide the connection details.

Table 6. ORP Combinations for I/O Blocks with 8 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M2, M3, M4, M5, M6, M7, M8, M9
I/O 2	M4, M5, M6, M7, M8, M9, M10, M11
I/O 3	M6, M7, M8, M9, M10, M11, M12, M13
I/O 4	M8, M9, M10, M11, M12, M13, M14, M15
I/O 5	M10, M11, M12, M13, M14, M15, M0, M1
I/O 6	M12, M13, M14, M15, M0, M1, M2, M3
I/O 7	M14, M15, M0, M1, M2, M3, M4, M5

Table 7. ORP Combinations for I/O Blocks with 16 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M1, M2, M3, M4, M5, M6, M7, M8
I/O 2	M2, M3, M4, M5, M6, M7, M8, M9
I/O 3	M3, M4, M5, M6, M7, M8, M9, M10
I/O 4	M4, M5, M6, M7, M8, M9, M10, M11
I/O 5	M5, M6, M7, M8, M9, M10, M11, M12
I/O 6	M6, M7, M8, M9, M10, M11, M12, M13
I/O 7	M7, M8, M9, M10, M11, M12, M13, M14
I/O 8	M8, M9, M10, M11, M12, M13, M14, M15
I/O 9	M9, M10, M11, M12, M13, M14, M15, M0
I/O 10	M10, M11, M12, M13, M14, M15, M0, M1
I/O 11	M11, M12, M13, M14, M15, M0, M1, M2
I/O 12	M12, M13, M14, M15, M0, M1, M2, M3
I/O 13	M13, M14, M15, M0, M1, M2, M3, M4
I/O 14	M14, M15, M0, M1, M2, M3, M4, M5
I/O 15	M15, M0, M1, M2, M3, M4, M5, M6

Table 8. ORP Combinations for I/O Blocks with 12 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M1, M2, M3, M4, M5, M6, M7, M8
I/O 2	M2, M3, M4, M5, M6, M7, M8, M9
I/O 3	M4, M5, M6, M7, M8, M9, M10, M11
I/O 4	M5, M6, M7, M8, M9, M10, M11, M12
I/O 5	M6, M7, M8, M9, M10, M11, M12, M13
I/O 6	M8, M9, M10, M11, M12, M13, M14, M15
I/O 7	M9, M10, M11, M12, M13, M14, M15, M0
I/O 8	M10, M11, M12, M13, M14, M15, M0, M1
I/O 9	M12, M13, M14, M15, M0, M1, M2, M3
I/O 10	M13, M14, M15, M0, M1, M2, M3, M4
I/O 11	M14, M15, M0, M1, M2, M3, M4, M5

ORP Bypass and Fast Output Multiplexers

The ORP bypass and fast-path output multiplexer is a 4:1 multiplexer and allows the 5-PT fast path to bypass the ORP and be connected directly to the pin with either the regular output or the inverted output. This multiplexer also allows the register output to bypass the ORP to achieve faster t_{CO}.

Output Enable Routing Multiplexers

The OE Routing Pool provides the corresponding local output enable (OE) product term to the I/O cell.

I/O Cell

The I/O cell contains the following programmable elements: output buffer, input buffer, OE multiplexer and bus maintenance circuitry. Figure 8 details the I/O cell.

Figure 9. Global OE Generation for All Devices Except LA-ispMACH 4032V/Z

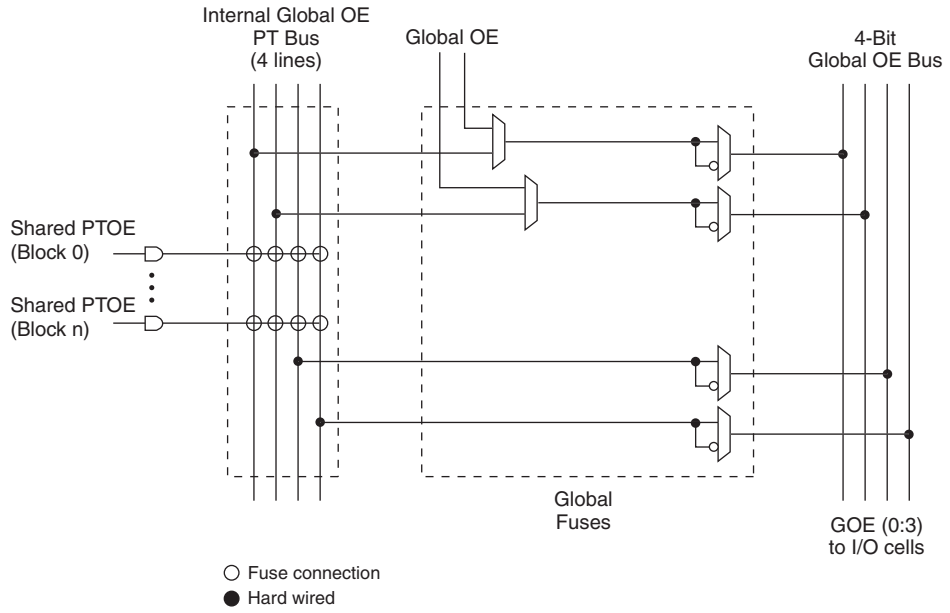
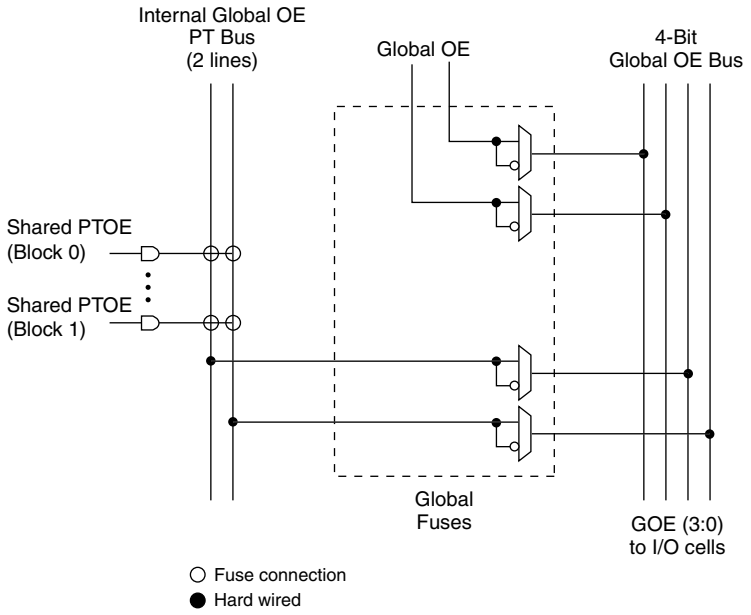


Figure 10. Global OE Generation for LA-ispMACH 4032V/Z



Zero Power/Low Power and Power Management

The LA-ispMACH 4000V/Z automotive family is designed with high speed low power design techniques to offer both high speed and low power. With an advanced E^2 low power cell and non sense-amplifier design approach (full CMOS logic approach), the LA-ispMACH 4000V/Z automotive family offers SuperFAST pin-to-pin speeds, while simultaneously delivering low standby power without needing any “turbo bits” or other power management schemes associated with a traditional sense-amplifier approach.

The zero power LA-ispMACH 4000Z is based on the 1.8V ispMACH 4000C family. With innovative circuit design changes, the LA-ispMACH 4000Z family is able to achieve the industry's "lowest static power".

IEEE 1149.1-Compliant Boundary Scan Testability

All LA-ispMACH 4000V/Z automotive devices have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic notes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more board-level testing. The test access port operates with an LVCMOS interface that corresponds to the power supply voltage.

I/O Quick Configuration

To facilitate the most efficient board test, the physical nature of the I/O cells must be set before running any continuity tests. As these tests are fast, by nature, the overhead and time that is required for configuration of the I/Os' physical nature should be minimal so that board test time is minimized. The LA-ispMACH 4000V/Z automotive family of devices allows this by offering the user the ability to quickly configure the physical nature of the I/O cells. This quick configuration takes milliseconds to complete, whereas it takes seconds for the entire device to be programmed. Lattice's ispVM™ System programming software can either perform the quick configuration through the PC parallel port, or can generate the ATE or test vectors necessary for a third-party test system.

IEEE 1532-Compliant In-System Programming

Programming devices in-system provides a number of significant benefits including: rapid prototyping, lower inventory levels, higher quality and the ability to make in-field modifications. The LA-ispMACH 4000V/Z automotive devices provide In-System Programming (ISP™) capability through the Boundary Scan Test Access Port. This capability has been implemented in a manner that ensures that the port remains complaint to the IEEE 1149.1 standard. By using IEEE 1149.1 as the communication interface through which ISP is achieved, users get the benefit of a standard, well-defined interface. All LA-ispMACH 4000V/Z automotive devices are also compliant with the IEEE 1532 standard.

The LA-ispMACH 4000V/Z automotive devices can be programmed across the commercial temperature and voltage range. The PC-based Lattice software facilitates in-system programming of LA-ispMACH 4000V/Z automotive devices. The software takes the JEDEC file output produced by the design implementation software, along with information about the scan chain, and creates a set of vectors used to drive the scan chain. The software can use these vectors to drive a scan chain via the parallel port of a PC. Alternatively, the software can output files in formats understood by common automated test equipment. This equipment can then be used to program LA-ispMACH 4000V/Z automotive devices during the testing of a circuit board.

User Electronic Signature

The User Electronic Signature (UES) allows the designer to include identification bits or serial numbers inside the device, stored in E^2CMOS memory. The LA-ispMACH 4000V/Z automotive device contains 32 UES bits that can be configured by the user to store unique data such as ID codes, revision numbers or inventory control codes.

Security Bit

A programmable security bit is provided on the LA-ispMACH 4000V/Z automotive devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

Hot Socketing

The LA-ispMACH 4000V/Z automotive devices are well-suited for applications that require hot socketing capability. Hot socketing a device requires that the device, during power-up and down, can tolerate active signals on the I/Os

and inputs without being damaged. Additionally, it requires that the effects of I/O pin loading be minimal on active signals. The LA-ispMACH 4000V/Z automotive devices provide this capability for input voltages in the range 0V to 3.0V.

Density Migration

The LA-ispMACH 4000V/Z automotive family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is possible to shift a lower utilization design targeted for a high density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

AEC-Q100 Tested and Qualified

The Automotive Electronics Council (AEC) consists of two committees: the Quality Systems Committee and the Component Technical Committee. These committees are composed of representatives from sustaining and other associate members. The AEC Component Technical Committee is the standardization body for establishing standards for reliable, high quality electronic components. In particular, the AEC-Q100 specification “Stress Test for Qualification for Integrated Circuits” defines qualification and re-qualification requirements for electronic components. Components meeting these specifications are suitable for use in the harsh automotive environment without additional component-level qualification testing. Lattice's LA-ispMACH 4000V/Z and LA-MachXO devices completed and passed the requirements of the AEC-Q100 specification.

I/O Recommended Operating Conditions

Standard	V_{CCO} (V)[1]	
	Min.	Max.
LVTTL	3.0	3.6
LVCMOS 3.3	3.0	3.6
Extended LVCMOS 3.3[2]	2.7	3.6
LVCMOS 2.5	2.3	2.7
LVCMOS 1.8	1.65	1.95
PCI 3.3	3.0	3.6

1. Typical values for V_{CCO} are the average of the min. and max. values.
2. LA-ispMACH 4000Z only.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1, 4]	Input Leakage Current (LA-ispMACH 4000Z)	$0 \le V_{IN} < V_{CCO}$	—	0.5	1	µA
I_{IH}[1, 2]	Input High Leakage Current (LA-ispMACH 4000V)	$3.6V < V_{IN} \le 5.5V$, $T_j = 105°C$ $3.0V \le V_{CCO} \le 3.6V$	—	—	20	µA
		$3.6V < V_{IN} \le 5.5V$, $T_j = 130°C$ $3.0V \le V_{CCO} \le 3.6V$	—	—	50	µA
	Input High Leakage Current (LA-ispMACH 4000Z)	$V_{CCO} < V_{IN} \le 5.5V$	—	—	10	µA
I_{PU}	I/O Weak Pull-up Resistor Current (LA-ispMACH 4000V)	$0 \le V_{IN} \le 0.7V_{CCO}$	-30	—	-200	µA
	I/O Weak Pull-up Resistor Current (LA-ispMACH 4000Z)	$0 \le V_{IN} \le 0.7V_{CCO}$	-30	—	-150	µA
I_{PD}	I/O Weak Pull-down Resistor Current	V_{IL} (MAX) $\le V_{IN} \le V_{IH}$ (MIN)	30	—	150	µA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7\ V_{CCO}$	-30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive Current	$0V \le V_{IN} \le V_{BHT}$	—	—	150	µA
I_{BHHO}	Bus Hold High Overdrive Current	$V_{BHT} \le V_{IN} \le V_{CCO}$	—	—	-150	µA
V_{BHT}	Bus Hold Trip Points	—	V_{CCO} * 0.35	—	V_{CCO} * 0.65	V
C_1	I/O Capacitance[3]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	8	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	
C_2	Clock Capacitance[3]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	6	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	
C_3	Global Input Capacitance[3]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	6	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. 5V tolerant inputs and I/O should only be placed in banks where $3.0V \le V_{CCO} \le 3.6V$.
3. $T_A = 25°C$, f = 1.0MHz.
4. I_{IH} excursions of up to 1.5µA maximum per pin above the spec limit may be observed for certain voltage conditions on no more than 10% of the device's I/O pins.

Supply Current, LA-ispMACH 4000Z

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
LA-ispMACH 4032Z						
ICC[1, 2, 3, 5]	Operating Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	50	—	µA
		Vcc = 1.9V, T_A = 70°C	—	58	—	µA
		Vcc = 1.9V, T_A = 85°C	—	60	—	µA
		Vcc = 1.9V, T_A = 125°C	—	70	—	µA
ICC[4, 5]	Standby Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	10	—	µA
		Vcc = 1.9V, T_A = 70°C	—	13	20	µA
		Vcc = 1.9V, T_A = 85°C	—	15	25	µA
		Vcc = 1.9V, T_A = 125°C	—	22		µA
LA-ispMACH 4064Z						
ICC[1, 2, 3, 5]	Operating Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	80	—	µA
		Vcc = 1.9V, T_A = 70°C	—	89	—	µA
		Vcc = 1.9V, T_A = 85°C	—	92	—	µA
		Vcc = 1.9V, T_A = 125°C	—	109	—	µA
ICC[4, 5]	Standby Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	11	—	µA
		Vcc = 1.9V, T_A = 70°C	—	15	25	µA
		Vcc = 1.9V, T_A = 85°C	—	18	35	µA
		Vcc = 1.9V, T_A = 125°C	—	37		µA
LA-ispMACH 4128Z						
ICC[1, 2, 3, 5]	Operating Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	168	—	µA
		Vcc = 1.9V, T_A = 70°C	—	190	—	µA
		Vcc = 1.9V, T_A = 85°C	—	195	—	µA
		Vcc = 1.9V, T_A = 125°C	—	212	—	µA
ICC[4, 5]	Standby Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	12	—	µA
		Vcc = 1.9V, T_A = 70°C	—	16	35	µA
		Vcc = 1.9V, T_A = 85°C	—	19	50	µA
		Vcc = 1.9V, T_A = 125°C	—	42	—	µA

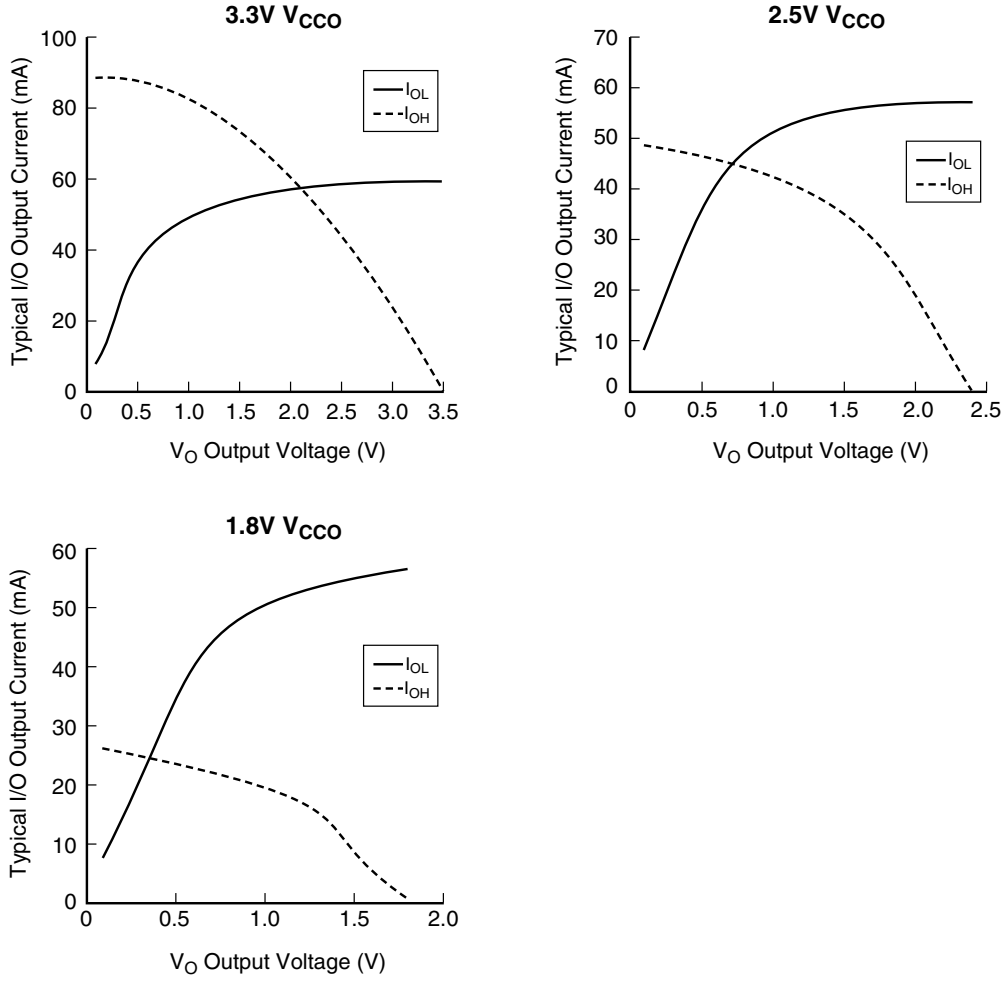
1. T_A = 25°C, frequency = 1.0 MHz.
2. Device configured with 16-bit counters.
3. I_{CC} varies with specific device configuration and operating frequency.
4. V_{CCO} = 3.6V, V_{IN} = 0V or $V_{CCO,}$ bus maintenance turned off. V_{IN} above V_{CCO} will add transient current above the specified standby I_{CC}.
5. Includes V_{CCO} current without output loading.

I/O DC Electrical Characteristics

Over Recommended Operating Conditions

Standard	V_{IL}		V_{IH}		V_{OL} Max (V)	V_{OH} Min (V)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVTTL	-0.3	0.80	2.0	5.5	0.40	V_{CCO} - 0.40	8.0	-4.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
LVCMOS 3.3	-0.3	0.80	2.0	5.5	0.40	V_{CCO} - 0.40	8.0	-4.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
LVCMOS 2.5	-0.3	0.70	1.70	3.6	0.40	V_{CCO} - 0.40	8.0	-4.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
LVCMOS 1.8 (4000V)	-0.3	0.63	1.17	3.6	0.40	V_{CCO} - 0.45	2.0	-2.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
LVCMOS 1.8 (4000Z)	-0.3	0.35 * V_{CC}	0.65 * V_{CC}	3.6	0.40	V_{CCO} - 0.45	2.0	-2.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
PCI 3.3 (4000V)	-0.3	1.08	1.5	5.5	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5
PCI 3.3 (4000Z)	-0.3	0.3 * 3.3 * (V_{CC} / 1.8)	0.5 * 3.3 * (V_{CC} / 1.8)	5.5	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5

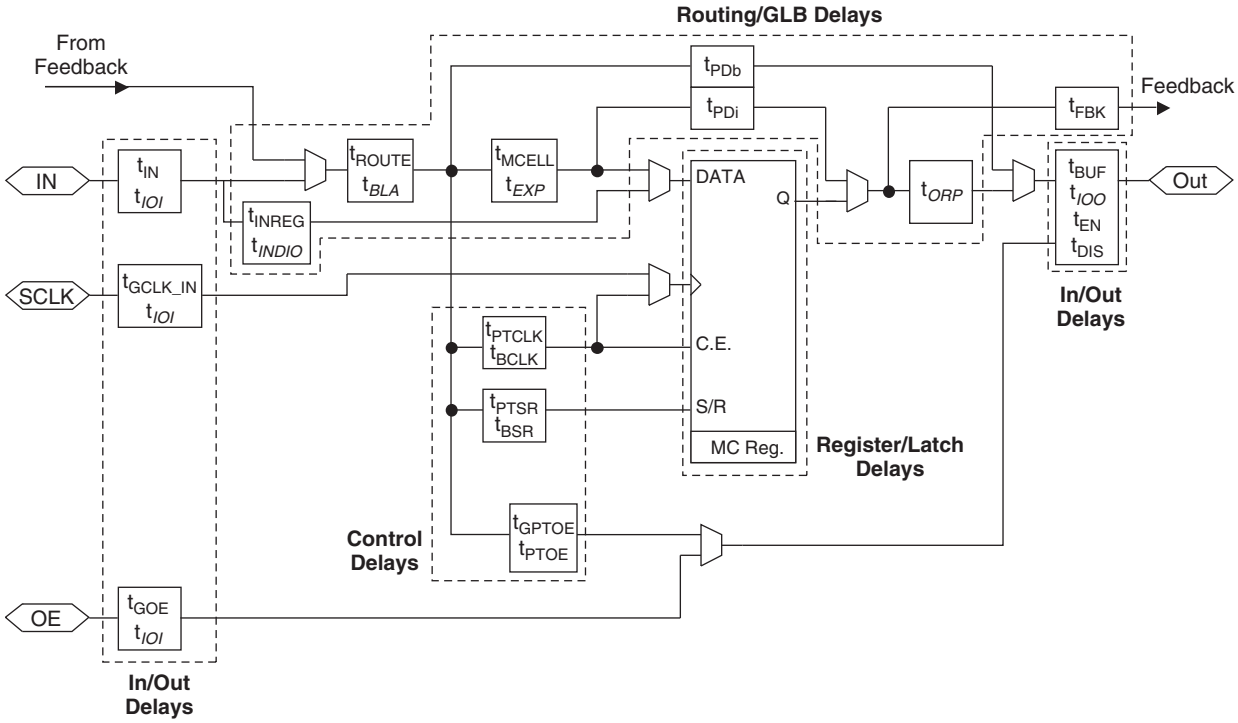
1. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank, as shown in the logic signals connection table, shall not exceed *n**8mA. Where *n* is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.



Timing Model

The task of determining the timing through the LA-ispMACH 4000V/Z automotive family, like any CPLD, is relatively simple. The timing model provided in Figure 11 shows the specific delay paths. Once the implementation of a given function is determined either conceptually or from the software report file, the delay path of the function can easily be determined from the timing model. The Lattice design tools report the timing delays based on the same timing model for a particular design. Note that the internal timing parameters are given for reference only, and are not tested. The external timing parameters are tested and guaranteed for every device. For more information on the timing model and usage, refer to TN1004, ispMACH 4000 Timing Model Design and Usage Guidelines.

Figure 11. LA-ispMACH 4000V/Z Automotive Timing Model



Note: Italicized items are optional delay adders.

LA-ispMACH 4000V/Z Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	LA-ispMACH 4000V -75		LA-ispMACH 4000Z -75		Units
		Min.	Max.	Min.	Max.	
t_{BSR}	GLB PT Set/Reset Delay	—	1.83	—	1.83	ns
t_{PTSR}	Macrocell PT Set/Reset Delay	—	3.41	—	2.72	ns
t_{GPTOE}	Global PT OE Delay	—	5.58	—	3.50	ns
t_{PTOE}	Macrocell PT OE Delay	—	4.28	—	2.00	ns

Timing v.3.2

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the Timing Model in this data sheet for further details.

Boundary Scan Waveforms and Timing Specifications

Symbol	Parameter	Min.	Max.	Units
t_{BTCP}	TCK [BSCAN test] clock cycle	40	—	ns
t_{BTCH}	TCK [BSCAN test] pulse width high	20	—	ns
t_{BTCL}	TCK [BSCAN test] pulse width low	20	—	ns
t_{BTSU}	TCK [BSCAN test] setup time	8	—	ns
t_{BTH}	TCK [BSCAN test] hold time	10	—	ns
t_{BRF}	TCK [BSCAN test] rise and fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
t_{BTOZ}	TAP controller falling edge of clock to data output disable	—	10	ns
t_{BTVO}	TAP controller falling edge of clock to data output enable	—	10	ns
t_{BTCPSU}	BSCAN test Capture register setup time	8	—	ns
t_{BTCPH}	BSCAN test Capture register hold time	10	—	ns
t_{BTUCO}	BSCAN test Update reg, falling edge of clock to valid output	—	25	ns
t_{BTUOZ}	BSCAN test Update reg, falling edge of clock to output disable	—	25	ns
t_{BTUOV}	BSCAN test Update reg, falling edge of clock to output enable	—	25	ns

Signal Descriptions

Signal Names	Description	
TMS	Input – This pin is the IEEE 1149.1 Test Mode Select input, which is used to control the state machine	
TCK	Input – This pin is the IEEE 1149.1 Test Clock input pin, used to clock through the state machine	
TDI	Input – This pin is the IEEE 1149.1 Test Data In pin, used to load data	
TDO	Output – This pin is the IEEE 1149.1 Test Data Out pin used to shift data out	
GOE0/IO, GOE1/IO	These pins are configured to be either Global Output Enable Input or as general I/O pins	
GND	Ground	
NC	Not Connected	
V_{CC}	The power supply pins for the logic core and JTAG port	
CLK0/I, CLK1/I, CLK2/I, CLK3/I	These pins are configured to be either CLK input or as an input	
V_{CCO0}, V_{CCO1}	The power supply pins for each I/O bank	
yzz	Input/Output[1] – These are the general purpose I/O used by the logic array. y is GLB reference (alpha) and z is macrocell reference (numeric). z: 0-15	
	LA-ispMACH 4032V/Z	y: A-B
	LA-ispMACH 4064V/Z	y: A-D
	LA-ispMACH 4128V/Z	y: A-H

1. In some packages, certain I/Os are only available for use as inputs. See the signal connections table for details.

LA-ispMACH 4000V ORP Reference Table

	4032V		4064V			4128V		
Number of I/Os	30[1]	32	30[2]	32	64	64	92[3]	96
Number of GLBs	2	2	4	4	4	8	8	8
Number of I/Os /GLB	16	16	8	8	16	8	12	12
Reference ORP Table	16 I/Os / GLB		8 I/Os / GLB		16 I/Os / GLB	8 I/Os /GLB	12 I/Os / GLB	

1. 32-macrocell device, 44 TQFP: 2 GLBs have 15 out of 16 I/Os bonded out.
2. 64-macrocells device, 44 TQFP: 2 GLBs have 7 out of 8 I/Os bonded out.
3. 128-macrocell device, 128 TQFP: 4 GLBs have 11 out of 12 I/Os

LA-ispMACH 4000Z ORP Reference Table

	4032Z	4064Z		4128Z
Number of I/Os	32	32	64	64
Number of GLBs	2	4	4	8
Number of I/Os / GLB	16	8	16	8
Reference ORP Table	16 I/Os / GLB	8 I/Os / GLB	16 I/Os / GLB	8 I/Os / GLB

LA-ispMACH 4032V and 4064V Logic Signal Connections: 44-Pin TQFP

Pin Number	Bank Number	LA-ispMACH 4032V		LA-ispMACH 4064V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
43	0	A3	A^3	A6	A^3
44	0	A4	A^4	A8	A^4

LA-ispMACH 4032V/Z and 4064V/Z Logic Signal Connections: 48-Pin TQFP

Pin Number	Bank Number	LA-ispMACH 4032V/Z		LA-ispMACH 4064V/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	TDI	-	TDI	-
2	0	A5	A^5	A10	A^5
3	0	A6	A^6	A12	A^6
4	0	A7	A^7	A14	A^7
5	0	GND (Bank 0)	-	GND (Bank 0)	-
6	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
7	0	A8	A^8	B0	B^0
8	0	A9	A^9	B2	B^1
9	0	A10	A^10	B4	B^2
10	0	A11	A^11	B6	B^3
11	-	TCK	-	TCK	-
12	-	VCC	-	VCC	-
13	-	GND	-	GND	-
14	0	A12	A^12	B8	B^4
15	0	A13	A^13	B10	B^5
16	0	A14	A^14	B12	B^6
17	0	A15	A^15	B14	B^7
18	0	CLK1/I	-	CLK1/I	-
19	1	CLK2/I	-	CLK2/I	-
20	1	B0	B^0	C0	C^0
21	1	B1	B^1	C2	C^1
22	1	B2	B^2	C4	C^2
23	1	B3	B^3	C6	C^3
24	1	B4	B^4	C8	C^4
25	-	TMS	-	TMS	-
26	1	B5	B^5	C10	C^5
27	1	B6	B^6	C12	C^6
28	1	B7	B^7	C14	C^7
29	1	GND (Bank 1)	-	GND (Bank 1)	-
30	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
31	1	B8	B^8	D0	D^0
32	1	B9	B^9	D2	D^1
33	1	B10	B^10	D4	D^2
34	1	B11	B^11	D6	D^3
35	-	TDO	-	TDO	-

LA-ispMACH 4064V/Z and 4128V/Z Logic Signal Connections: 100-Pin TQFP

Pin Number	Bank Number	LA-ispMACH 4064V/Z		LA-ispMACH 4128V/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
25	-	VCC	-	VCC	-
26	-	GND	-	GND	-
27*	0	I	-	I	-
28	0	B7	B^7	D13	D^7
29	0	B6	B^6	D12	D^6
30	0	B5	B^5	D10	D^5
31	0	B4	B^4	D8	D^4
32	0	GND (Bank 0)	-	GND (Bank 0)	-
33	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
34	0	B3	B^3	D6	D^3
35	0	B2	B^2	D4	D^2
36	0	B1	B^1	D2	D^1
37	0	B0	B^0	D0	D^0
38	0	CLK1/I	-	CLK1/I	-
39	1	CLK2/I	-	CLK2/I	-
40	-	VCC	-	VCC	-
41	1	C0	C^0	E0	E^0
42	1	C1	C^1	E2	E^1
43	1	C2	C^2	E4	E^2
44	1	C3	C^3	E6	E^3
45	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
46	1	GND (Bank 1)	-	GND (Bank 1)	-
47	1	C4	C^4	E8	E^4
48	1	C5	C^5	E10	E^5
49	1	C6	C^6	E12	E^6
50	1	C7	C^7	E14	E^7
51	-	GND	-	GND	-
52	-	TMS	-	TMS	-
53	1	C8	C^8	F0	F^0
54	1	C9	C^9	F2	F^1
55	1	C10	C^10	F4	F^2
56	1	C11	C^11	F6	F^3
57	1	GND (Bank 1)	-	GND (Bank 1)	-
58	1	C12	C^12	F8	F^4
59	1	C13	C^13	F10	F^5
60	1	C14	C^14	F12	F^6
61	1	C15	C^15	F13	F^7
62*	1	I	-	I	-
63	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
64	1	D15	D^15	G14	G^7
65	1	D14	D^14	G12	G^6
66	1	D13	D^13	G10	G^5
67	1	D12	D^12	G8	G^4

LA-ispMACH 4064V/Z and 4128V/Z Logic Signal Connections: 100-Pin TQFP

Pin Number	Bank Number	LA-ispMACH 4064V/Z		LA-ispMACH 4128V/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
68	1	GND (Bank 1)	-	GND (Bank 1)	-
69	1	D11	D^11	G6	G^3
70	1	D10	D^10	G5	G^2
71	1	D9	D^9	G4	G^1
72	1	D8	D^8	G2	G^0
73*	1	I	-	I	-
74	-	TDO	-	TDO	-
75	-	VCC	-	VCC	-
76	-	GND	-	GND	-
77*	1	I	-	I	-
78	1	D7	D^7	H13	H^7
79	1	D6	D^6	H12	H^6
80	1	D5	D^5	H10	H^5
81	1	D4	D^4	H8	H^4
82	1	GND (Bank 1)	-	GND (Bank 1)	-
83	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
84	1	D3	D^3	H6	H^3
85	1	D2	D^2	H4	H^2
86	1	D1	D^1	H2	H^1
87	1	D0/GOE1	D^0	H0/GOE1	H^0
88	1	CLK3/I	-	CLK3/I	-
89	0	CLK0/I	-	CLK0/I	-
90	-	VCC	-	VCC	-
91	0	A0/GOE0	A^0	A0/GOE0	A^0
92	0	A1	A^1	A2	A^1
93	0	A2	A^2	A4	A^2
94	0	A3	A^3	A6	A^3
95	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
96	0	GND (Bank 0)	-	GND (Bank 0)	-
97	0	A4	A^4	A8	A^4
98	0	A5	A^5	A10	A^5
99	0	A6	A^6	A12	A^6
100	0	A7	A^7	A14	A^7

*This pin is input only.

LA-ispMACH 4128V Logic Signal Connections: 128-Pin TQFP (Cont.)

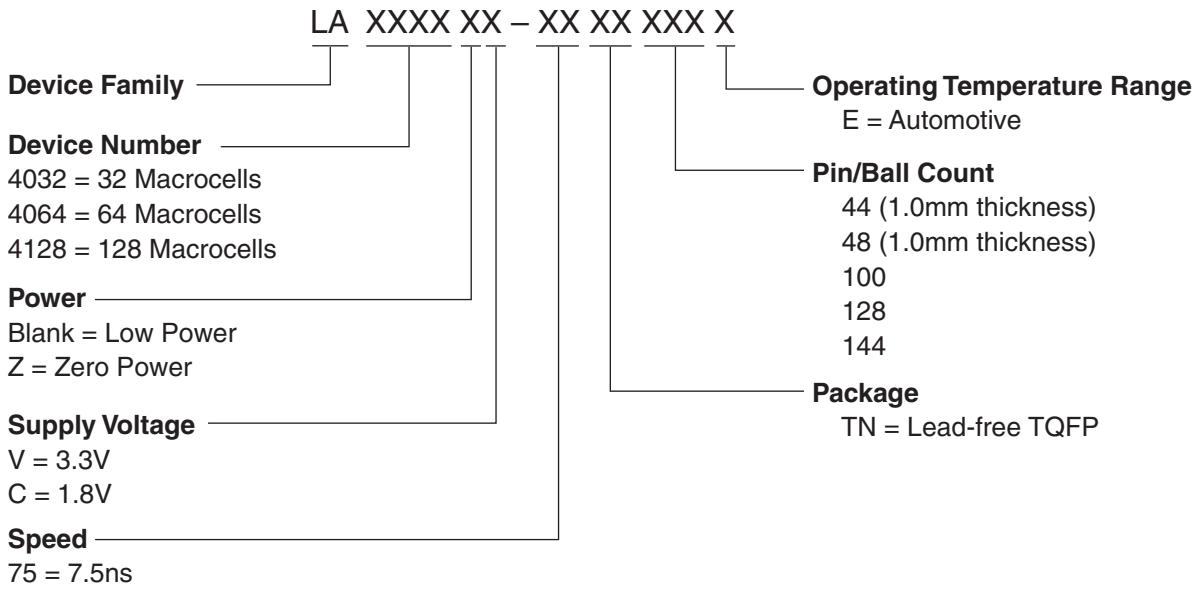
Pin Number	Bank Number	LA-ispMACH 4128V	
		GLB/MC/Pad	ORP
86	1	G9	G^7
87	1	G8	G^6
88	1	GND (Bank 1)	-
89	1	G6	G^5
90	1	G5	G^4
91	1	G4	G^3
92	1	G2	G^2
93	1	G0	G^0
94	1	VCCO (Bank 1)	-
95	1	TDO	-
96	1	VCC	-
97	1	GND	-
98	1	H14	H^11
99	1	H13	H^10
100	1	H12	H^9
101	1	H10	H^8
102	1	H9	H^7
103	1	H8	H^6
104	1	GND (Bank 1)	-
105	1	VCCO (Bank 1)	-
106	1	H6	H^5
107	1	H5	H^4
108	1	H4	H^3
109	1	H2	H^2
110	1	H1	H^1
111	1	H0/GOE1	H^0
112	1	CLK3/I	-
113	0	GND (Bank 0)	-
114	0	CLK0/I	-
115	0	VCC	-
116	0	A0/GOE0	A^0
117	0	A1	A^1
118	0	A2	A^2
119	0	A4	A^3
120	0	A5	A^4
121	0	A6	A^5
122	0	VCCO (Bank 0)	-
123	0	GND (Bank 0)	-
124	0	A8	A^6
125	0	A9	A^7
126	0	A10	A^8
127	0	A12	A^9
128	0	A14	A^11

LA-ispMACH 4128V Logic Signal Connections: 144-Pin TQFP (Cont.)

Pin Number	Bank Number	LA-ispMACH 4128V	
		GLB/MC/Pad	ORP
129	-	VCC	-
130	0	A0/GOE0	A^0
131	0	A1	A^1
132	0	A2	A^2
133	0	A4	A^3
134	0	A5	A^4
135	0	A6	A^5
136	0	VCCO (Bank 0)	-
137	0	GND (Bank 0)	-
138	0	A8	A^6
139	0	A9	A^7
140	0	A10	A^8
141	0	A12	A^9
142	0	A13	A^10
143	0	A14	A^11
144	0	NC[2]	-

1. For device migration considerations, these NC pins are GND pins for I/O banks in LA-ispMACH 4128V devices.

Part Number Description



Ordering Information

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LA4032V	LA4032V-75TN48E	32	3.3	7.5	Lead-free TQFP	48	32	E
	LA4032V-75TN44E	32	3.3	7.5	Lead-free TQFP	44	30	E
LA4064V	LA4064V-75TN100E	64	3.3	7.5	Lead-free TQFP	100	64	E
	LA4064V-75TN48E	64	3.3	7.5	Lead-free TQFP	48	32	E
	LA4064V-75TN44E	64	3.3	7.5	Lead-free TQFP	44	30	E
LA4128V	LA4128V-75TN144E	128	3.3	7.5	Lead-free TQFP	144	96	E
	LA4128V-75TN128E	128	3.3	7.5	Lead-free TQFP	128	92	E
	LA4128V-75TN100E	128	3.3	7.5	Lead-free TQFP	100	64	E
LA4032Z	LA4032ZC-75TN48E	32	1.8	7.5	Lead-free TQFP	48	32	E
LA4064Z	LA4064ZC-75TN100E	64	1.8	7.5	Lead-free TQFP	100	64	E
	LA4064ZC-75TN48E	64	1.8	7.5	Lead-free TQFP	48	32	E
LA4128Z	LA4128ZC-75TN100E	128	1.8	7.5	Lead-free TQFP	100	64	E

Automotive Disclaimer

Products are not designed, intended or warranted to be fail-safe and are not designed, intended or warranted for use in applications related to the deployment of airbags. Further, products are not intended to be used, designed or warranted for use in applications that affect the control of the vehicle unless there is a fail-safe or redundancy feature and also a warning signal to the operator of the vehicle upon failure. Use of products in such applications is fully at the risk of the customer, subject to applicable laws and regulations governing limitations on product liability.

For Further Information

In addition to this data sheet, the following technical notes may be helpful when designing with the LA-ispMACH 4000V/Z automotive family:

- TN1004, ispMACH 4000 Timing Model Design and Usage Guidelines
- TN1005, Power Estimation in ispMACH 4000V/B/C/Z Devices

Revision History

Date	Version	Change Summary
April 2006	01.0	Initial release.
October 2006	02.0	Added LA-ispMACH 4000Z support information throughout.
March 2007	02.1	Updated ispMACH 4000 Introduction section.
		Updated Signal Descriptions table.
September 2007	02.2	DC Electrical Characteristics table, removed duplicate specifications.
July 2008	02.3	Lowered the maximum supply current at 85°C to match the commercial product values.
		Added automotive disclaimer.
May 2009	02.4	Correction to t_{CW}, tGW, t_{WIR} and f_{MAX} parameters in External Switching Characteristics table.
May 2009	02.5	Correction to t_{CW}, tGW and t_{WIR} parameters in External Switching Characteristics table.