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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST6
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	LVD, POR, WDT
Number of I/O	20
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 6V
Data Converters	A/D 16x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SO
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st62t25cm6

1 INTRODUCTION

The ST6215C, 25C devices are low cost members of the ST62xx 8-bit HCMOS family of microcontrollers, which is targeted at low to medium complexity applications. All ST62xx devices are based on a building block approach: a common core is surrounded by a number of on-chip peripherals.

The ST62E25C is the erasable EPROM version of the ST62T15C, T25C devices, which may be used during the development phase for the ST62T15C, T25C target devices, as well as the respective ST6215C, 25C ROM devices.

OTP and EPROM devices are functionally identical. OTP devices offer all the advantages of user programmability at low cost, which make them the ideal choice in a wide range of applications where frequent code changes, multiple code versions or last minute programmability are required.

The ROM based versions offer the same functionality, selecting the options defined in the programmable option bytes of the OTP/EPROM versions in the ROM option list (See Section 12.6 on page 97).

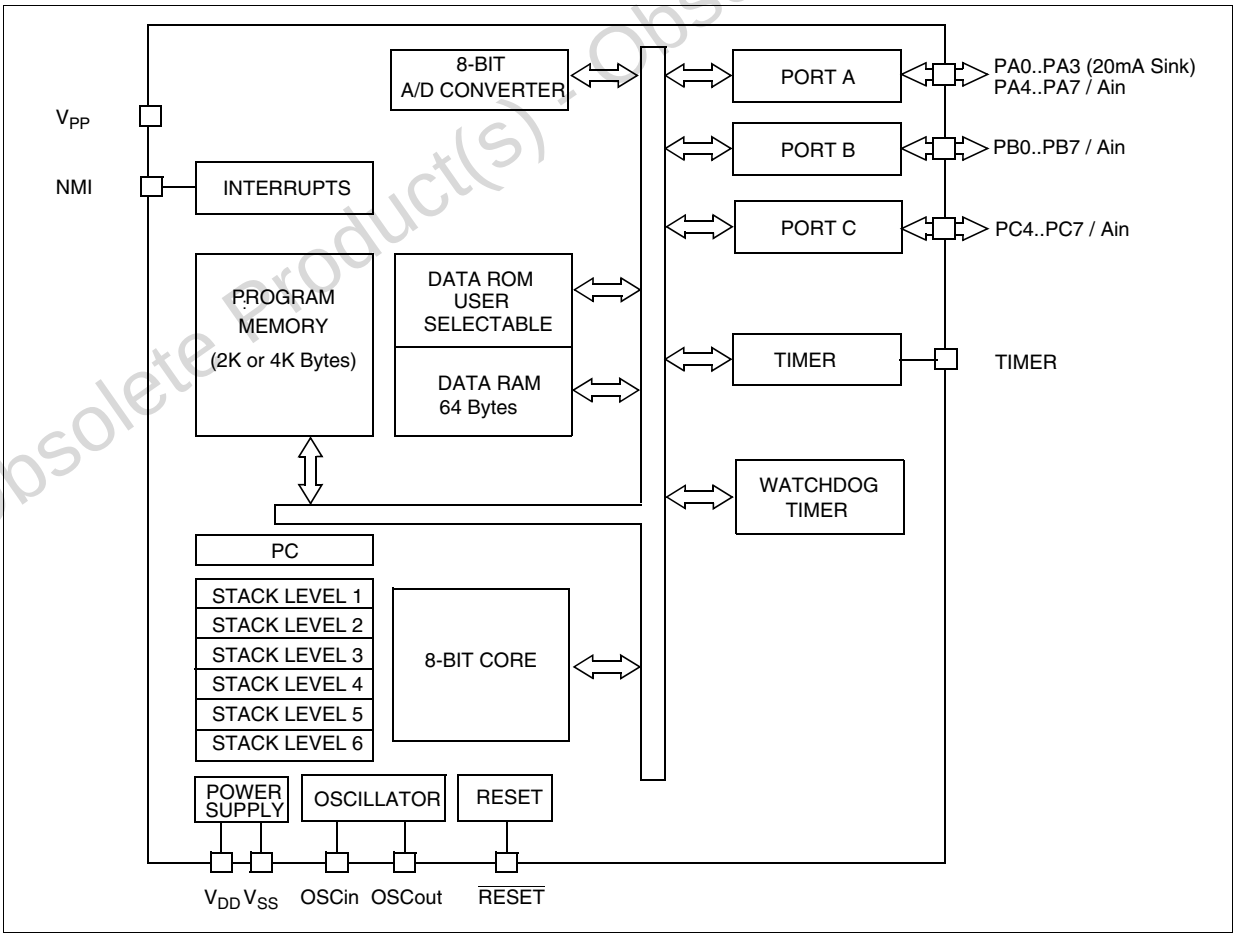
The ST62P15C/P25C are the **F**actory **A**dvanced **S**ervice **T**echnique ROM (FASTROM) versions of ST62T15C,T25C OTP devices.

They offer the same functionality as OTP devices, but they do not have to be programmed by the customer (See Section 12 on page 91).

These compact low-cost devices feature a Timer comprising an 8-bit counter with a 7-bit programmable prescaler, an 8-bit A/D Converter with 16 analog inputs and a Digital Watchdog timer, making them well suited for a wide range of automotive, appliance and industrial applications.

For easy reference, all parametric data is located in Section 11 on page 63.

Figure 1. Block Diagram



2 PIN DESCRIPTION

Figure 2. 28-Pin Package Pinout

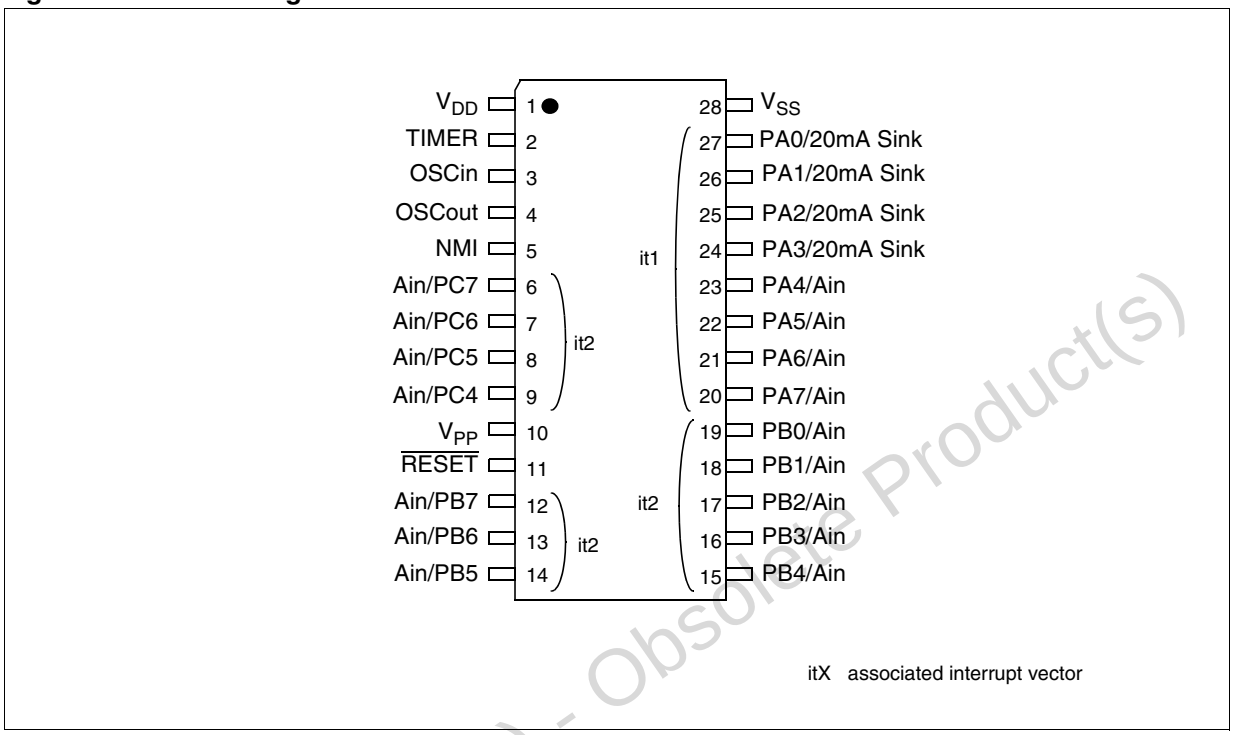
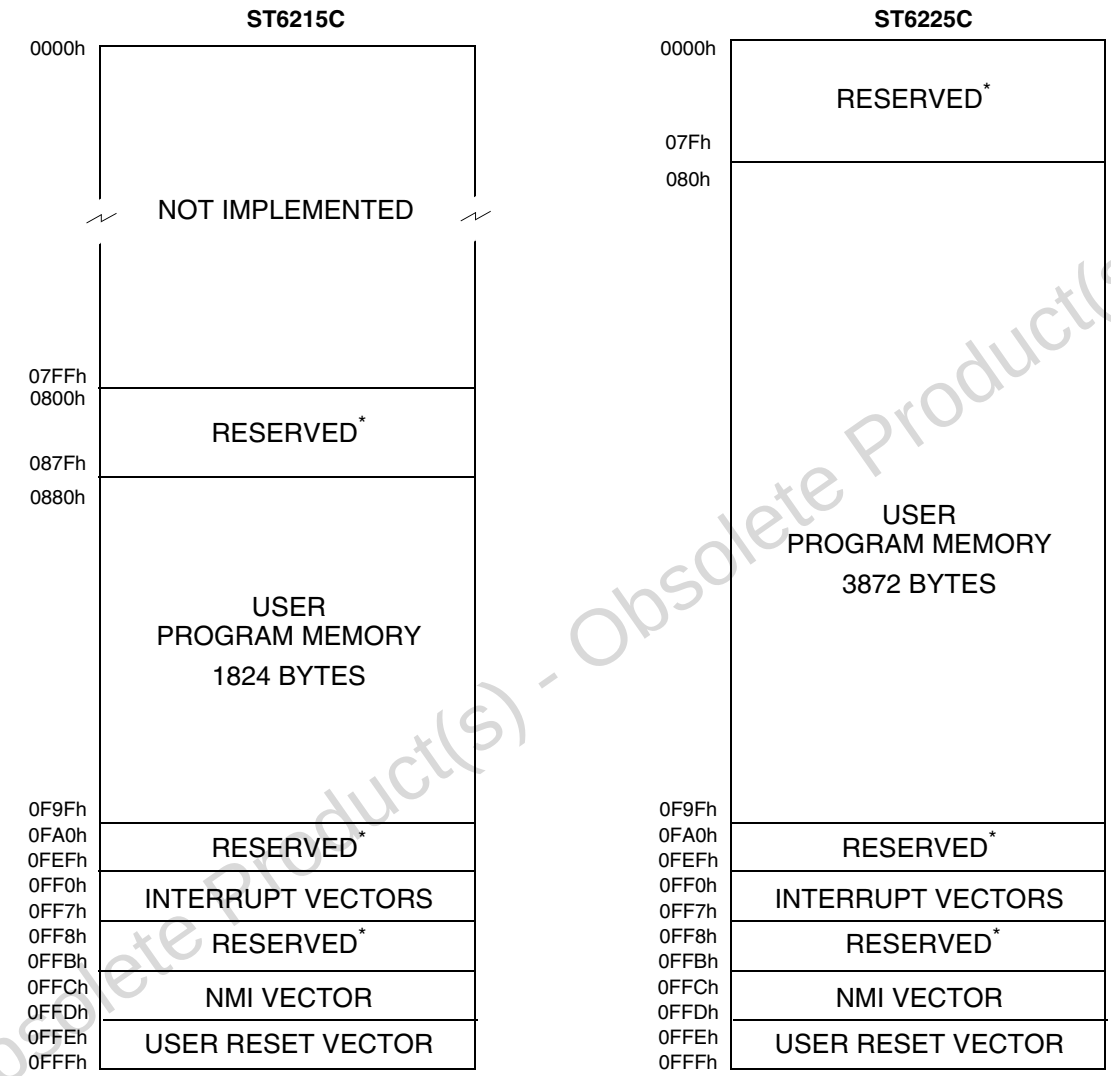


Table 1. Device Pin Description

Pin n°	Pin Name	Type	Main Function (after Reset)	Alternate Function
1	V_{DD}	S	Main power supply	
2	TIMER	I/O	Timer input or output	
3	OSCin	I	External clock input or resonator oscillator inverter input	
4	OSCout	O	Resonator oscillator inverter output or resistor input for RC oscillator	
5	NMI	I	Non maskable interrupt (falling edge sensitive)	
6	PC7/Ain	I/O	Pin C7 (IPU)	Analog input
7	PC6/Ain	I/O	Pin C6 (IPU)	Analog input
8	PC5/Ain	I/O	Pin C5 (IPU)	Analog input
9	PC4/Ain	I/O	Pin C4 (IPU)	Analog input
10	V_{PP}		Must be held at Vss for normal operation, if a 12.5V level is applied to the pin during the reset phase, the device enters EPROM programming mode.	
11	$\overline{\text{RESET}}$	I/O	Top priority non maskable interrupt (active low)	
12	PB7/Ain	I/O	Pin B7 (IPU)	Analog input
13	PB6/Ain	I/O	Pin B6 (IPU)	Analog input

MEMORY MAP (Cont'd)

Figure 4. Program Memory Map



(*) Reserved areas should be filled with 0FFh

RESET (Cont'd)

5.3.3 RESET Pin

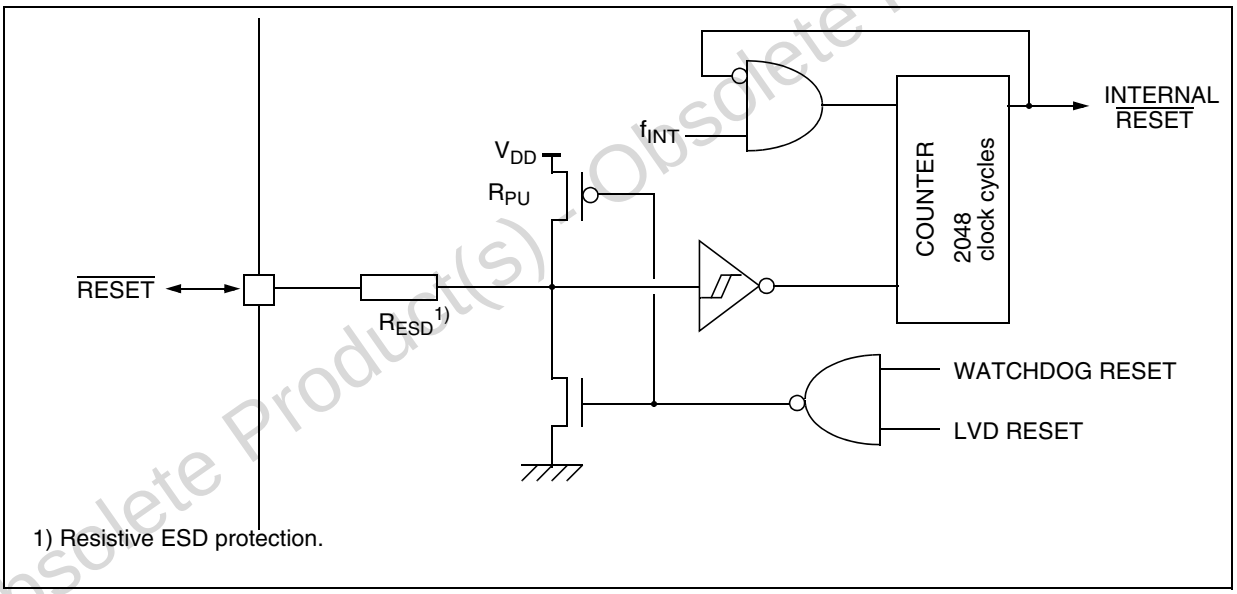
The RESET pin may be connected to a device on the application board in order to reset the MCU if required. The RESET pin may be pulled low in RUN, WAIT or STOP mode. This input can be used to reset the internal state of the MCU and ensure it starts-up correctly. The pin, which is connected to an internal pull-up, is active low and features a Schmitt trigger input. A delay (2048 clock cycles) added to the external signal ensures that even short pulses on the RESET pin are accepted as valid, provided V_{DD} has completed its rising phase and that the oscillator is running correctly (normal RUN or WAIT modes). The MCU is kept in the Reset state as long as the RESET pin is held low.

If the RESET pin is grounded while the MCU is in RUN or WAIT modes, processing of the user program is stopped (RUN mode only), the I/O ports are configured as inputs with pull-up resistors and the main oscillator is restarted. When the level on the RESET pin then goes high, the initialization sequence is executed at the end of the internal delay period.

If the RESET pin is grounded while the MCU is in STOP mode, the oscillator starts up and all the I/O ports are configured as inputs with pull-up resistors. When the RESET pin level then goes high, the initialization sequence is executed at the end of the internal delay period.

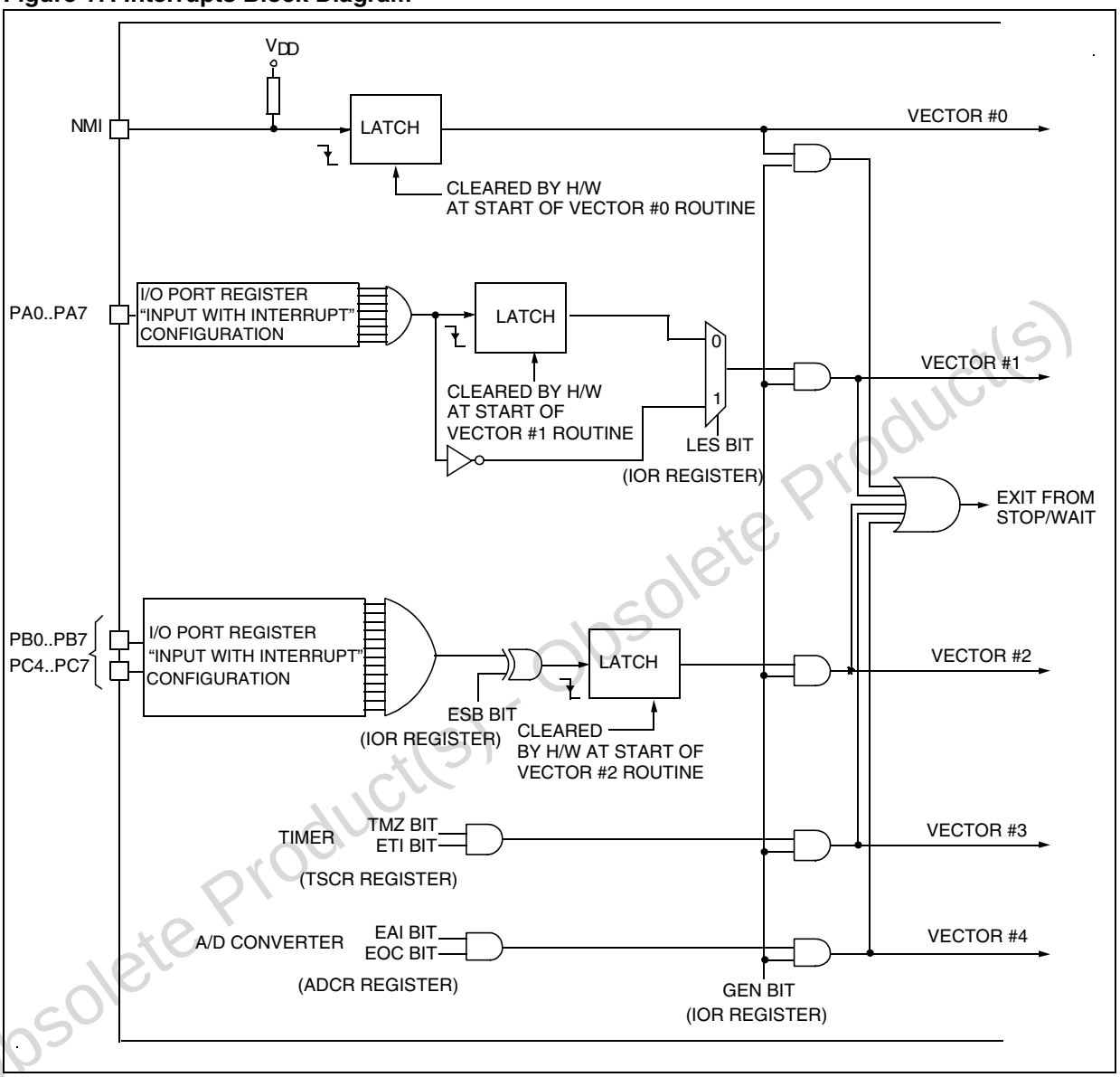
A simple external RESET circuitry is shown in Figure 15. For more details, please refer to the application note AN669.

Figure 14. Reset Block Diagram



1) Resistive ESD protection.

Figure 17. Interrupts Block Diagram



7.4 NOTES RELATED TO WAIT AND STOP MODES

7.4.1 Exit from Wait and Stop Modes

7.4.1.1 NMI Interrupt

It should be noted that when the GEN bit in the IOR register is low (interrupts disabled), the NMI interrupt is active but cannot cause a wake up from STOP/WAIT modes.

7.4.1.2 Restart Sequence

When the MCU exits from WAIT or STOP mode, it should be noted that the restart sequence depends on the original state of the MCU (normal, interrupt or non-maskable interrupt mode) prior to entering WAIT or STOP mode, as well as on the interrupt type.

Normal Mode. If the MCU was in the main routine when the WAIT or STOP instruction was executed, exit from Stop or Wait mode will occur as soon as an interrupt occurs; the related interrupt routine is executed and, on completion, the instruction which follows the STOP or WAIT instruction is then executed, providing no other interrupts are pending.

Non Maskable Interrupt Mode. If the STOP or WAIT instruction has been executed during execution of the non-maskable interrupt routine, the MCU exits from Stop or Wait mode as soon as an interrupt occurs: the instruction which follows the STOP or WAIT instruction is executed, and the MCU remains in non-maskable interrupt mode, even if another interrupt has been generated.

Normal Interrupt Mode. If the MCU was in interrupt mode before the STOP or WAIT instruction was executed, it exits from STOP or WAIT mode as soon as an interrupt occurs. Nevertheless, two cases must be considered:

– If the interrupt is a normal one, the interrupt routine in which the WAIT or STOP mode was entered will be completed, starting with the execution of the instruction which follows the STOP or the WAIT instruction, and the MCU is still in interrupt mode. At the end of this routine pending interrupts will be serviced according to their priority.

– In the event of a non-maskable interrupt, the non-maskable interrupt service routine is processed first, then the routine in which the WAIT or STOP mode was entered will be completed by executing the instruction following the STOP or WAIT instruction. The MCU remains in normal interrupt mode.

7.4.2 Recommended MCU Configuration

For lowest power consumption during RUN or WAIT modes, the user software must configure the MCU as follows:

– Configure unused I/Os as output push-pull low mode

– Place all peripherals in their power down modes before entering STOP mode

– Select the Low Frequency Auxiliary Oscillator (provided this runs at a lower frequency than the main oscillator).

The WAIT and STOP instructions are not executed if an enabled interrupt request is pending.

8 I/O PORTS

8.1 INTRODUCTION

Each I/O port contains up to 8 pins. Each pin can be programmed independently as digital input (with or without pull-up and interrupt generation), digital output (open drain, push-pull) or analog input (when available).

The I/O pins can be used in either standard or alternate function mode.

Standard I/O mode is used for:

– Transfer of data through digital inputs and outputs (on specific pins):

– External interrupt generation

Alternate function mode is used for:

– Alternate signal input/output for the on-chip peripherals

The generic I/O block diagram is shown in Figure 23.

8.2 FUNCTIONAL DESCRIPTION

Each port is associated with 3 registers located in Data space:

– Data Register (DR)

– Data Direction Register (DDR)

– Option Register (OR)

Each I/O pin may be programmed using the corresponding register bits in the DDR, DR and OR registers: bit x corresponding to pin x of the port. Table 8 illustrates the various port configurations which can be selected by user software.

During MCU initialization, all I/O registers are cleared and the input mode with pull-up and no interrupt generation is selected for all the pins, thus avoiding pin conflicts.

8.2.1 Digital Input Modes

The input configuration is selected by clearing the corresponding DDR register bit.

In this case, reading the DR register returns the digital value applied to the external I/O pin.

Different input modes can be selected by software through the DR and OR registers, see Table 8.

External Interrupt Function

All input lines can be individually connected by software to the interrupt system by programming the OR and DR registers accordingly. The interrupt trigger modes (falling edge, rising edge and low level) can be configured by software for each port as described in the Interrupt section.

8.2.2 Analog Inputs

Some pins can be configured as analog inputs by programming the OR and DR registers accordingly, see Table 8. These analog inputs are connected to the on-chip 8-bit Analog to Digital Converter.

Caution: ONLY ONE pin should be programmed as an analog input at any time, since by selecting more than one input simultaneously their pins will be effectively shorted.

8.2.3 Output Modes

The output configuration is selected by setting the corresponding DDR register bit. In this case, writing to the DR register applies this digital value to the I/O pin through the latch. Then, reading the DR register returns the previously stored value.

Two different output modes can be selected by software through the OR register: push-pull and open-drain.

DR register value and output pin status:

DR	Push-pull	Open-drain
0	V_{SS}	V_{SS}
1	V_{DD}	Floating

Note: The open drain setting is not a true open drain. This means it has the same structure as the push-pull setting but the P-buffer is deactivated. To avoid damaging the device, please respect the V_{OUT} absolute maximum rating described in the Electrical Characteristics section.

8.2.4 Alternate Functions

When an on-chip peripheral is configured to use a pin, the alternate function (timer input/output...) is not systematically selected but has to be configured through the DDR, OR and DR registers. Refer to the chapter describing the peripheral for more details.

I/O PORTS (Cont'd)

Figure 23. I/O Port Block Diagram

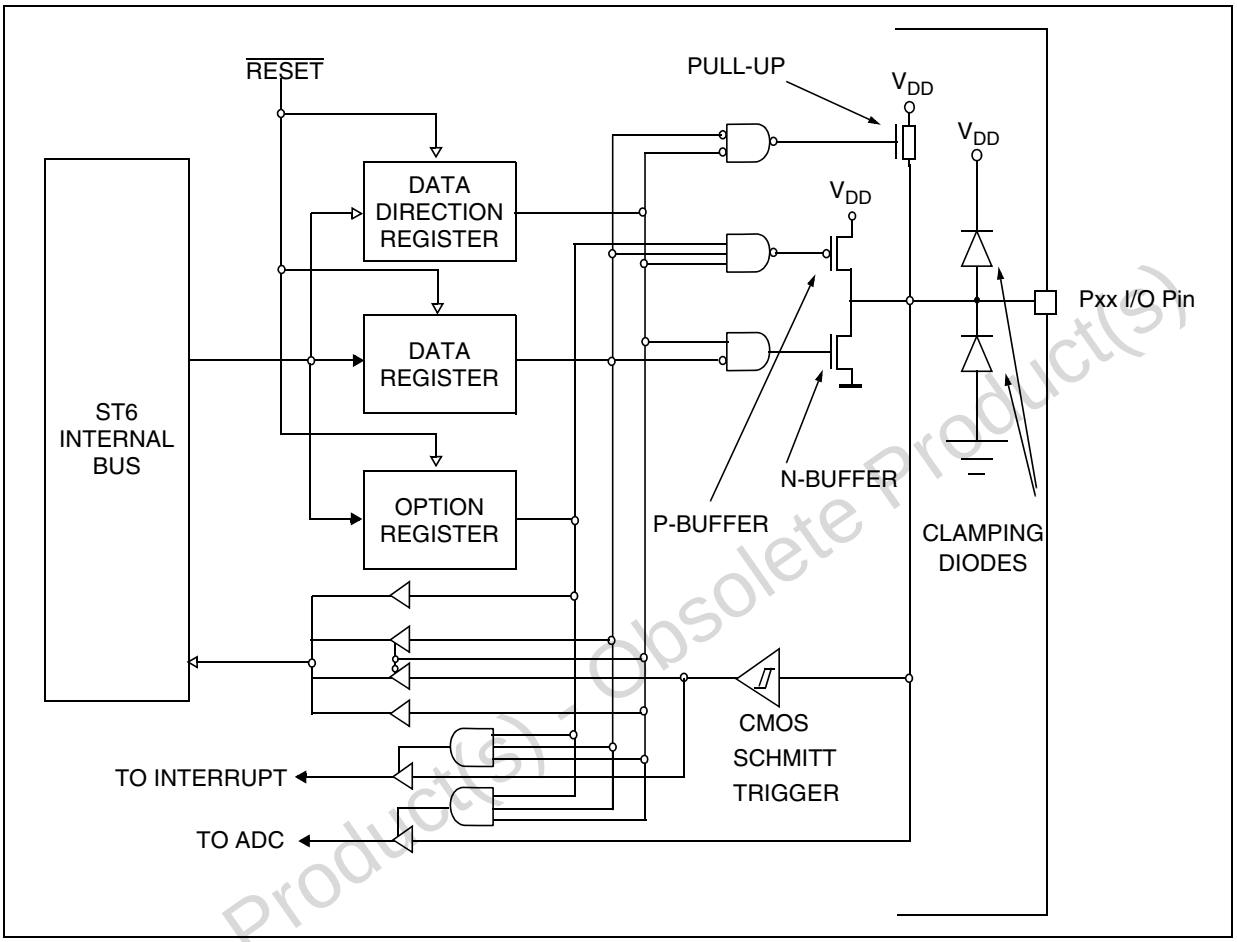


Table 8. I/O Port Configurations

DDR	OR	DR	Mode	Option
0	0	0	Input	With pull-up, no interrupt
0	0	1	Input	No pull-up, no interrupt
0	1	0	Input	With pull-up and with interrupt
0	1	1	Input	Analog input (when available)
1	0	x	Output	Open-drain output (20mA sink when available)
1	1	x	Output	Push-pull output (20mA sink when available)

Note: x = Don't care

9.3 A/D CONVERTER (ADC)

9.3.1 Introduction

The on-chip Analog to Digital Converter (ADC) peripheral is a 8-bit, successive approximation converter. This peripheral has multiplexed analog input channels (refer to device pin out description) that allow the peripheral to convert the analog voltage levels from different sources.

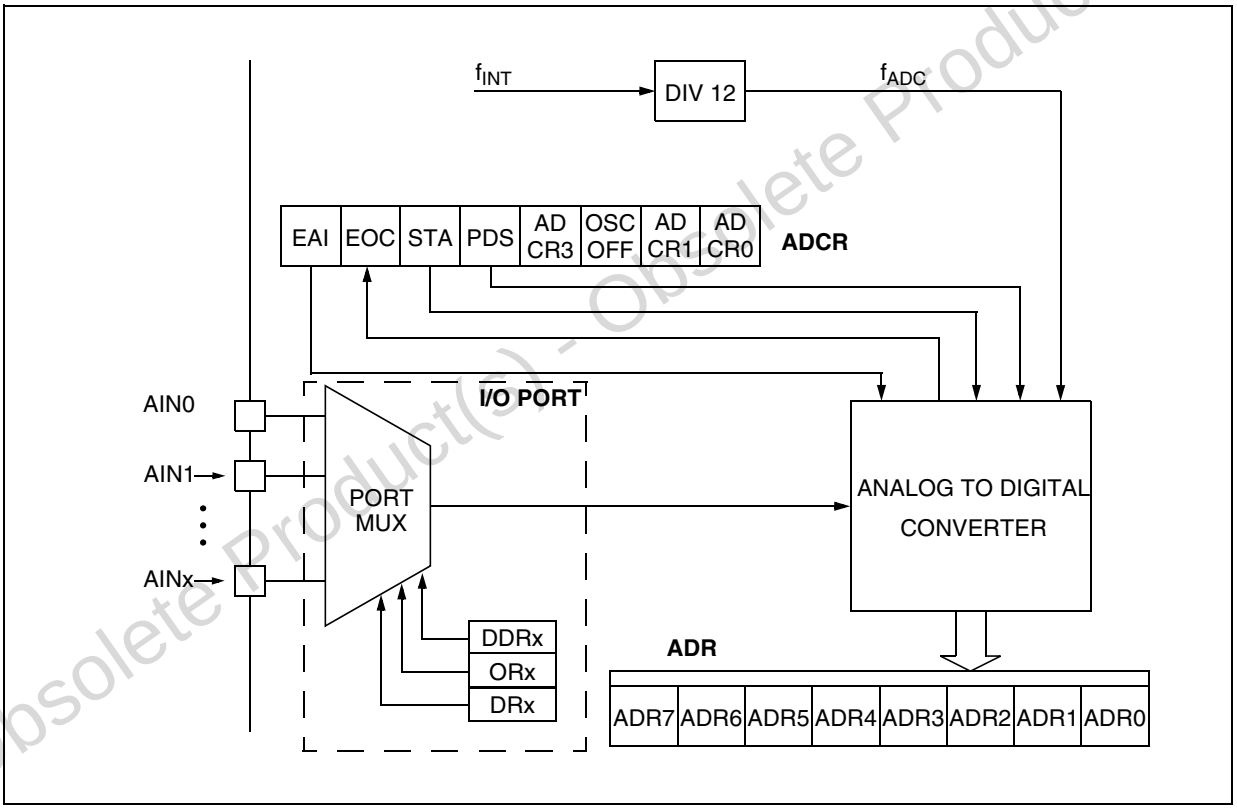
The result of the conversion is stored in a 8-bit Data Register. The A/D converter is controlled through a Control Register.

9.3.2 Main Features

- 8-bit conversion
- Multiplexed analog input channels
- Linear successive approximation
- Data register (DR) which contains the results
- End of Conversion flag
- On/Off bit (to reduce consumption)
- Typical conversion time 70 µs (with an 8 MHz crystal)

The block diagram is shown in Figure 34.

Figure 34. ADC Block Diagram



A/D CONVERTER (Cont'd)

9.3.4 Recommendations

The following six notes provide additional information on using the A/D converter.

1.The A/D converter does not feature a sample and hold circuit. The analog voltage to be measured should therefore be stable during the entire conversion cycle. Voltage variation should not exceed ±1/2 LSB for optimum conversion accuracy. A low pass filter may be used at the analog input pins to reduce input voltage variation during conversion.

2. When selected as an analog channel, the input pin is internally connected to a capacitor C_{ad} of typically 9pF. For maximum accuracy, this capacitor must be fully charged at the beginning of conversion. In the worst case, conversion starts one instruction (6.5 µs) after the channel has been selected. The impedance of the analog voltage source (ASI) in worst case conditions, is calculated using the following formula:

$$6.5\mu s = 9 \times C_{ad} \times ASI$$

(capacitor charged to over 99.9%), i.e. 30 kΩ including a 50% guardband.
The ASI can be higher if C_{ad} has been charged for a longer period by adding instructions before the start of conversion (adding more than 26 CPU cycles is pointless).

3. Since the ADC is on the same chip as the microprocessor, the user should not switch heavily loaded output signals during conversion, if high precision is required. Such switching will affect the supply voltages used as analog references.

4. Conversion accuracy depends on the quality of the power supplies (V_{DD} and V_{SS}). The user must take special care to ensure a well regulated reference voltage is present on the V_{DD} and V_{SS} pins (power supply voltage variations must be less than 0.1V/ms). This implies, in particular, that a suitable decoupling capacitor is used at the V_{DD} pin.
The converter resolution is given by:

$$\frac{V_{DD} - V_{SS}}{256}$$

The Input voltage (Ain) which is to be converted must be constant for 1µs before conversion and remain constant during conversion.

5. Conversion resolution can be improved if the power supply voltage (V_{DD}) to the microcontroller is lowered.

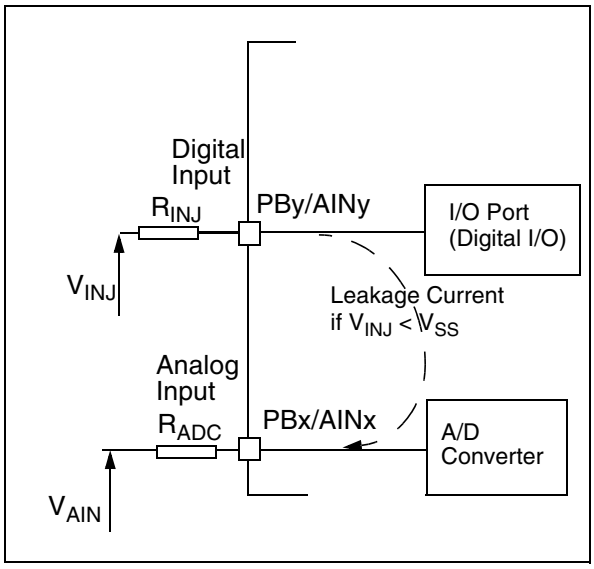
6. In order to optimize the conversion resolution, the user can configure the microcontroller in WAIT mode, because this mode minimises noise disturbances and power supply variations due to output switching. Nevertheless, the WAIT instruction should be executed as soon as possible after the beginning of the conversion, because execution of the WAIT instruction may cause a small variation of the V_{DD} voltage. The negative effect of this variation is minimized at the beginning of the conversion when the converter is less sensitive, rather than at the end of conversion, when the least significant bits are determined.
The best configuration, from an accuracy standpoint, is WAIT mode with the Timer stopped. In this case only the ADC peripheral and the oscillator are then still working. The MCU must be woken up from WAIT mode by the ADC interrupt at the end of the conversion. The microcontroller can also be woken up by the Timer interrupt, but this means the Timer must be running and the resulting noise could affect conversion accuracy.

Caution: When an I/O pin is used as an analog input, A/D conversion accuracy will be impaired if negative current injections ($V_{INJ} < V_{SS}$) occur from adjacent I/O pins with analog input capability. Refer to Figure 35. To avoid this:

– Use another I/O port located further away from the analog pin, preferably not multiplexed on the A/D converter

– Increase the input resistance $R_{IN\,J}$ (to reduce the current injections) and reduce R_{ADC} (to preserve conversion accuracy).

Figure 35. Leakage from Digital Inputs



INSTRUCTION SET (Cont'd)

Arithmetic and Logic. These instructions are used to perform arithmetic calculations and logic operations. In AND, ADD, CP, SUB instructions one operand is always the accumulator while, depending on the addressing mode, the other can be either a data space memory location or an immediate value. In CLR, DEC, INC instructions the operand can be any of the 256 data space addresses. In COM, RLC, SLA the operand is always the accumulator.

Table 17. Arithmetic & Logic Instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
ADD A, (X)	Indirect	1	4	Δ	Δ
ADD A, (Y)	Indirect	1	4	Δ	Δ
ADD A, rr	Direct	2	4	Δ	Δ
ADDI A, #N	Immediate	2	4	Δ	Δ
AND A, (X)	Indirect	1	4	Δ	Δ
AND A, (Y)	Indirect	1	4	Δ	Δ
AND A, rr	Direct	2	4	Δ	Δ
ANDI A, #N	Immediate	2	4	Δ	Δ
CLR A	Short Direct	2	4	Δ	Δ
CLR r	Direct	3	4	*	*
COM A	Inherent	1	4	Δ	Δ
CP A, (X)	Indirect	1	4	Δ	Δ
CP A, (Y)	Indirect	1	4	Δ	Δ
CP A, rr	Direct	2	4	Δ	Δ
CPI A, #N	Immediate	2	4	Δ	Δ
DEC X	Short Direct	1	4	Δ	*
DEC Y	Short Direct	1	4	Δ	*
DEC V	Short Direct	1	4	Δ	*
DEC W	Short Direct	1	4	Δ	*
DEC A	Direct	2	4	Δ	*
DEC rr	Direct	2	4	Δ	*
DEC (X)	Indirect	1	4	Δ	*
DEC (Y)	Indirect	1	4	Δ	*
INC X	Short Direct	1	4	Δ	*
INC Y	Short Direct	1	4	Δ	*
INC V	Short Direct	1	4	Δ	*
INC W	Short Direct	1	4	Δ	*
INC A	Direct	2	4	Δ	*
INC rr	Direct	2	4	Δ	*
INC (X)	Indirect	1	4	Δ	*
INC (Y)	Indirect	1	4	Δ	*
RLC A	Inherent	1	4	Δ	Δ
SLA A	Inherent	2	4	Δ	Δ
SUB A, (X)	Indirect	1	4	Δ	Δ
SUB A, (Y)	Indirect	1	4	Δ	Δ
SUB A, rr	Direct	2	4	Δ	Δ
SUBI A, #N	Immediate	2	4	Δ	Δ

Notes:
X,Y Index Registers
V, W Short Direct Registers
Δ Affected
Immediate data (stored in ROM memory)
* Not Affected
rr Data space register

INSTRUCTION SET (Cont'd)

Conditional Branch. Branch instructions perform a branch in the program when the selected condition is met.

Bit Manipulation Instructions. These instructions can handle any bit in Data space memory. One group either sets or clears. The other group (see Conditional Branch) performs the bit test branch operations.

Control Instructions. Control instructions control microcontroller operations during program execution.

Jump and Call. These two instructions are used to perform long (12-bit) jumps or subroutine calls to any location in the whole program space.

Table 18. Conditional Branch Instructions

Instruction	Branch If	Bytes	Cycles	Flags	
				Z	C
JRC e	C = 1	1	2	*	*
JRNC e	C = 0	1	2	*	*
JRZ e	Z = 1	1	2	*	*
JRNZ e	Z = 0	1	2	*	*
JRR b, rr, ee	Bit = 0	3	5	*	Δ
JRS b, rr, ee	Bit = 1	3	5	*	Δ

Notes:
b 3-bit address
e 5 bit signed displacement in the range -15 to +16
ee 8 bit signed displacement in the range -126 to +129
rr Data space register
Δ Affected. The tested bit is shifted into carry.
* Not Affected

Table 19. Bit Manipulation Instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
SET b,rr	Bit Direct	2	4	*	*
RES b,rr	Bit Direct	2	4	*	*

Notes:
b 3-bit address
rr Data space register
* Not Affected
Bit Manipulation Instructions should not be used on Port Data Registers and any registers with read only and/or write only bits (see I/O port chapter)

Table 20. Control Instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
NOP	Inherent	1	2	*	*
RET	Inherent	1	2	*	*
RETI	Inherent	1	2	Δ	Δ
STOP (1)	Inherent	1	2	*	*
WAIT	Inherent	1	2	*	*

Notes:
1. This instruction is deactivated and a WAIT is automatically executed instead of a STOP if the watchdog function is selected.
Δ Affected
*Not Affected

Table 21. Jump & Call Instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
CALL abc	Extended	2	4	*	*
JP abc	Extended	2	4	*	*

Notes:
abc 12-bit address
* Not Affected

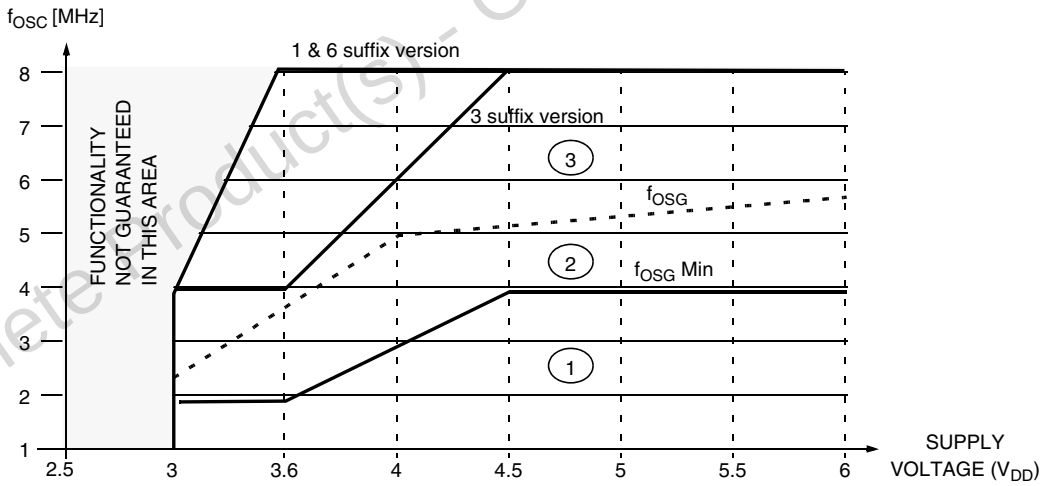
11.3 OPERATING CONDITIONS

11.3.1 General Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Supply voltage	see Figure 38	3.0	6	V
f_{OSC}	Oscillator frequency	V_{DD}=3.0V, 1 & 6 Suffix	0 [1]	4	MHz
		V_{DD}=3.0V, 3 Suffix	0 [1]	4	
		V_{DD}=3.6V, 1 & 6Suffix	0 [1]	8	
		V_{DD}=3.6V, 3 Suffix	0 [1]	4	
V_{DD}	Operating Supply Voltage	f_{OSC}=4MHz, 1 & 6 Suffix	3.0	6.0	V
		f_{OSC}=4MHz, 3 Suffix	3.0	6.0	
		f_{OSC}=8MHz, 1 & 6 Suffix	3.6	6.0	
		f_{OSC}=8MHz, 3 Suffix	4.5	6.0	
T_A	Ambient temperature range	1 Suffix Version	0	70	°C
		6 Suffix Version	-40	85	
		3 Suffix Version	-40	125	

Notes:
1. An oscillator frequency above 1.2MHz is recommended for reliable A/D results.
2. Operating conditions with T_A=-40 to +125°C.

Figure 38. f_{OSC} Maximum Operating Frequency Versus V_{DD} Supply Voltage for OTP & ROM devices



1. In this area, operation is guaranteed at the quartz crystal frequency.
2. When the OSG is disabled, operation in this area is guaranteed at the crystal frequency. When the OSG is enabled, operation in this area is guaranteed at a frequency of at least f_{OSG} Min.
3. When the OSG is disabled, operation in this area is guaranteed at the quartz crystal frequency. When the OSG is enabled, access to this area is prevented. The internal frequency is kept at f_{OSG}.

SUPPLY CURRENT CHARACTERISTICS (Cont'd)

11.4.3 STOP Mode

Symbol	Parameter	Conditions	Typ [1]	Max	Unit
I_{DD}	Supply current in STOP mode [2] (see Figure 47 & Figure 48)	OTP devices	0.3	10 [3] 20 [4]	µA
		ROM devices	0.1	2 [3] 20 [4]	

Notes:

1. Typical data are based on V_{DD}=5.0V at T_A=25°C.
2. All I/O pins in input with pull-up mode (no load), all peripherals in reset state, OSG and LVD disabled, option bytes programmed to 00H. Data based on characterization results, tested in production at V_{DD} max. and f_{CPU} max.
3. Maximum STOP consumption for -40°C<Ta<90°C
4. Maximum STOP consumption for -40°C<Ta<125°C

Figure 47. Typical I_{DD} in STOP vs Temperature for OTP devices

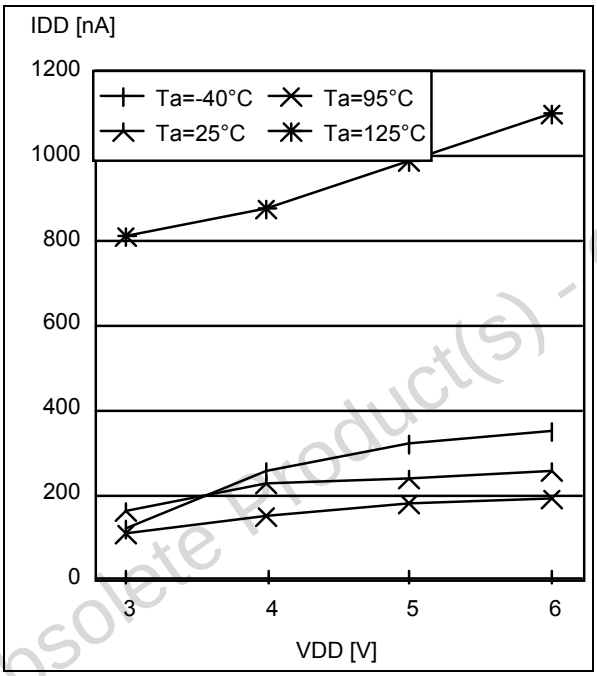
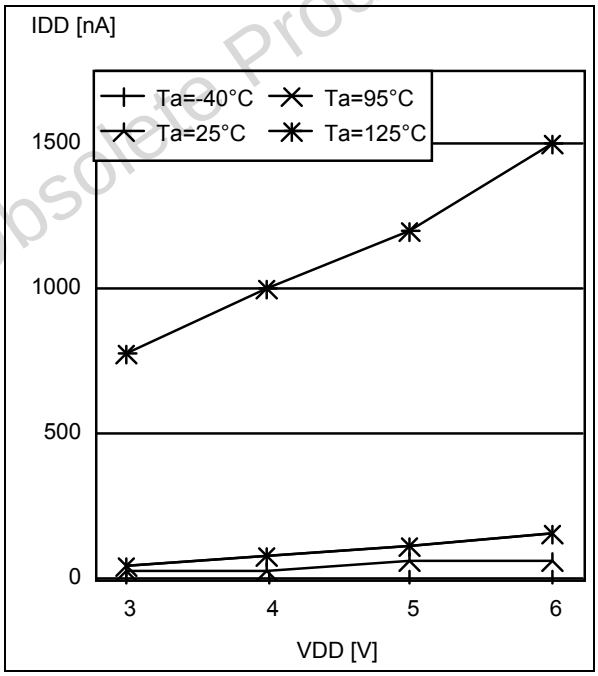


Figure 48. Typical I_{DD} in STOP vs Temperature for ROM devices



CLOCK AND TIMING CHARACTERISTICS (Cont'd)

11.5.3 Crystal and Ceramic Resonator Oscillators

The ST6 internal clock can be supplied with several different Crystal/Ceramic resonator oscillators. Only parallel resonant crystals can be used. All the information given in this paragraph are based on characterization results with specified typical external components. Refer to the crystal/ceramic resonator manufacturer for more details (frequency, package, accuracy...).

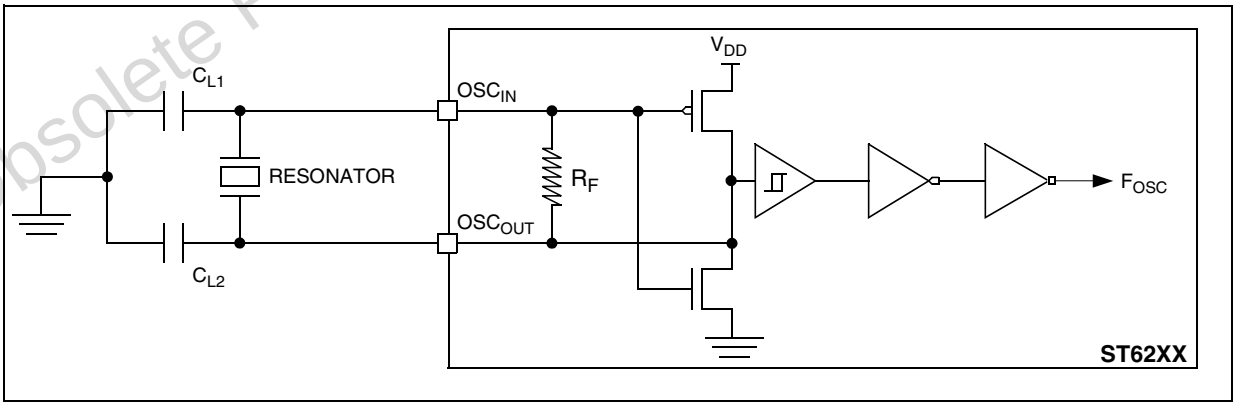
Symbol	Parameter	Conditions	Typ	Unit
R_F	Feedback resistor		3	MΩ
C_{L1} C_{L2}	Recommended load capacitances versus equivalent crystal or ceramic resonator frequency	f_{OSC}=32 kHz, f_{OSC}=1 MHz f_{OSC}=2 MHz f_{OSC}=4 MHz f_{OSC}=8 MHz	120 47 33 33 22	pF

Oscillator	Typical Crystal or Ceramic Resonators				C_{L1} [pF]	C_{L2} [pF]	$t_{SU(osc)}$ [ms] 1)
	Reference		Freq.	Characteristic 1)			
Ceramic	MURATA	CSB455E	455KHz	Δf_{OSC}=[±0.5KHz$_{tolerance}$,±0.3%$_{\Delta Ta}$,±0.5%$_{aging}$]	220	220	
		CSB1000J	1MHz	Δf_{OSC}=[±0.5KHz$_{tolerance}$,±0.3%$_{\Delta Ta}$,±0.5%$_{aging}$]	100	100	
		CSTCC2.00MG0H6	2MHz	Δf_{OSC}=[±0.5%$_{tolerance}$,±0.5%$_{\Delta Ta}$,±0.3%$_{aging}$]	47	47	
		CSTCC4.00MG0H6	4MHz	Δf_{OSC}=[±0.5%$_{tolerance}$,±0.3%$_{\Delta Ta}$,±0.3%$_{aging}$]	47	47	
		CSTCC8.00MG	8MHz	Δf_{OSC}=[±0.5%$_{tolerance}$,±0.3%$_{\Delta Ta}$,±0.3%$_{aging}$]	15	15	

Notes:

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. $t_{SU(OSC)}$ is the typical oscillator start-up time measured between V_{DD}=2.8V and the fetch of the first instruction (with a quick V_{DD} ramp-up from 0 to 5V (<50µs).
3. The oscillator selection can be optimized in terms of supply current using an high quality resonator with small R_S value. Refer to crystal/ceramic resonator manufacturer for more details.

Figure 50. Typical Application with a Crystal or Ceramic Resonator



EMC CHARACTERISTICS (Cont'd)

11.7.2 Absolute Electrical Sensitivity

Based on three different tests (ESD, LU and DLU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the AN1181 application note.

11.7.2.1 Electro-Static Discharge (ESD)

Electro-Static Discharges (3 positive then 3 negative pulses separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends of the number of supply pins of the device (3 parts*(n+1) supply pin). Two models are usually simulated: Human Body Model and Machine Model. This test conforms to the JESD22-A114A/A115A standard. See Figure 57 and the following test sequences.

Human Body Model Test Sequence

– C_L is loaded through S1 by the HV pulse generator.
– S1 switches position from generator to R.
– A discharge from C_L through R (body resistance) to the ST6 occurs.
– S2 must be closed 10 to 100ms after the pulse delivery period to ensure the ST6 is not left in charge state. S2 must be opened at least 10ms prior to the delivery of the next pulse.

Machine Model Test Sequence

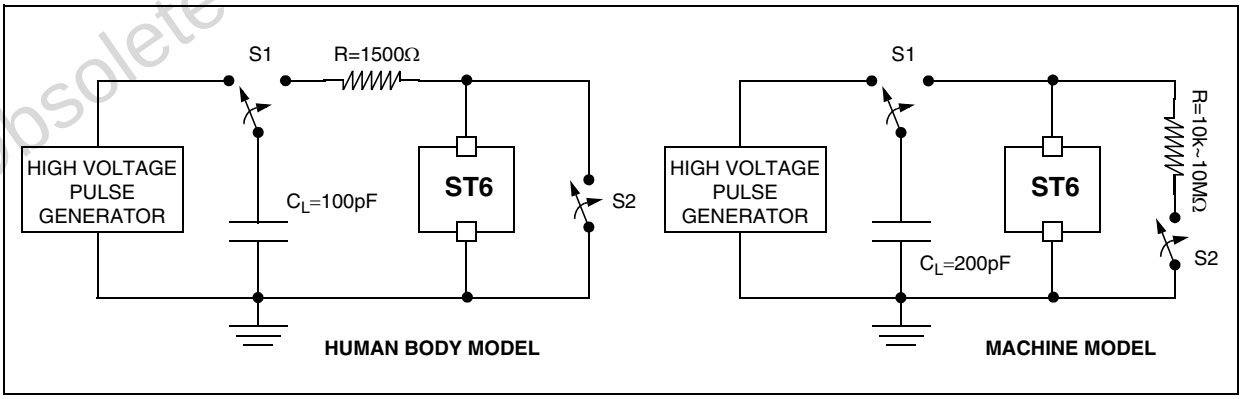
– C_L is loaded through S1 by the HV pulse generator.
– S1 switches position from generator to ST6.
– A discharge from C_L to the ST6 occurs.
– S2 must be closed 10 to 100ms after the pulse delivery period to ensure the ST6 is not left in charge state. S2 must be opened at least 10ms prior to the delivery of the next pulse.
– R (machine resistance), in series with S2, ensures a slow discharge of the ST6.

Absolute Maximum Ratings

Symbol	Ratings	Conditions	Maximum value [1]	Unit
$V_{ESD(HBM)}$	Electro-static discharge voltage (Human Body Model)	T_A=+25°C	2000	V
$V_{ESD(MM)}$	Electro-static discharge voltage (Machine Model)	T_A=+25°C	200	

Notes:
1. Data based on characterization results, not tested in production.

Figure 57. Typical Equivalent ESD Circuits



I/O PORT PIN CHARACTERISTICS (Cont'd)

Figure 65. Typical V_{OH} at V_{DD} = 5V

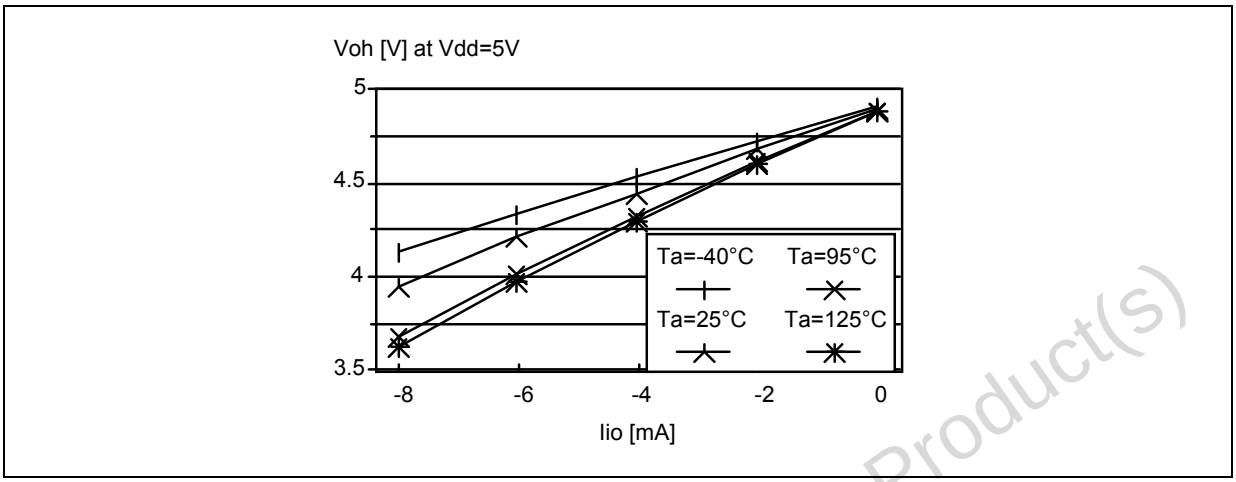


Figure 66. Typical V_{OL} vs V_{DD} (standard I/Os)

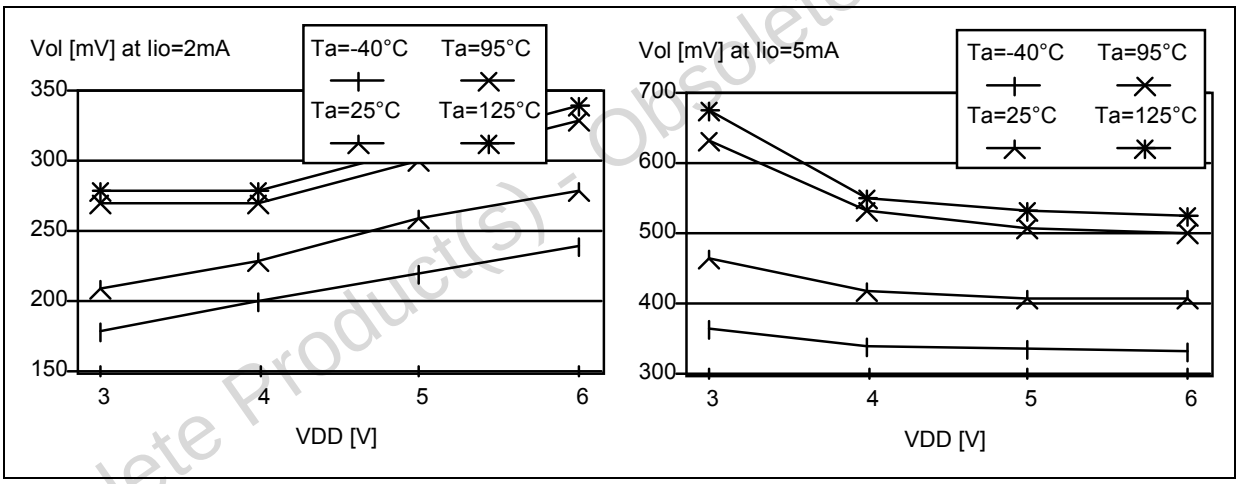
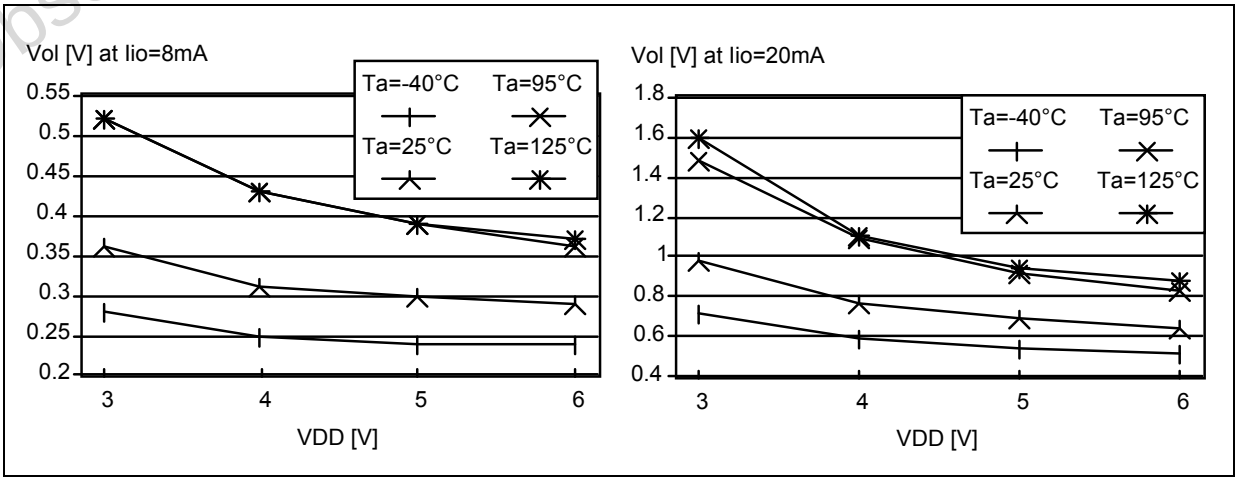


Figure 67. Typical V_{OL} vs V_{DD} (high-sink I/Os)



12.2 THERMAL CHARACTERISTICS

Symbol	Ratings	Value	Unit
R_{thJA}	Package thermal resistance (junction to ambient) DIP28 SO28 SSOP28	 55 75 110	°C/W
P_D	Power dissipation [1]	500	mW
T_{Jmax}	Maximum junction temperature [2]	150	°C

Notes:

1. The power dissipation is obtained from the formula $P_D = P_{INT} + P_{PORT}$ where P_{INT} is the chip internal power ($I_{DD}xV_{DD}$) and P_{PORT} is the port power dissipation determined by the user.
2. The average chip-junction temperature can be obtained from the formula $T_J = T_A + P_D$ x RthJA.

13 DEVELOPMENT TOOLS

STMicroelectronics offers a range of hardware and software development tools for the ST6 microcontroller family. Full details of tools available for the ST6 from third party manufacturers can be obtain from the STMicroelectronics Internet site: ➟ http://www.st.com.

Table 25. Dedicated Third Parties Development Tools

Third Party [1)]	Designation	ST Sales Type	Web site address
ACTUM	ST-REALIZER II: Graphical Schematic based Development available from STMicroelectronics.	STREALIZER-II	http://www.actum.com/
CEIBO	Low cost emulator available from CEIBO.		http://www.ceibo.com/
RAISONANCE	This tool includes in the same environment: an assembler, linker, C compiler, debugger and simulator. The assembler package (plus limited C compiler) is free and can be downloaded from raisonance web site. The full version is available both from STMicroelectronics and Raisonance.	ST6RAIS-SWC/PC	http://www.raisonance.com/
SOFTEC	High end emulator available from SOFTEC.		http://www.softecmicro.com/
	Gang programmer available from SOFTEC.		
ADVANCED EQUIPMENT	Single and gang programmers		http://www.aec.com.tw/
ADVANCED TRANSDATA			http://www.adv-transdata.com/
BP MICROSYSTEMS			http://www.bpmicro.com/
DATA I/O			http://www.data-io.com/
DATAMAN			http://www.dataman.com/
EE TOOLS			http://www.eetools.com/
ELNEC			http://www.elnec.com/
HI-LO SYSTEMS			http://www.hilosystems.com.tw/
ICE TECHNOLOGY			http://www.icetech.com/
LEAP			http://www.leap.com.tw/
LLOYD RESEARCH			http://www.lloyd-research.com/
LOGICAL DEVICES			http://www.chipprogrammers.com/
MQP ELECTRONICS			http://www.mqp.com/
NEEDHAMS ELECTRONICS			http://www.needhams.com/
STAG PROGRAMMERS			http://www.stag.co.uk/
SYSTEM GENERAL CORP			http://www.sg.com.tw
TRIBAL MICROSYSTEMS			http://www.tribalmicro.com/
XELTEK			http://www.xeltek.com/

Note 1: For latest information on third party tools, please visit our Internet site: ➟ http://www.st.com.

14 ST6 APPLICATION NOTES

IDENTIFICATION	DESCRIPTION
MOTOR CONTROL	
AN392	MICROCONTROLLER AND TRIACS ON THE 110/240V MAINS
AN414	CONTROLLING A BRUSH DC MOTOR WITH AN ST6265 MCU
AN416	SENSORLESS MOTOR DRIVE WITH THE ST62 MCU + TRIAC
AN422	IMPROVES UNIVERSAL MOTOR DRIVE
AN863	IMPROVED SENSORLESS CONTROL WITH THE ST62 MCU FOR UNIVERSAL MOTOR
BATTERY MANAGEMENT	
AN417	FROM NICD TO NIMH FAST BATTERY CHARGING
AN433	ULTRA FAST BATTERY CHARGER USING ST6210 MICROCONTROLLER
AN859	AN INTELLIGENT ONE HOUR MULTICHARGER FOR Li-Ion, NiMH and NiCd BATTERIES
HOME APPLIANCE	
AN674	MICROCONTROLLERS IN HOME APPLIANCES: A SOFT REVOLUTION
AN885	ST62 MICROCONTROLLERS DRIVE HOME APPLIANCE MOTOR TECHNOLOGY
GRAPHICAL DESIGN	
AN676	BATTERY CHARGER USING THE ST6-REALIZER
AN677	PAINLESS MICROCONTROLLER CODE BY GRAPHICAL APPLICATION DESCRIPTION
AN839	ANALOG MULTIPLE KEY DECODING USING THE ST6-REALIZER
AN840	CODED LOCK USING THE ST6-REALIZER
AN841	A CLOCK DESIGN USING THE ST6-REALIZER
AN842	7 SEGMENT DISPLAY DRIVE USING THE ST6-REALIZER
COST REDUCTION	
AN431	USING ST6 ANALOG INPUTS FOR MULTIPLE KEY DECODING
AN594	DIRECT SOFTWARE LCD DRIVE WITH ST621X AND ST626X
AN672	OPTIMIZING THE ST6 A/D CONVERTER ACCURACY
AN673	REDUCING CURRENT CONSUMPTION AT 32KHZ WITH ST62
DESIGN IMPROVEMENTS	
AN420	EXPANDING A/D RESOLUTION OF THE ST6 A/D CONVERTER
AN432	USING ST62XX I/O PORTS SAFELY
AN434	MOVEMENT DETECTOR CONCEPTS FOR NOISY ENVIRONMENTS
AN435	DESIGNING WITH MICROCONTROLLERS IN NOISY ENVIRONMENTS
AN669	SIMPLE RESET CIRCUITS FOR THE ST6
AN670	OSCILLATOR SELECTION FOR ST62
AN671	PREVENTION OF DATA CORRUPTION IN ST6 ON-CHIP EEPROM
AN911	ST6 MICRO IS EMC CHAMPION
AN975	UPGRADING FROM ST625X/6XB TO ST625X/6XC
AN1015	SOFTWARE TECHNIQUES FOR IMPROVING ST6 EMC PERFORMANCE
PERIPHERAL OPERATIONS	
AN590	PWM GENERATION WITH ST62 AUTO-RELOAD TIMER
AN591	INPUT CAPTURE WITH ST62 AUTO-RELOAD TIMER
AN592	PLL GENERATION USING THE ST62 AUTO-RELOAD TIMER
AN593	ST62 IN-CIRCUIT PROGRAMMING
AN678	LCD DRIVING WITH ST6240