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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0 |
| Core Size | 32-Bit Single-Core |
| Speed | 50MHz |
| Connectivity | SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, WDT |
| Number of I/O | 11 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 5x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 16-UFBGA, WLCSP |
| Supplier Device Package | 16-WLCSP (2.17x2.32) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1102uk-118 |

- GPIO pins can be used as edge and level sensitive interrupt sources.
- Four general purpose counter/timers with a total of one capture input and 10 match outputs.
- Programmable windowed WatchDog Timer (WDT).

- Analog peripherals:
  - 10-bit ADC with input multiplexing among five pins.
- Serial interfaces:
  - UART with fractional baud rate generation, internal FIFO, and RS-485 support.
  - One SPI controller with SSP features and with FIFO and multi-protocol capabilities (see Section 7.16).
- Clock generation:
  - 12 MHz internal RC oscillator trimmed to 1 % accuracy that can optionally be used as a system clock.
  - Programmable watchdog oscillator with a frequency range of 9.4 kHz to 2.3 MHz.
  - PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from an external clock or the internal RC oscillator.
  - Clock output function with divider that can reflect the system oscillator clock, IRC clock, CPU clock, and the Watchdog clock (LPC1104 only).
- Power control:
  - Integrated PMU (Power Management Unit) to minimize power consumption during Sleep and Deep-sleep modes.
  - Power profiles residing in boot ROM allowing to optimize performance and minimize power consumption for any given application through one simple function call.
  - Two reduced power modes: Sleep and Deep-sleep modes.
  - Processor wake-up from Deep-sleep mode via a dedicated start logic using up to six of the functional pins.
  - Power-On Reset (POR).
  - Brownout detect with up to four separate thresholds for interrupt and forced reset.
- Unique device serial number for identification.
- Single 3.3 V power supply (1.8 V to 3.6 V).
- Available as WLCSP16 package.

## 3. Applications

- Mobile devices
- Consumer peripherals
- Lighting
- 8-/16-bit applications
- Portable devices

# 4. Ordering information

**Table 1. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| LPC1102UK | WLCSP16 | wafer level chip-size package; 16 bumps; 2.17 × 2.32 × 0.6 mm | - |
| LPC1104UK | WLCSP16 | wafer level chip-size package; 16 bumps; 2.17 × 2.32 × 0.6 mm | - |

## 4.1 Ordering options

**Table 2. Ordering options**

| Type number | Flash | Total SRAM | UART RS-485 | SPI | ADC channels | Package |
|---|---|---|---|---|---|---|
| LPC1102UK | 32 kB | 8 kB | 1 | 1 | 5 | WLCSP16 |
| LPC1104UK | 32 kB | 8 kB | 1 | 1 | 5 | WLCSP16 |

# 6. Pinning information

## 6.1 Pinning

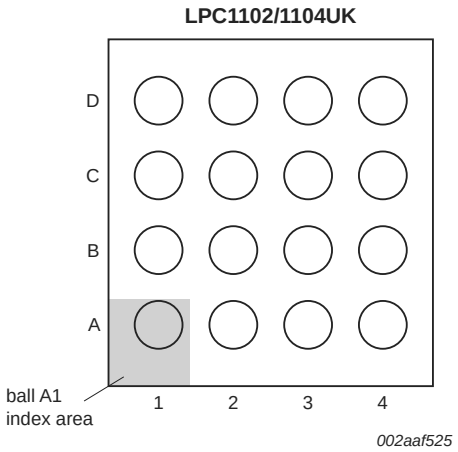



**Fig 2. Pin configuration WLCSP16 package**

## 6.2 Pin description

**Table 3. LPC1102/1104 pin description table**

| Symbol | LPC1102 | LPC1104 | Start logic input | Type | Reset state[1] | Description |
|---|---|---|---|---|---|---|
| $\overline{\text{RESET}}$/PIO0_0 | C1[2] | B2[2] | yes | I | I; PU | **$\overline{\text{RESET}}$ —** External reset input with 20 ns glitch filter. A LOW -going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. |
| | | | | I/O | - | **PIO0_0 —** General purpose digital input/output pin. |
| PIO0_1/CLKOUT/ CT32B0_MAT2 | - | C1[3] | yes | I/O | I; PU | **PIO0_1 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler. |
| | | | | O | - | **CLKOUT —** Clockout pin. |
| | | | | O | - | **CT32B0_MAT2 —** Match output 2 for 32-bit timer 0. |
| PIO0_6/SCK0 | - | A1[3] | yes | I/O | I;PU | **PIO0_6 —** General purpose digital input/output pin. |
| | | | | I/O | - | **SCK0 —** Serial clock for SPI0. |
| PIO0_8/MISO/ CT16B0_MAT0 | A2[3] | A3[3] | yes | I/O | I; PU | **PIO0_8 —** General purpose digital input/output pin. |
| | | | | I/O | - | **MISO0 —** Master In Slave Out for SPI. |
| | | | | O | - | **CT16B0_MAT0 —** Match output 0 for 16-bit timer 0. |
| PIO0_9/MOSI/ CT16B0_MAT1 | A3[3] | A4[3] | yes | I/O | I; PU | **PIO0_9 —** General purpose digital input/output pin. |
| | | | | I/O | - | **MOSI0 —** Master Out Slave In for SPI. |
| | | | | O | - | **CT16B0_MAT1 —** Match output 1 for 16-bit timer 0. |
| SWCLK/ PIO0_10/ SCK0/CT16B0_MAT2 | A4[3] | A2[3] | yes | I | I; PU | **SWCLK —** Serial wire clock. |
| | | | | I/O | - | **PIO0_10 —** General purpose digital input/output pin. |
| | | | | I/O | - | **SCK0 —** Serial clock for SPI0. |
| | | | | O | - | **CT16B0_MAT2 —** Match output 2 for 16-bit timer 0. |
| R/PIO0_11/ AD0/CT32B0_MAT3 | B4[4] | B4[4] | yes | - | I; PU | **R —** Reserved. |
| | | | | I/O | - | **PIO0_11 —** General purpose digital input/output pin. |
| | | | | I | - | **AD0 —** A/D converter, input 0. |
| | | | | I | - | **CT32B0_MAT3 —** Match output 3 for 32-bit timer 0. |
| R/PIO1_0/ AD1/CT32B1_CAP0 | B3[4] | B3[4] | yes | - | I; PU | **R —** Reserved. |
| | | | | I/O | - | **PIO1_0 —** General purpose digital input/output pin. |
| | | | | I | - | **AD1 —** A/D converter, input 1. |
| | | | | I | - | **CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1. |
| R/PIO1_1/ AD2/CT32B1_MAT0 | C4[4] | C4[4] | no | - | I; PU | **R —** Reserved. |
| | | | | I/O | - | **PIO1_1 —** General purpose digital input/output pin. |
| | | | | I | - | **AD2 —** A/D converter, input 2. |
| | | | | O | - | **CT32B1_MAT0 —** Match output 0 for 32-bit timer 1. |

- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the IRC or the dedicated watchdog oscillator (WDO). This gives a wide range of potential timing choices of watchdog operation under different power conditions.

## 7.14 Clocking and power control

### 7.14.1 Crystal oscillators

The LPC1102/1104 include two independent oscillators. These are the Internal RC oscillator (IRC) and the Watchdog oscillator. Each oscillator can be used for more than one purpose as required in a particular application.

Following reset, the LPC1102/1104 operate from the Internal RC oscillator until switched by software. This allows systems to operate without any external crystal and the bootloader code to operate at a known frequency.

See Figure 4 for an overview of the LPC1102/1104 clock generation.

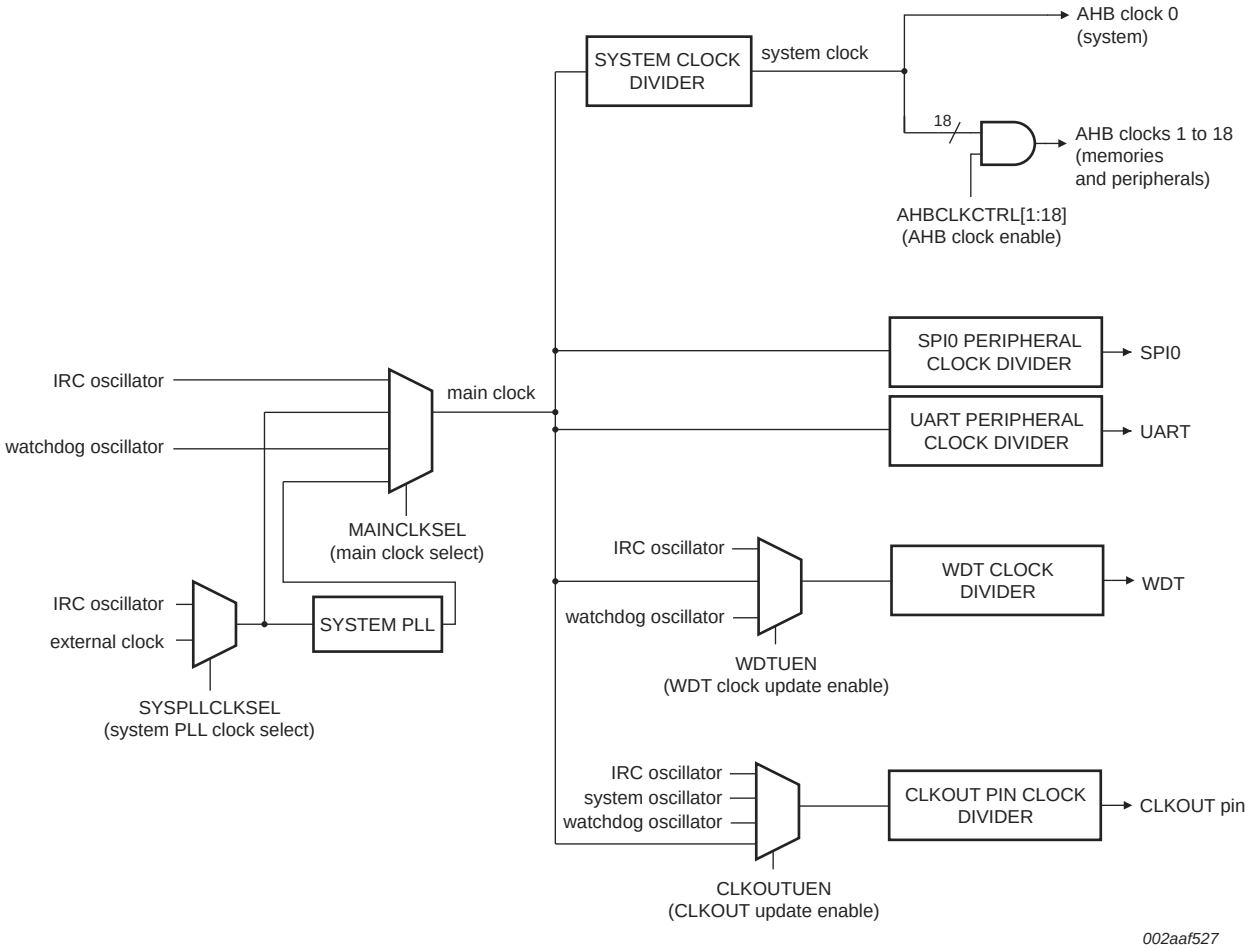



**Fig 4. LPC1102/1104 clock generation block diagram**

#### 7.14.1.1 Internal RC oscillator

The IRC may be used as the clock source for the WDT, and/or as the clock that drives the PLL and subsequently the CPU. The nominal IRC frequency is 12 MHz. The IRC is trimmed to 1 % accuracy over the entire voltage and temperature range.

Upon power-up or any chip reset, the LPC1102/1104 use the IRC as the clock source. Software may later switch to one of the other available clock sources.

#### 7.14.1.2 Watchdog oscillator

The watchdog oscillator can be used as a clock source that directly drives the CPU or the watchdog timer. The watchdog oscillator nominal frequency is programmable between 9.4 kHz to 2.3 MHz. The frequency spread over processing and temperature is ±40 %.

### 7.14.2 System PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

#### 7.14.5.3 Deep-sleep mode

In Deep-sleep mode, the chip is in Sleep mode, and in addition all analog blocks are shut down except for the watchdog oscillator and the BOD circuit, which can be configured to remain running in Deep-sleep mode to allow a reset initiated by a timer or BOD event. Deep-sleep mode allows for additional power savings.

Six of the GPIO pins (see Table 3) serve as external wake-up pins to a dedicated start logic to wake up the chip from Deep-sleep mode.

The clock source should be switched to IRC before entering Deep-sleep mode unless the watchdog oscillator remains running in Deep-sleep mode. The IRC can be switched on and off glitch-free and provides a clean clock signal after start-up.

## 7.15 System control

### 7.15.1 Start logic

The start logic connects external pins to corresponding interrupts in the NVIC. Each pin shown in Table 3 as input to the start logic has an individual interrupt in the NVIC interrupt vector table. The start logic pins can serve as external interrupt pins when the chip is running. In addition, an input signal on the start logic pins can wake up the chip from Deep-sleep mode when all clocks are shut down.

The start logic must be configured in the system configuration block and in the NVIC before being used.

### 7.15.2 Reset

Reset has four sources on the LPC1102/1104: the $\overline{\text{RESET}}$ pin, the Watchdog reset, Power-On Reset (POR), and the BrownOut Detection (BOD) circuit. In addition, there is an ARM software reset. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip reset by any source, once the operating voltage attains a usable level, starts the IRC and initializes the flash controller.

A LOW-going pulse as short as 50 ns resets the part.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

### 7.15.3 Brownout detection

The LPC1102/1104 include up to four levels for monitoring the voltage on the $V_{DD}$ pin. If this voltage falls below one of the three selected levels, the BOD asserts an interrupt signal to the NVIC. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC in order to cause a CPU interrupt; if not, software can monitor the signal by reading a dedicated status register. Four additional threshold levels can be selected to cause a forced reset of the chip.

### 7.15.4 Code security (Code Read Protection - CRP)

This feature of the LPC1102/1104 allow user to enable different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0). This mode is useful when CRP is required and flash field updates are needed but all sectors can not be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update.
3. Running an application with level CRP3 selected fully disables any access to the chip via the SWD pins.

**Remark:** The LPC1102 does not provide an ISP entry pin to be monitored at reset. For all three CRP levels, the user's application code must provide a flash update mechanism which reinvokes ISP by defining a user-selected PIOn pin for ISP entry.

**CAUTION**

If Code Read Protection of any level (CRP1, CRP2 or CRP3) is selected, no future factory testing can be performed on the device.

### 7.15.5 APB interface

The APB peripherals are located on one APB bus.

### 7.15.6 AHBLite

The AHBLite connects the CPU bus of the ARM Cortex-M0 to the flash memory, the main static RAM, and the Boot ROM.

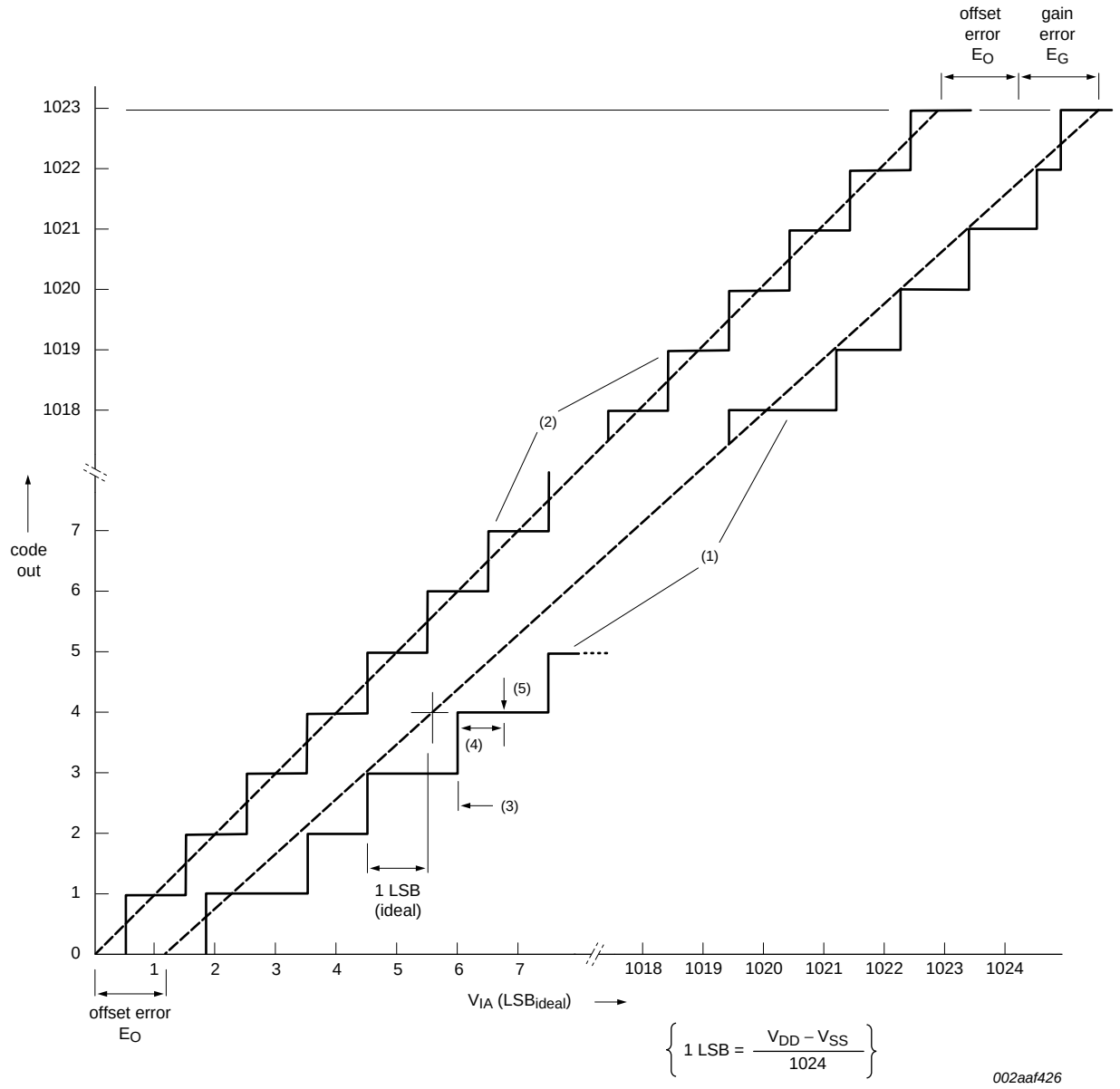
### 7.15.7 External interrupt inputs

All GPIO pins can be level or edge sensitive interrupt inputs. In addition, start logic inputs serve as external interrupts (see Section 7.15.1).

## 7.16 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M0. Serial wire debug with four breakpoints and two watchpoints is supported.

**Remark:** Care must be taken when using the SPI because the SPI clock SCK and the serial wire debug clock SWCLK share the same pin on the WLCSP16 package. Once the SPI is enabled, the serial wire debugger is no longer available (LPC1102 only).




(1) Example of an actual transfer curve.

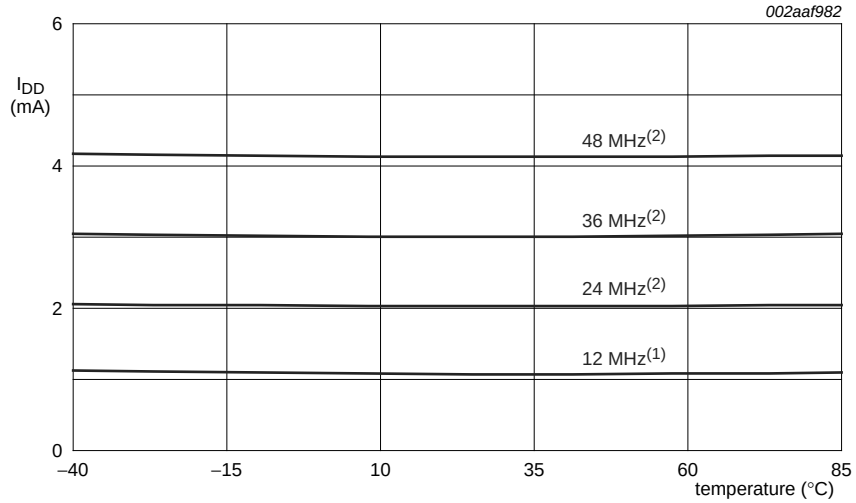
(2) The ideal transfer curve.

(3) Differential linearity error ($E_D$).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

**Fig 5. ADC characteristics**

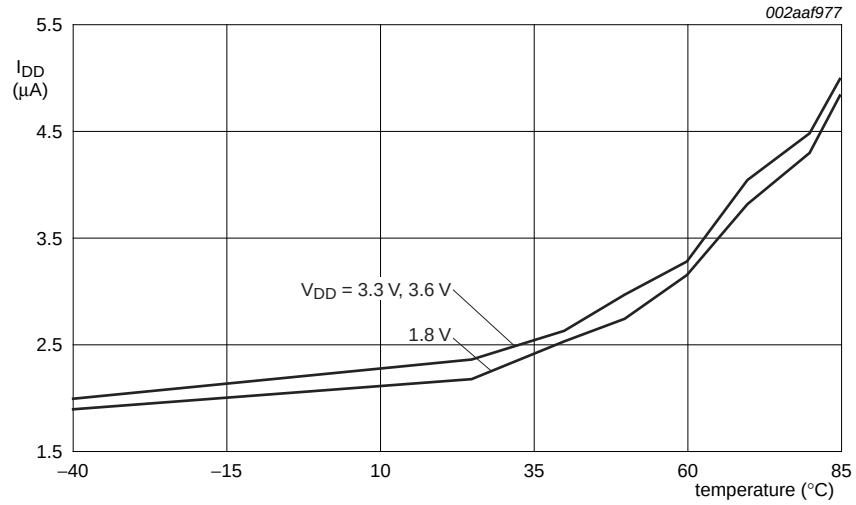



Conditions: $V_{DD}$ = 3.3 V; sleep mode entered from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL= 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

(1) System PLL disabled; IRC enabled.

(2) System PLL enabled; IRC disabled.

**Fig 8. Sleep mode: Typical supply current $I_{DD}$ versus temperature for different system clock frequencies**

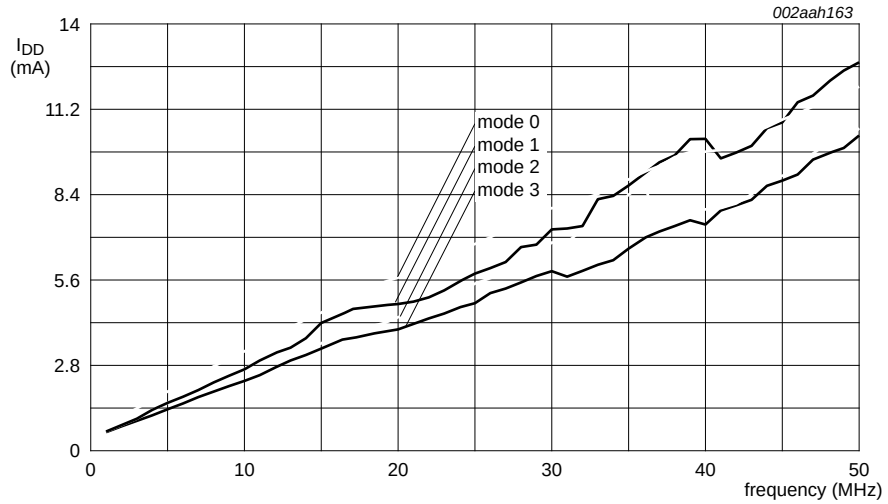



Conditions: BOD disabled; all oscillators and analog blocks disabled in the PDSLEEPCFG register (PDSLEEPCFG = 0x0000 18FF).

**Remark:** Before entering deep-sleep mode, you must write a 0 to bit 4 and bit 5 of the GPIO0DATA register at location 0x5000 3FFC and a 1 to bit 4 and bit 5 of the GPIO0DIR register at location 0x5000 8000.

**Fig 9. Deep-sleep mode: Typical supply current $I_{DD}$ versus temperature for different supply voltages $V_{DD}$**

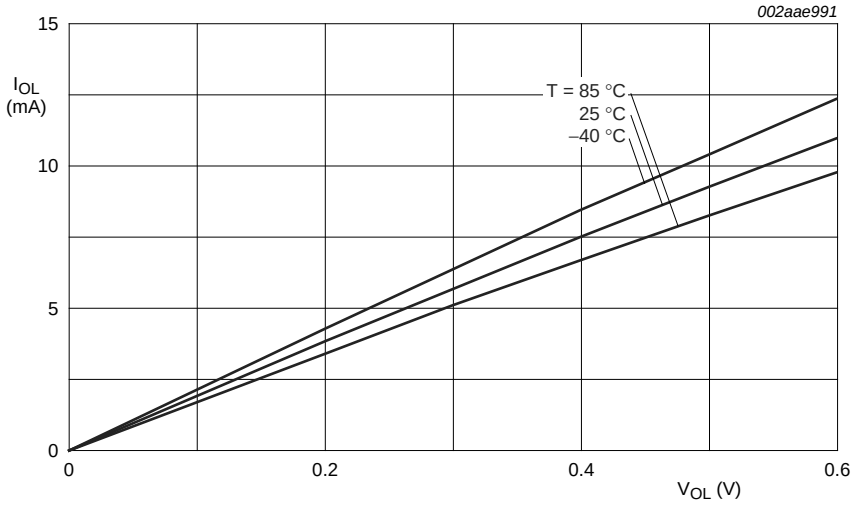
## 9.3 CoreMark data




External signal generator providing 1 MHz to 20 MHz signal drives the XTALIN input; when testing 1 MHz to 19 MHz the system PLL is OFF, SYSAHBCLKDIV = 1; when testing 20 MHz to 50 MHz the system PLL is configured so that SYSAHBCLKDIV = 1.

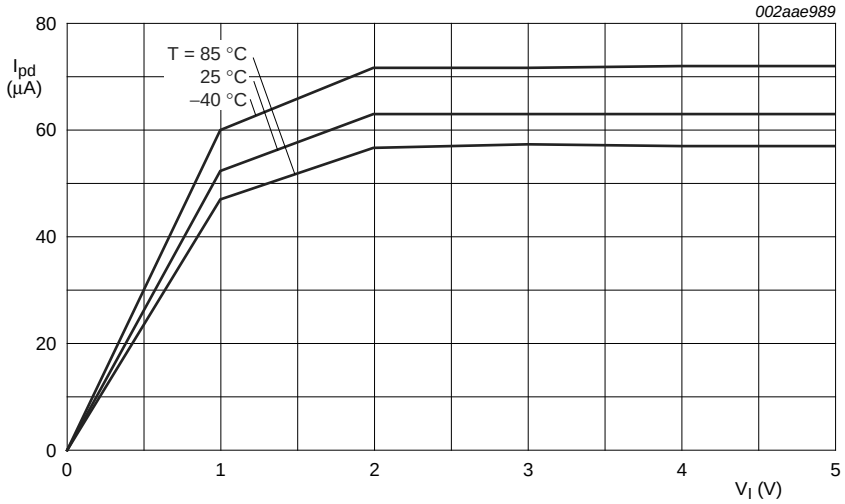
**Fig 10. CoreMark current consumption for power modes 0, 1, 2, and 3**

## 9.4 Electrical pin characteristics




Conditions: $V_{DD}$ = 3.3 V; standard port pins.

**Fig 11. Typical LOW-level output current $I_{OL}$ versus LOW-level output voltage $V_{OL}$**




Conditions: $V_{DD}$ = 3.3 V; standard port pins.

**Fig 14. Typical pull-down current $I_{pd}$ versus input voltage $V_I$**

# 10. Dynamic characteristics

## 10.1 Power-up ramp conditions

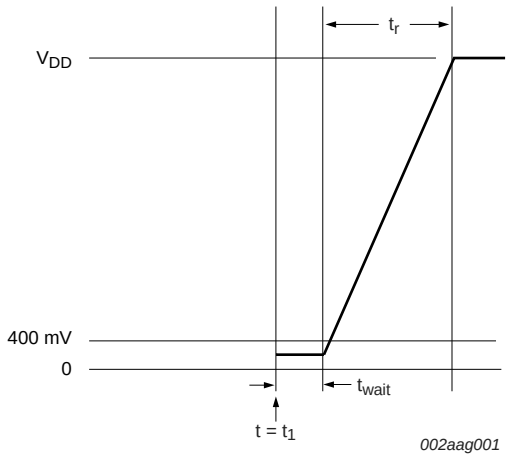
**Table 8. Power-up characteristics**

*$T_{amb}$ = −40 °C to +85 °C.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_r$ | rise time | at t = $t_1$: 0 < $V_I \leq$ 400 mV | [1] | 0 | - | 500 | ms |
| $t_{wait}$ | wait time | | [1][2] | 12 | - | - | µs |
| $V_I$ | input voltage | at t = $t_1$ on pin $V_{DD}$ | | 0 | - | 400 | mV |

[1] See Figure 15.

[2] The wait time specifies the time the power supply must be at levels below 400 mV before ramping up.




Condition: 0 < $V_I \leq$ 400 mV at start of power-up (t = $t_1$)

**Fig 15. Power-up ramp**

## 10.2 Flash memory

**Table 9. Flash characteristics**

*$T_{amb}$ = −40 °C to +85 °C, unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $N_{endu}$ | endurance | | [1] | 10000 | 100 000 | - | cycles |
| $t_{ret}$ | retention time | powered | | 10 | - | - | years |
| | | unpowered | | 20 | - | - | years |
| $t_{er}$ | erase time | sector or multiple consecutive sectors | | 95 | 100 | 105 | ms |
| $t_{prog}$ | programming time | | [2] | 0.95 | 1 | 1.05 | ms |

[1] Number of program/erase cycles.

[2] Programming times are given for writing 256 bytes from RAM to the flash. Data must be written to the flash in blocks of 256 bytes.

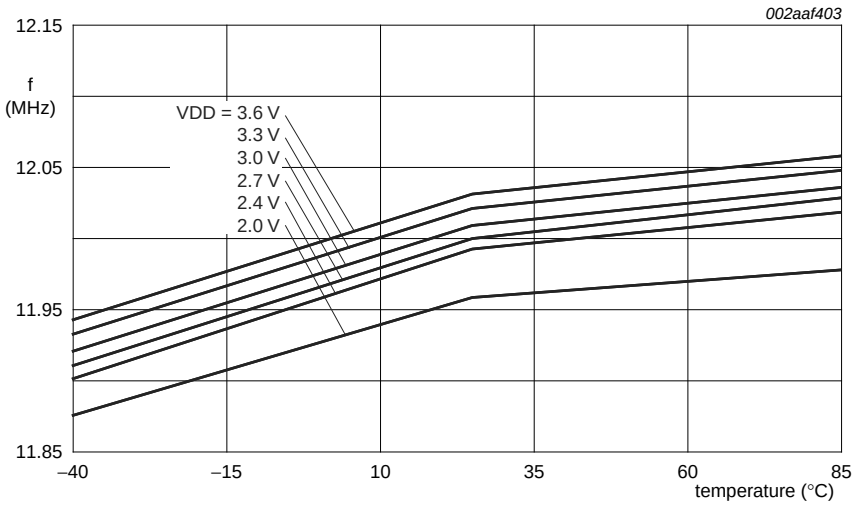
## 10.4 Internal oscillators

**Table 11. Dynamic characteristic: internal oscillators**
*$T_{amb}$ = −40 °C to +85 °C; 2.7 V ≤ $V_{DD}$ ≤ 3.6 V.*[1]

| Symbol | Parameter | Conditions | Min | Typ[2] | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{osc(RC)}$ | internal RC oscillator frequency | - | 11.88 | 12 | 12.12 | MHz |

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.




Conditions: Frequency values are typical values. 12 MHz ± 1 % accuracy is guaranteed for 2.7 V ≤ $V_{DD}$ ≤ 3.6 V and $T_{amb}$ = −40 °C to +85 °C. Variations between parts may cause the IRC to fall outside the 12 MHz ± 1 % accuracy specification for voltages below 2.7 V.

**Fig 17. Internal RC oscillator frequency versus temperature**

**Table 12. Dynamic characteristics: Watchdog oscillator**

| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $f_{osc(int)}$ | internal oscillator frequency | DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register; | [2][3] | - | 9.4 | - | kHz |
| | | DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register | [2][3] | - | 2300 | - | kHz |

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The typical frequency spread over processing and temperature ($T_{amb}$ = −40 °C to +85 °C) is ±40 %.

[3] See *user manual UM10429*.

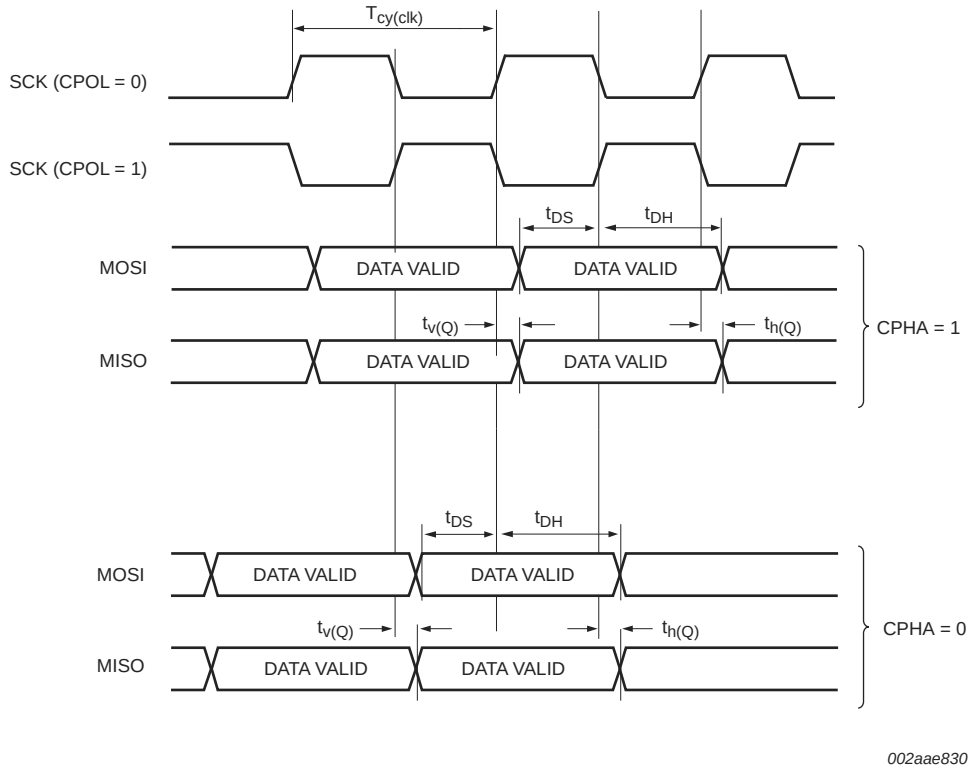



**Fig 19. SPI slave timing in SPI mode**

# 11. Application information

## 11.1 ADC usage notes

The following guidelines show how to increase the performance of the ADC in a noisy environment beyond the ADC specifications listed in Table 6:

- The ADC input trace must be short and as close as possible to the LPC1102/1104 chip.
- The ADC input traces must be shielded from fast switching digital signals and noisy power supply lines.
- Because the ADC and the digital core share the same power supply, the power supply line must be adequately filtered.
- To improve the ADC performance in a very noisy environment, put the device in Sleep mode during the ADC conversion.

## 11.2 XTAL input

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with $C_i$ = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground $C_g$ which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV (RMS) is needed.

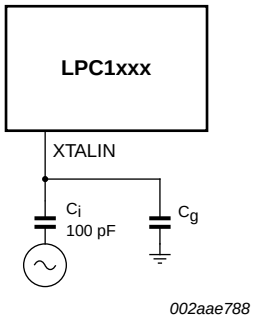



**Fig 20. Slave mode operation of the on-chip oscillator**

In slave mode the input clock signal should be coupled by means of a capacitor of 100 pF (Figure 20), with an amplitude between 200 mV (RMS) and 1000 mV (RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V.

## 11.3 Standard I/O pad configuration

Figure 21 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver
- Digital input: Pull-up enabled/disabled
- Digital input: Pull-down enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Analog input

## 11.5 ADC effective input impedance

A simplified diagram of the ADC input channels can be used to determine the effective input impedance seen from an external voltage source. See Figure 23.

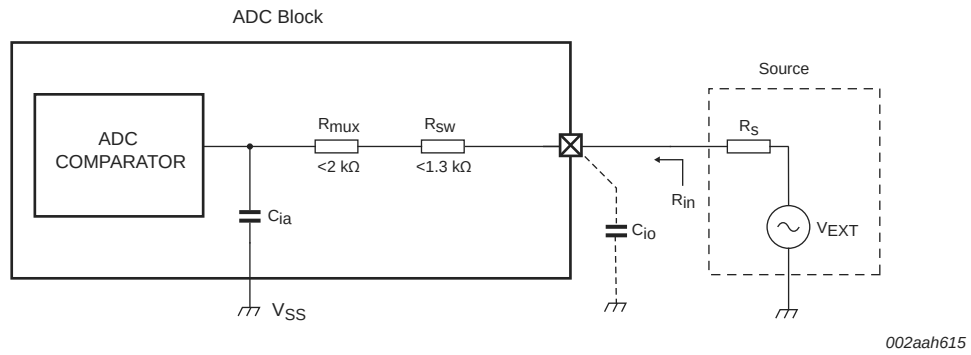



**Fig 23. ADC input channel**

The effective input impedance, $R_{in}$, seen by the external voltage source, $V_{EXT}$, is the parallel impedance of $((1/f_s \times C_{ia}) + R_{mux} + R_{sw})$ and $(1/f_s \times C_{io})$, and can be calculated using Equation 1 with

$f_s$ = sampling frequency

$C_{ia}$ = ADC analog input capacitance

$R_{mux}$ = analog mux resistance

$R_{sw}$ = switch resistance

$C_{io}$ = pin capacitance

$$R_{in} = \left(\frac{1}{f_s \times C_{ia}} + R_{mux} + R_{sw}\right) \| \left(\frac{1}{f_s \times C_{io}}\right) \quad (1)$$

Under nominal operating condition $V_{DD}$ = 3.3 V and with the maximum sampling frequency fs = 400 kHz, the parameters assume the following values:

$C_{ia}$ = 1 pF (max)

$R_{mux}$ = 2 kΩ (max)

$R_{sw}$ = 1.3 kΩ (max)

$C_{io}$ = 7.1 pF (max)

The effective input impedance with these parameters is $R_{in}$ = 308 kΩ.

# 14. Revision history

**Table 16. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| LPC1102_1104 v.7 | 20130926 | Product data sheet | - | LPC1102_1104 v.6 |
| Modifications: | • Parameter $V_I$ updated in Table 4 and Table 5. Condition $V_{DD}$ = 0 added.<br>• Section 11.5 “ADC effective input impedance” added.<br>• Removed $t_{clk(H)}$ and $t_{clk(L)}$ from Figure 18 “SPI master timing in SPI mode” and Figure 19 “SPI slave timing in SPI mode”; spec not characterized. | | | |
| LPC1102_1104 v.6 | 20121231 | Product data sheet | - | LPC1102_1104 v.5 |
| Modifications: | • Added Section 9.3 “CoreMark data”.<br>• Conditions for power consumption in Deep-sleep mode updated in Table 5, Table note 8 and Section 9.2.<br>• Table 4 “Limiting values” expanded for clarity.<br>• BOD reset level 0 added in Table 7. | | | |
| LPC1102_1104 v.5 | 20120727 | Product data sheet | - | LPC1102 v.4 |
| Modifications: | • Added LPC1104UK.<br>• Removed footnote “The peak current is limited to 25 times the corresponding maximum current.” from Table 4.<br>• For parameters $I_{OL}$, $V_{OL}$, $I_{OH}$, $V_{OH}$, changed conditions to 1.8 V ≤ $V_{DD}$ < 2.5 V and 2.5 V ≤ $V_{DD}$ ≤ 3.6 V in Table 5).<br>• WDOSc frequency range corrected.<br>• BOD level 0 removed in Table 7. | | | |
| LPC1102 v.4 | 20110624 | Product data sheet | - | LPC1102 v.3 |
| Modifications: | • ADC sampling frequency corrected in Table 6 (Table note 7).<br>• Parameter $T_{cy(clk)}$ corrected on Table 14.<br>• Windowed WDT features added (Section 7.13).<br>• Programmable open-drain mode added to GPIO pins (Section 7.7).<br>• Pull-up level specified in Table 3, Table note 1 and Section 7.7.<br>• Condition for parameter $T_{stg}$ in Table 4 updated.<br>• Table note 4 of Table 4 updated. | | | |
| LPC1102 v.3 | 20110418 | Product data sheet | - | LPC1102 v.2 |
| Modifications: | • Changed data sheet status to Product.<br>• Power consumption data added (see Figure 6 to Figure 9).<br>• Section 10.1 “Power-up ramp conditions” added.<br>• Reset pad description updated (5 V tolerant) in Table 3.<br>• IRC frequency data added (see Figure 16 “Internal RC oscillator frequency versus temperature”.<br>• Clock output removed from feature list. | | | |
| LPC1102 v.2 | 20101126 | Preliminary data sheet | - | LPC1102 v.1 |
| Modifications: | • Changed data sheet status to Preliminary. | | | |
| LPC1102 v.1 | 20101116 | Objective data sheet | - | - |

# 15. Legal information

## 15.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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