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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	11
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-UFBGA, WLCSP
Supplier Device Package	16-WLCSP (2.17x2.32)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1104uk-118

4. Ordering information

Table 1. Ordering information

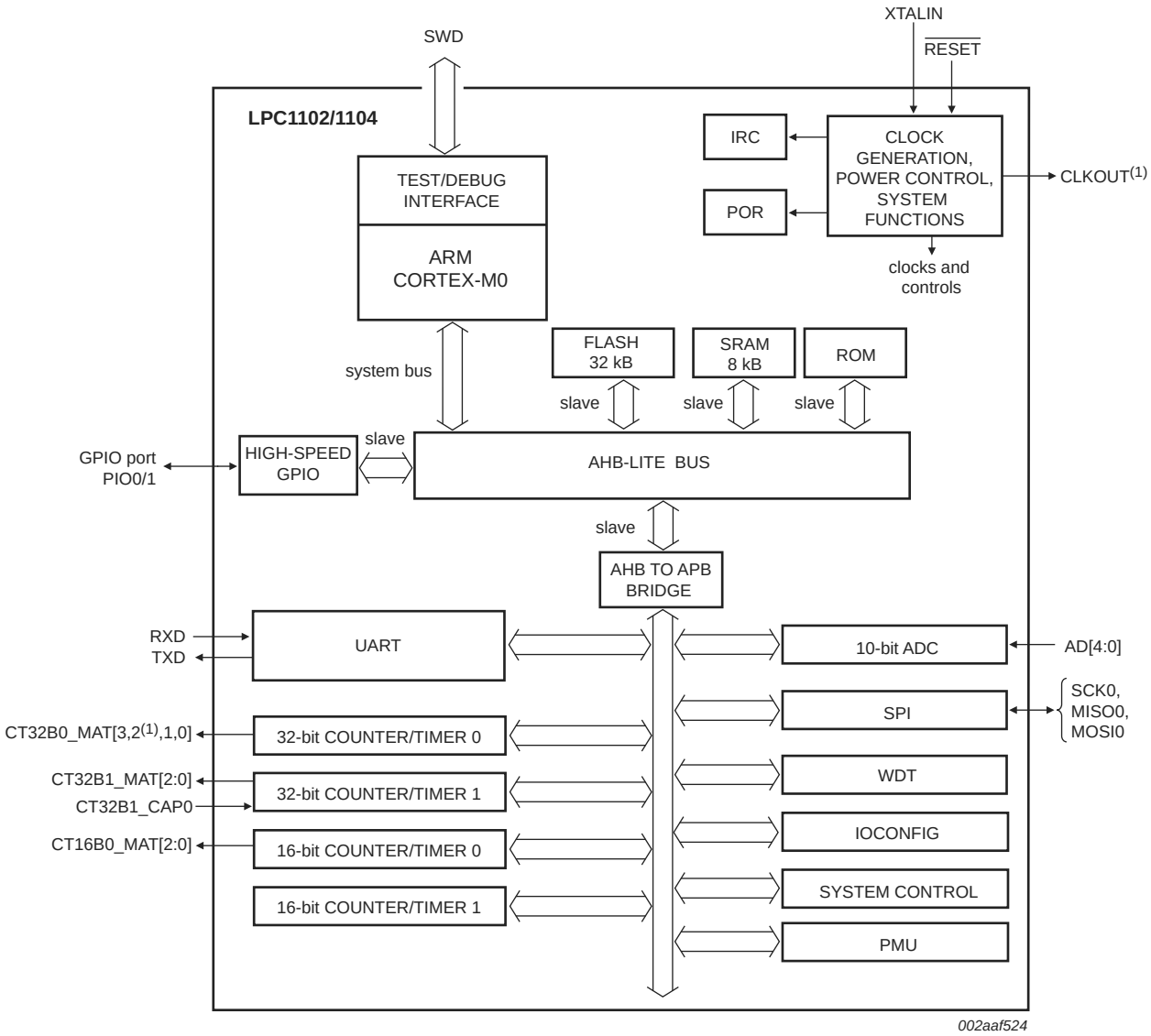
Type number	Package		
	Name	Description	Version
LPC1102UK	WLCSP16	wafer level chip-size package; 16 bumps; 2.17 × 2.32 × 0.6 mm	-
LPC1104UK	WLCSP16	wafer level chip-size package; 16 bumps; 2.17 × 2.32 × 0.6 mm	-

4.1 Ordering options

Table 2. Ordering options

Type number	Flash	Total SRAM	UART RS-485	SPI	ADC channels	Package
LPC1102UK	32 kB	8 kB	1	1	5	WLCSP16
LPC1104UK	32 kB	8 kB	1	1	5	WLCSP16

5. Block diagram



(1) LPC1104 only.

(2) CT32B0_MAT2 LPC1104 only.

Fig 1. LPC1102/1104 block diagram

Table 3. LPC1102/1104 pin description table *…continued*

Symbol	LPC1102	LPC1104	Start logic input	Type	Reset state[1]	Description
R/PIO1_2/ AD3/CT32B1_MAT1	C3[4]	C3[4]	no	-	I; PU	**R —** Reserved.
				I/O	-	**PIO1_2 —** General purpose digital input/output pin.
				I	-	**AD3 —** A/D converter, input 3.
				O	-	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
SWDIO/PIO1_3/AD4/ CT32B1_MAT2	D4[4]	D4[4]	no	I/O	I; PU	**SWDIO —** Serial wire debug input/output.
				I/O	-	**PIO1_3 —** General purpose digital input/output pin.
				I	-	**AD4 —** A/D converter, input 4.
				O	-	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.
PIO1_6/RXD/ CT32B0_MAT0	C2[3]	C2[3]	no	I/O	I; PU	**PIO1_6 —** General purpose digital input/output pin.
				I	-	**RXD —** Receiver input for UART.
				O	-	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.
PIO1_7/TXD/ CT32B0_MAT1	D1[3]	D1[3]	no	I/O	I; PU	**PIO1_7 —** General purpose digital input/output pin.
				O	-	**TXD —** Transmitter output for UART.
				O	-	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
V_{DD}	D2; A1	D2	-	I	-	3.3 V supply voltage to the internal regulator, the external rail, and the ADC. Also used as the ADC reference voltage.
XTALIN	B2[5]	B1[5]	-	I	-	External clock input and input to internal clock generator circuits. Input voltage must not exceed 1.8 V.
V_{SS}	D3; B1	D3	-	I	-	Ground.

[1] Pin state at reset for default function: I = Input; PU = internal pull-up enabled (pins pulled up to full V_{DD} level (V_{DD} = 3.3 V)).

[2] 5 V tolerant pad. See Figure 22 for the reset pad configuration.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 21).

[4] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see Figure 21).

[5] When the external clock is not used, connect XTALIN as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise).

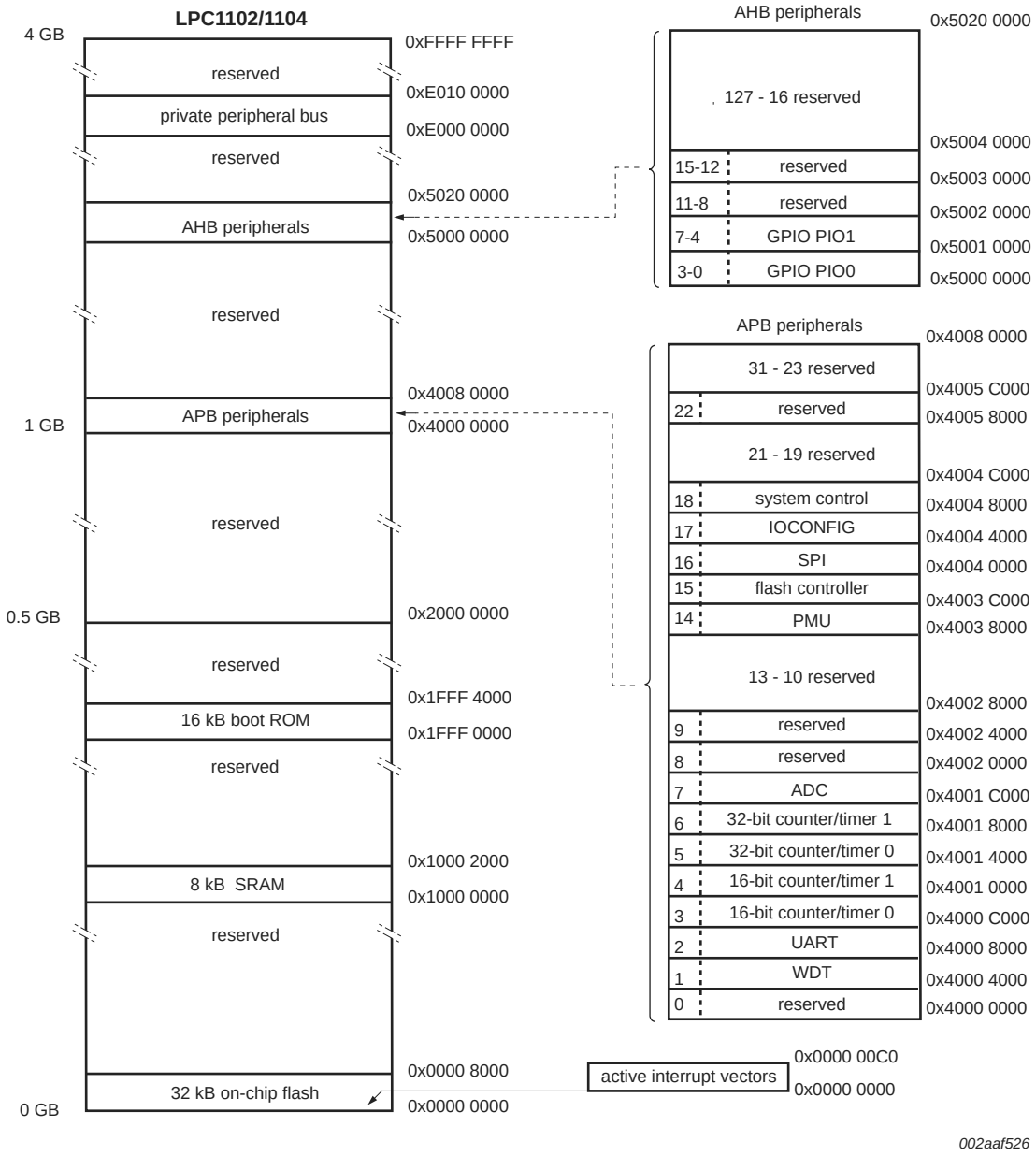


Fig 3. LPC1102/1104 memory map

7.5 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is an integral part of the Cortex-M0. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.5.1 Features

- Controls system exceptions and peripheral interrupts.
- In the LPC1102/1104, the NVIC supports 19 vectored interrupts including up to 6 inputs to the start logic from individual GPIO pins.

- Four programmable interrupt priority levels, with hardware priority level masking.
- Software interrupt generation.

7.5.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Any GPIO pin (total of up to 11 pins) regardless of the selected function, can be programmed to generate an interrupt on a level, or rising edge or falling edge, or both.

7.6 IOCONFIG block

The IOCONFIG block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Peripherals should be connected to the appropriate pins prior to being activated and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

7.7 Fast general purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

The LPC1102/1104 use accelerated GPIO functions:

- GPIO registers are a dedicated AHB peripheral so that the fastest possible I/O timing can be achieved.
- Entire port value can be written in one instruction.

Additionally, any GPIO pin (total of 11 pins) providing a digital function can be programmed to generate an interrupt on a level, a rising or falling edge, or both.

7.7.1 Features

- Bit level port registers allow a single instruction to set or clear any number of bits in one write operation.
- Direction control of individual bits.
- All I/O default to inputs with pull-ups enabled after reset.
- Pull-up/pull-down resistor configuration can be programmed through the IOCONFIG block for each GPIO pin.
- All GPIO pins are pulled up to 3.3 V (V_{DD} = 3.3 V) if their pull-up resistor is enabled in the IOCONFIG block.
- Programmable open-drain mode.

7.8 UART

The LPC1102/1104 contain one UART.

Support for RS-485/9-bit mode allows both software address detection and automatic address detection using 9-bit mode.

The UART includes a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.8.1 Features

- Maximum UART data bit rate of 3.125 Mbit/s.
- 16 Byte Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit mode.

7.9 SPI serial I/O controller

The LPC1102/1104 contain one SPI controller and fully supports SSP features.

The SPI controller is capable of operation on a SSP, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SPI supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

Remark: Care must be taken when using the SPI because the SPI clock SCK and the serial wire debug clock SWCLK share the same pin on the WLCSP16 package. Once the SPI is enabled, the serial wire debugger is no longer available (LPC1102 only).

7.9.1 Features

- Maximum SPI speed of 25 Mbit/s (master) or 4.17 Mbit/s (slave) (in SSP mode)
- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame

7.10 10-bit ADC

The LPC1102/1104 contain one ADC. It is a single 10-bit successive approximation ADC with five channels.

7.10.1 Features

- 10-bit successive approximation ADC.

- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the IRC or the dedicated watchdog oscillator (WDO). This gives a wide range of potential timing choices of watchdog operation under different power conditions.

7.14 Clocking and power control

7.14.1 Crystal oscillators

The LPC1102/1104 include two independent oscillators. These are the Internal RC oscillator (IRC) and the Watchdog oscillator. Each oscillator can be used for more than one purpose as required in a particular application.

Following reset, the LPC1102/1104 operate from the Internal RC oscillator until switched by software. This allows systems to operate without any external crystal and the bootloader code to operate at a known frequency.

See Figure 4 for an overview of the LPC1102/1104 clock generation.

its frequency range while the PLL is providing the desired output frequency. The PLL output frequency must be lower than 100 MHz. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 μs.

7.14.3 Clock output (LPC1104 only)

The LPC1104 features a clock output function that routes the IRC oscillator, the system oscillator, the watchdog oscillator, or the main clock to an output pin.

7.14.4 Wake-up process

The LPC1102/1104 begin operation at power-up by using the 12 MHz IRC oscillator as the clock source. This allows chip operation to resume quickly. If an external clock or the PLL is needed by the application, software will need to enable these features and wait for them to stabilize before they are used as a clock source.

7.14.5 Power control

The LPC1102/1104 support a variety of power control features. There are two special modes of processor power reduction: Sleep mode and Deep-sleep mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals, allowing fine tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

7.14.5.1 Power profiles

The power consumption in Active and Sleep modes can be optimized for the application through a simple call to the power profiles. The power configuration routine configures the LPC1102/1104 for one of the following power modes:

- Default mode corresponding to power configuration after reset.
- CPU performance mode corresponding to optimized processing capability.
- Efficiency mode corresponding to optimized balance of current consumption and CPU performance.
- Low-current mode corresponding to lowest power consumption.

In addition, the power profiles includes a routine to select the optimal PLL settings for a given system clock and PLL input clock.

7.14.5.2 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

7.14.5.3 Deep-sleep mode

In Deep-sleep mode, the chip is in Sleep mode, and in addition all analog blocks are shut down except for the watchdog oscillator and the BOD circuit, which can be configured to remain running in Deep-sleep mode to allow a reset initiated by a timer or BOD event. Deep-sleep mode allows for additional power savings.

Six of the GPIO pins (see Table 3) serve as external wake-up pins to a dedicated start logic to wake up the chip from Deep-sleep mode.

The clock source should be switched to IRC before entering Deep-sleep mode unless the watchdog oscillator remains running in Deep-sleep mode. The IRC can be switched on and off glitch-free and provides a clean clock signal after start-up.

7.15 System control

7.15.1 Start logic

The start logic connects external pins to corresponding interrupts in the NVIC. Each pin shown in Table 3 as input to the start logic has an individual interrupt in the NVIC interrupt vector table. The start logic pins can serve as external interrupt pins when the chip is running. In addition, an input signal on the start logic pins can wake up the chip from Deep-sleep mode when all clocks are shut down.

The start logic must be configured in the system configuration block and in the NVIC before being used.

7.15.2 Reset

Reset has four sources on the LPC1102/1104: the $\overline{\text{RESET}}$ pin, the Watchdog reset, Power-On Reset (POR), and the BrownOut Detection (BOD) circuit. In addition, there is an ARM software reset. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip reset by any source, once the operating voltage attains a usable level, starts the IRC and initializes the flash controller.

A LOW-going pulse as short as 50 ns resets the part.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

7.15.3 Brownout detection

The LPC1102/1104 include up to four levels for monitoring the voltage on the V_{DD} pin. If this voltage falls below one of the three selected levels, the BOD asserts an interrupt signal to the NVIC. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC in order to cause a CPU interrupt; if not, software can monitor the signal by reading a dedicated status register. Four additional threshold levels can be selected to cause a forced reset of the chip.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage (core and external rail)		[2]	−0.5	+4.6	V
V_I	input voltage	5 V tolerant I/O pins; $V_{DD} \geq 1.8$ V	[2][3]	−0.5	+5.5	V
		$V_{DD} = 0$ V		−0.5	+3.6	V
V_{IA}	analog input voltage	pin configured as analog input	[2][4]	−0.5	+4.6	V
I_{DD}	supply current	per supply pin	[5]	-	100	mA
I_{SS}	ground current	per ground pin	[5]	-	100	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD}) < V_I < (1.5V_{DD})$; $T_j < 125$ °C		-	100	mA
T_{stg}	storage temperature	non-operating	[6]	−65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins	[7]		6500	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

c) The limiting values are stress ratings only. Operating the part at these values is not recommended and proper operation is not guaranteed. The conditions for functional operation are specified in Table 5.

[2] Maximum/minimum voltage above the maximum operating voltage (see Table 5) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

[3] Including voltage on outputs in 3-state mode.

[4] See Table 6 for maximum operating voltage.

[5] The peak current is limited to 25 times the corresponding maximum current.

[6] The maximum non-operating storage temperature is different than the temperature for required shelf life which should be determined based on required shelf lifetime. Please refer to the JEDEC spec (J-STD-033B.1) for further details.

[7] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

9. Static characteristics

Table 5. Static characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{DD}	supply voltage (core and external rail)			1.8	3.3	3.6	V
I_{DD}	supply current	Active mode; code `while(1){}` executed from flash					
		system clock = 12 MHz; V_{DD} = 3.3 V	[2][3][4][5][6]	-	2	-	mA
		system clock = 50 MHz; V_{DD} = 3.3 V	[2][3][5][6][7]	-	7	-	mA
		Sleep mode; system clock = 12 MHz; V_{DD} = 3.3 V	[2][3][4][5][6]	-	1	-	mA
		Deep-sleep mode; V_{DD} = 3.3 V	[2][3][8]	-	2	-	μA
Standard port pins, $\overline{\text{RESET}}$							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled		-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled		-	0.5	10	nA
V_I	input voltage	pin configured to provide a digital function; $V_{DD} \geq 1.8$ V; 5 V tolerant pins	[9]	0	-	5.0	V
		V_{DD} = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-level output voltage	2.5 V ≤ V_{DD} ≤ 3.6 V; I_{OH} = −4 mA		$V_{DD} - 0.4$	-	-	V
		1.8 V ≤ V_{DD} < 2.5 V; I_{OH} = −3 mA		$V_{DD} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	2.5 V ≤ V_{DD} ≤ 3.6 V; I_{OL} = 4 mA		-	-	0.4	V
		1.8 V ≤ V_{DD} < 2.5 V; I_{OL} = 3 mA		-	-	0.4	V

9.1 BOD static characteristics

Table 7. BOD static characteristics[1]
T_{amb} = 25 °C.

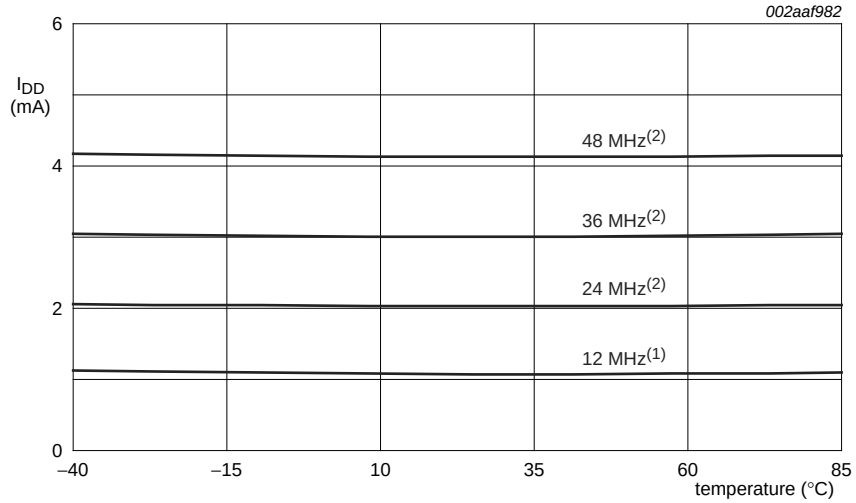
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 1				
		assertion	-	2.22	-	V
		de-assertion	-	2.35	-	V
		interrupt level 2				
		assertion	-	2.52	-	V
		de-assertion	-	2.66	-	V
		interrupt level 3				
		assertion	-	2.80	-	V
		de-assertion	-	2.90	-	V
		reset level 0				
		assertion	-	1.46	-	V
		de-assertion	-	1.63	-	V
		reset level 1				
		assertion	-	2.06	-	V
		de-assertion	-	2.15	-	V
		reset level 2				
		assertion	-	2.35	-	V
		de-assertion	-	2.43	-	V
		reset level 3				
		assertion	-	2.63	-	V
		de-assertion	-	2.71	-	V

[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see *User manual UM10429*.

9.2 Power consumption

Power measurements in Active, Sleep, and Deep-sleep modes were performed under the following conditions (see *user manual UM10429*):

- All digital pins configured as GPIO with pull-up resistor disabled in the IOCONFIG block.
- GPIO pins configured as outputs using the GPIOnDIR registers.
- Write 0 to all GPIOnDATA registers to drive the outputs LOW.
- Write a 1 to bit 4 and bit 5 of the GPIO0DIR register at location 0x5000 8000 and a 0 to bit 4 and bit 5 of the GPIO0DATA register at location 0x5000 3FFC. This ensures that not-bonded out pins are in a well-defined state.

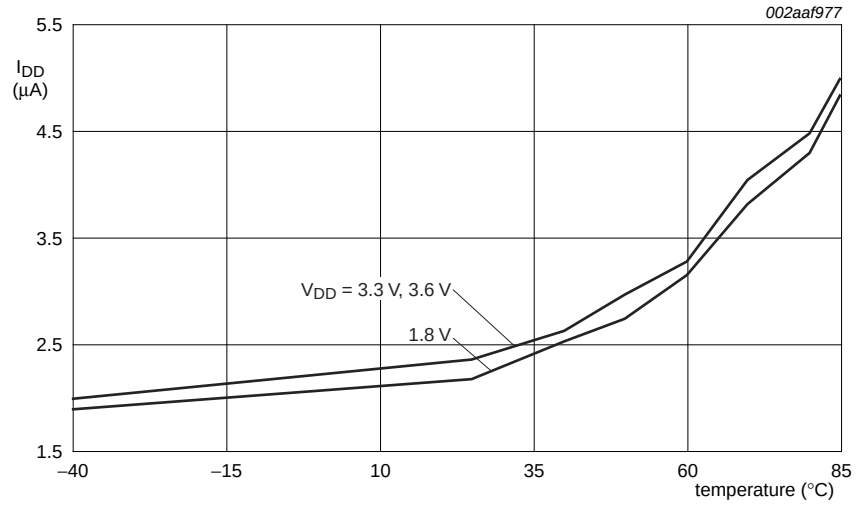


Conditions: V_{DD} = 3.3 V; sleep mode entered from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL= 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

(1) System PLL disabled; IRC enabled.

(2) System PLL enabled; IRC disabled.

Fig 8. Sleep mode: Typical supply current I_{DD} versus temperature for different system clock frequencies

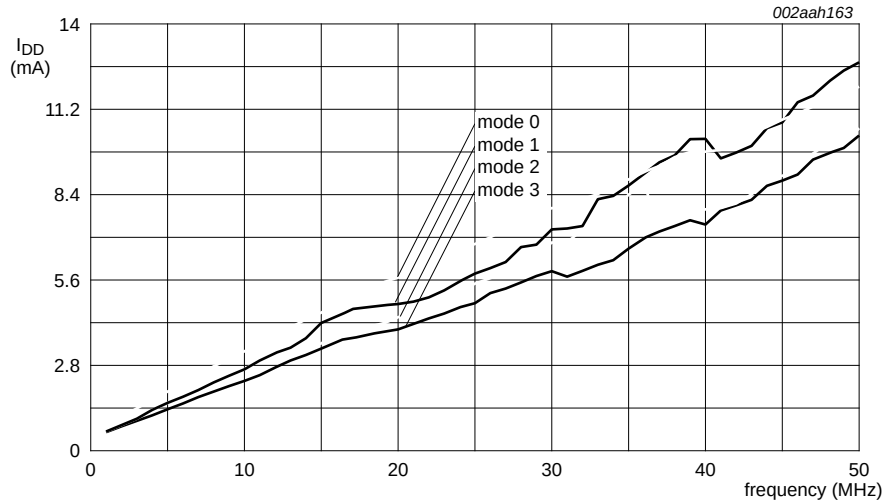


Conditions: BOD disabled; all oscillators and analog blocks disabled in the PDSLEEPCFG register (PDSLEEPCFG = 0x0000 18FF).

Remark: Before entering deep-sleep mode, you must write a 0 to bit 4 and bit 5 of the GPIO0DATA register at location 0x5000 3FFC and a 1 to bit 4 and bit 5 of the GPIO0DIR register at location 0x5000 8000.

Fig 9. Deep-sleep mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

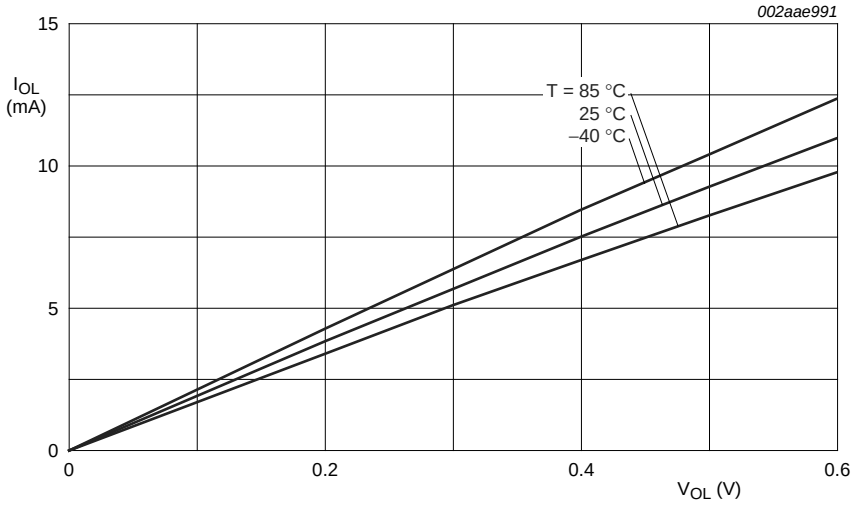
9.3 CoreMark data



External signal generator providing 1 MHz to 20 MHz signal drives the XTALIN input; when testing 1 MHz to 19 MHz the system PLL is OFF, SYSAHBCLKDIV = 1; when testing 20 MHz to 50 MHz the system PLL is configured so that SYSAHBCLKDIV = 1.

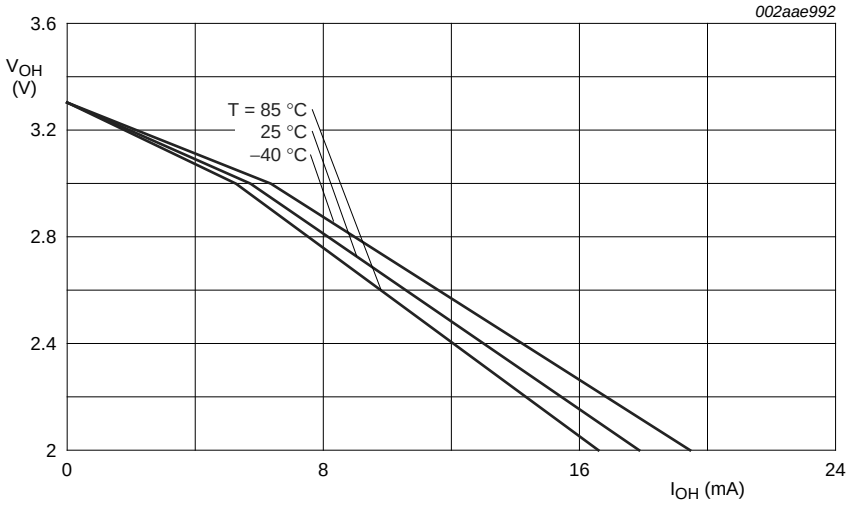
Fig 10. CoreMark current consumption for power modes 0, 1, 2, and 3

9.4 Electrical pin characteristics



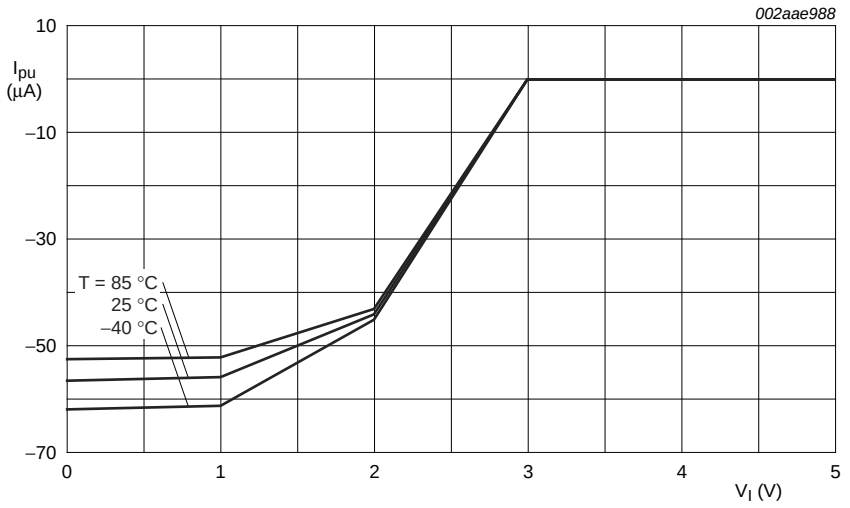
Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 11. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



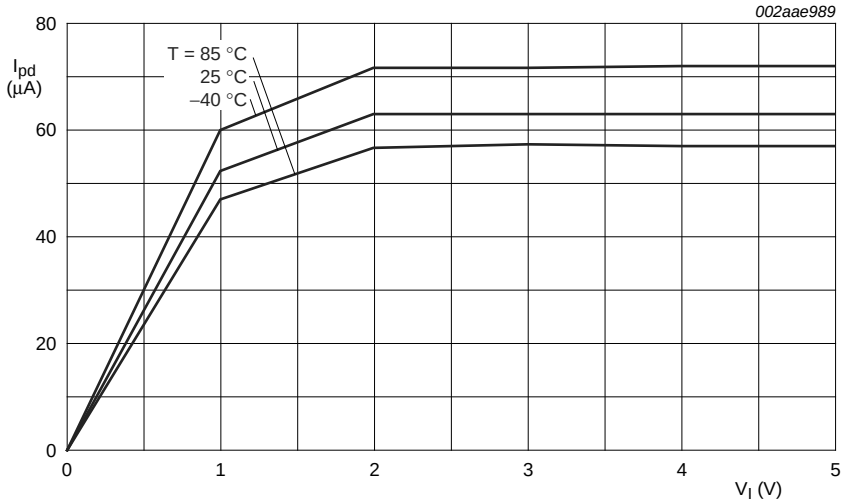
Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 12. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 13. Typical pull-up current I_{pu} versus input voltage V_I



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 14. Typical pull-down current I_{pd} versus input voltage V_I

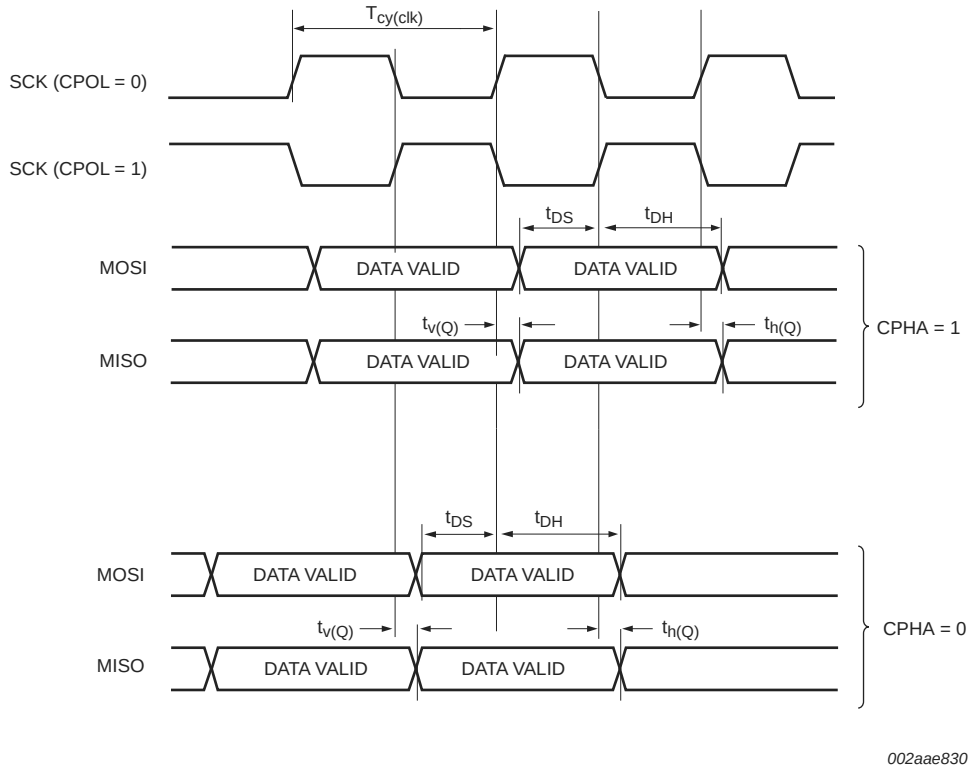


Fig 19. SPI slave timing in SPI mode

11. Application information

11.1 ADC usage notes

The following guidelines show how to increase the performance of the ADC in a noisy environment beyond the ADC specifications listed in Table 6:

- The ADC input trace must be short and as close as possible to the LPC1102/1104 chip.
- The ADC input traces must be shielded from fast switching digital signals and noisy power supply lines.
- Because the ADC and the digital core share the same power supply, the power supply line must be adequately filtered.
- To improve the ADC performance in a very noisy environment, put the device in Sleep mode during the ADC conversion.

11.2 XTAL input

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV (RMS) is needed.

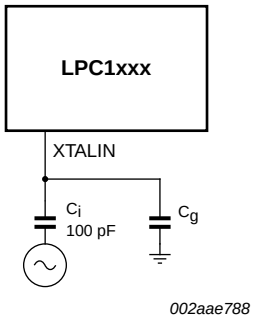


Fig 20. Slave mode operation of the on-chip oscillator

In slave mode the input clock signal should be coupled by means of a capacitor of 100 pF (Figure 20), with an amplitude between 200 mV (RMS) and 1000 mV (RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V.

11.3 Standard I/O pad configuration

Figure 21 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver
- Digital input: Pull-up enabled/disabled
- Digital input: Pull-down enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Analog input

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Date of release: 26 September 2013
Document identifier: LPC1102_1104