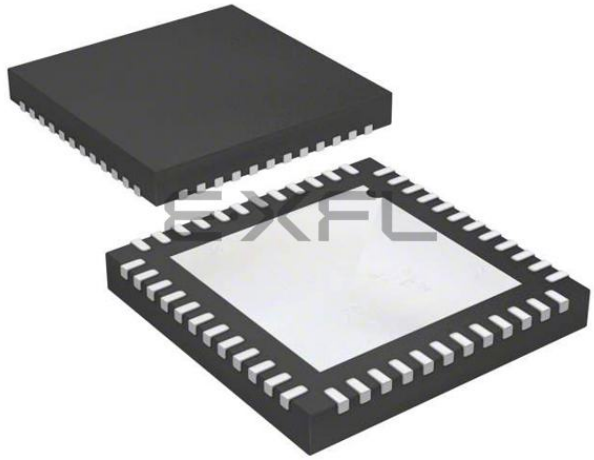

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	20.48MHz
Connectivity	LINbus, SPI, UART/USART
Peripherals	POR, PSM, Temp Sensor, WDT
Number of I/O	9
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 32
Voltage - Supply (Vcc/Vdd)	3.5V ~ 18V
Data Converters	A/D 2x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 115°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad, CSP
Supplier Device Package	48-LFCSP-VQ (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc7034bcpz-rl

REVISION HISTORY

5/10—Rev. A to Rev. B

Changes to Table 6 15
Changes to Timers Section 71

8/09—Rev. 0 to Rev. A

Changes to Features Section 1
Changes to Table 1 4
Added Exposed Pad Notation to Figure 7 and Table 7 16
Changes to Theory of Operation 20
Changes to Table 45 65
Changes to Figure 35 78
Changes to Table 96 128
Changes to Figure 57 131

4/08—Revision 0: Initial Version

Table 3. SPI Master Mode Timing—PHASE Mode = 0

Parameter	Description	Min	Typ	Max	Unit
t_{SL}	SCLK low pulse width[1]		(SPIDIV + 1) × t_{HCLK}		ns
t_{SH}	SCLK high pulse width[1]		(SPIDIV + 1) × t_{HCLK}		ns
t_{DAV}	Data output valid after SCLK edge[2]			(2 × t_{UCLK}) + (2 × t_{HCLK})	ns
t_{DOSU}	Data output setup before SCLK edge		½ t_{SL}		ns
t_{DSU}	Data input setup time before SCLK edge	0			ns
t_{DHD}	Data input hold time after SCLK edge[2]	3 × t_{UCLK}			ns
t_{DF}	Data output fall time		3.5		ns
t_{DR}	Data output rise time		3.5		ns
t_{SR}	SCLK rise time		3.5		ns
t_{SF}	SCLK fall time		3.5		ns

[1] t_{HCLK} depends on the clock divider (CD) bits in the POWCON MMR. $t_{HCLK} = t_{UCLK}/2^{CD}$.
[2] t_{UCLK} = 48.8 ns and corresponds to the 20.48 MHz internal clock from the PLL before the clock divider.

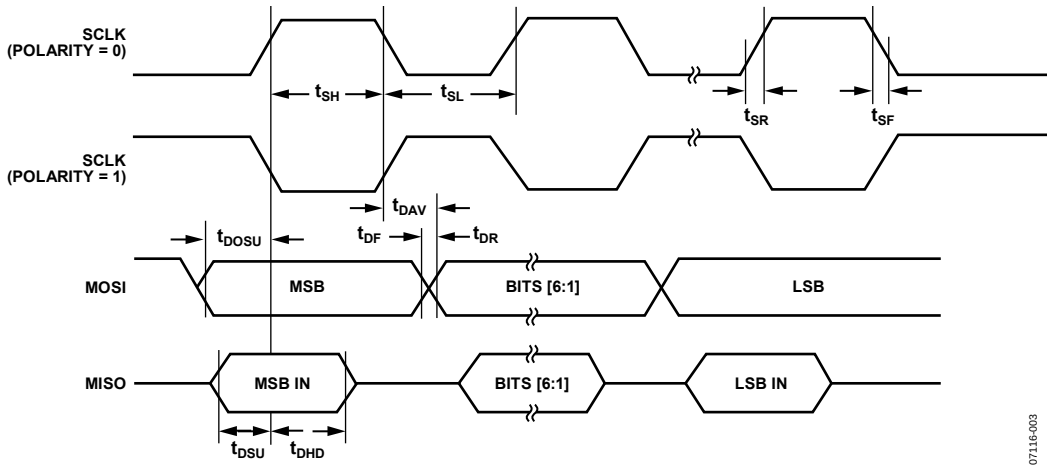

Figure 3. SPI Master Mode Timing—PHASE Mode = 0

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

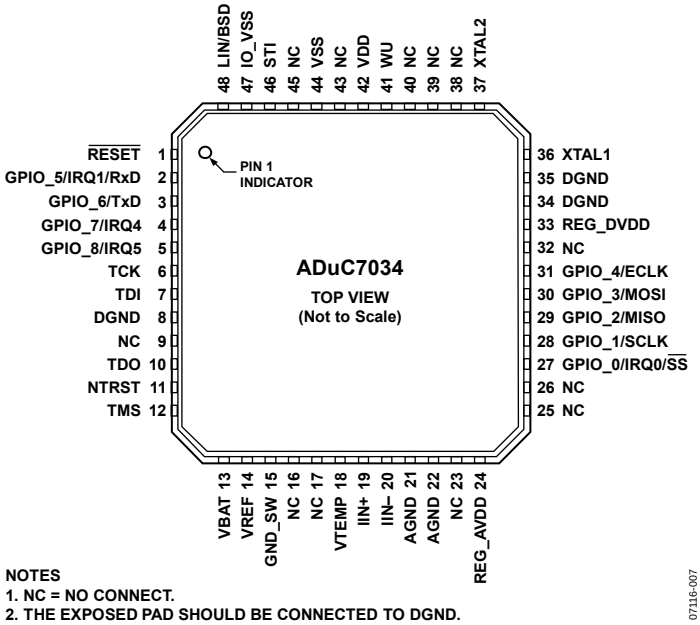

Figure 7. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	$\overline{\text{RESET}}$	I	Reset Input. Active low. This pin has an internal weak pull-up resistor to REG_DVDD and should be left unconnected when not in use. For added security and robustness, it is recommended that this pin be strapped via a resistor to REG_DVDD.
2	GPIO_5/IRQ1/RxD	I/O	General-Purpose Digital IO 5/External Interrupt Request 1 (Active High)/Receive Data for UART Serial Port. By default and after a power-on reset, this pin is configured as an input. The pin has an internal weak pull-up resistor and should be left unconnected when not in use.
3	GPIO_6/TxD	I/O	General-Purpose Digital IO 6/Transmit Data for UART Serial Port. By default and after a power-on reset, this pin is configured as an input. The pin has an internal weak pull-up resistor and should be left unconnected when not in use.
4	GPIO_7/IRQ4	I/O	General-Purpose Digital IO 7/External Interrupt Request 4 (Active High). By default and after a power-on reset, this pin is configured as an input. The pin has an internal weak pull-up resistor and should be left unconnected when not in use.
5	GPIO_8/IRQ5	I/O	General-Purpose Digital IO 8/External Interrupt Request 5 (Active High). By default and after power-on reset, this pin is configured as an input. The pin has an internal weak pull-up resistor and should be left unconnected when not in use.
6	TCK	I	JTAG Test Clock. This clock input pin is one of the standard 5-pin JTAG debug ports on the part. TCK is an input pin only and has an internal weak pull-up resistor. This pin should be left unconnected when not in use.
7	TDI	I	JTAG Test Data Input. This data input pin is one of the standard 5-pin JTAG debug ports on the part. TDI is an input pin only and has an internal weak pull-up resistor. This pin should be left unconnected when not in use.
8, 34, 35	DGND	S	Ground Reference for On-Chip Digital Circuits.
9, 16, 23, 32, 38 to 40, 43, 45	NC		No Connect. Not internally connected and are reserved for possible future use. Therefore, do not externally connect these pins. These pins can be grounded, if required.
17, 25, 26	NC		No Connect. Internally connected and are reserved for possible future use. Therefore, do not externally connect these pins. These pins can be grounded, if required.
10	TDO	O	JTAG Test Data Output. This data output pin is one of the standard 5-pin JTAG debug ports on the part. TDO is an output pin only. At power-on, this output is disabled and pulled high via an internal weak pull-up resistor. This pin should be left unconnected when not in use.

VOLTAGE/TEMPERATURE CHANNEL ADC (V-/T-ADC)

The voltage/temperature channel ADC (V-/T-ADC) converts additional battery parameters, such as voltage and temperature. The input to this channel can be multiplexed from one of three input sources, namely, an external voltage, an external temperature sensor circuit, or an on-chip temperature sensor.

As with the current channel ADC (I-ADC), the V-/T-ADC employs an identical Σ-Δ conversion technique, including a modified sinc3 low-pass filter to provide a valid 16-bit data conversion result at programmable output rates from 4 Hz to 8 kHz. An external RC filter network is not required because it is internally implemented in the voltage channel.

The external battery voltage (VBAT) is routed to the ADC input via an on-chip high voltage (divide-by-24) resistive attenuator. The voltage attenuator buffers are automatically enabled when the voltage attenuator input is selected.

The battery temperature can be derived through the on-chip temperature sensor or an external temperature sensor input. The time to a first valid (fully settled) result after an input channel switch on the voltage/temperature channel is three ADC conversion cycles with chop mode disabled.

This ADC is again buffered but, unlike the current channel, has a fixed input range of 0 V to VREF on VTEMP and 0 V to 28.8 V on VBAT (assuming an internal 1.2 V reference). A top-level overview of this ADC signal chain is shown in Figure 18.

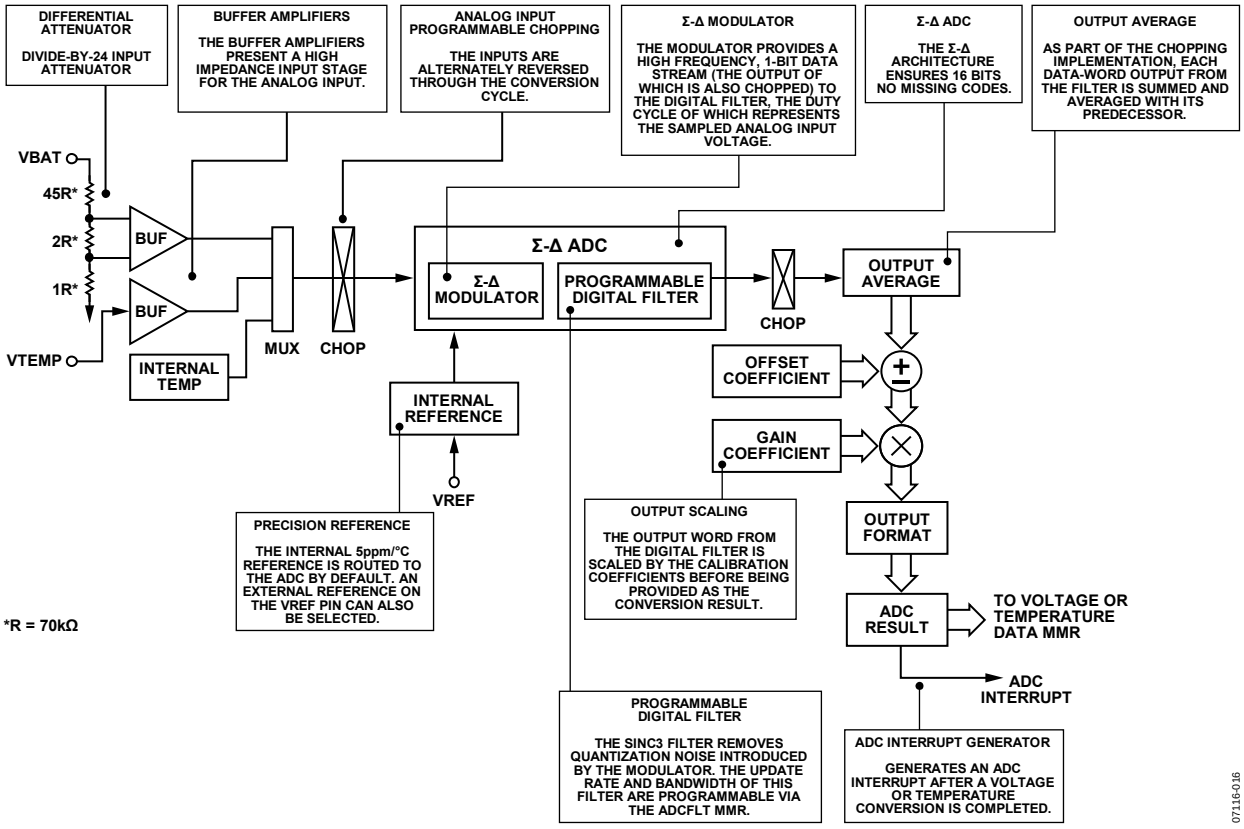

Figure 18. Voltage/Temperature ADC, Top-Level Overview

ADC GROUND SWITCH

The ADuC7034 features an integrated ground switch pin, GND_SW (Pin 15). This switch allows the user to dynamically disconnect the ground from external devices and instead use either a direct connection to ground or a connection to ground via a 20 kΩ resistor. If the latter option is chosen, the additional resistor can be used to reduce the number of external components required for an NTC circuit. In addition, the ground switch feature can be used to reduce power consumption on application-specific boards.

An example application is shown in Figure 19.

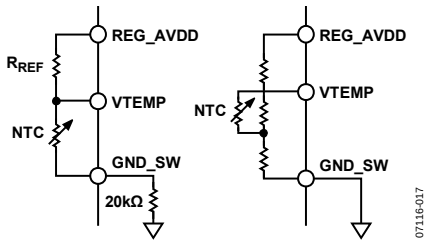

Figure 19. Example External Temperature Sensor Circuits

Figure 19 shows an external NTC used in two modes, with one using the internal 20 kΩ resistor and the second showing a direct connection to ground via the GND_SW.

ADCCFG[7] controls the connection of the ground switch to ground, and ADCMDE[6] controls the GND_SW resistance, as shown in Figure 20.

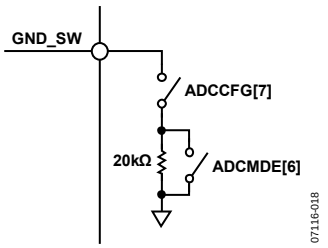

Figure 20. Internal Ground Switch Configuration

The possible combinations of ADCCFG[7] and ADCMDE[6] are shown in Table 30.

Table 30. GND_SW Configuration

ADCCFG[7]	ADCMDE[6]	GND_SW
0	0	Floating
0	1	Floating
1	0	Direct connection to ground
1	1	Connected to ground via 20 kΩ resistor

ADC NOISE PERFORMANCE TABLES

Table 31, Table 32, and Table 33 list the output rms noise in microvolts for some typical output update rates on the I-ADC and V-/T-ADC. The numbers are typical and are generated at a differential input voltage of 0 V. The output rms noise is specified as the standard deviation (or 1 Σ) of the distribution of ADC output codes collected when the ADC input voltage is at a dc voltage. It is expressed in microvolts rms.

Table 31. Typical Output RMS Noise of Current Channel ADC in Normal Power Mode

		ADC Input Range (Gain Setting)									
ADCFLT	Data Update Rate	±2.3 mV (512)	±4.6 mV (256)	±4.68 mV (128)	±18.75 mV (64)	±37.5 mV (32)	±75 mV (16)	±150 mV (8)	±300 mV (4[1])	±600 mV (2[1])	±1.2 V (1[1])
0xBF1D	4 Hz	0.040 µV	0.040 µV	0.043 µV	0.045 µV	0.087 µV	0.175 µV	0.35 µV	0.7 µV	1.4 µV	2.8 µV
0x961F	10 Hz	0.060 µV	0.060 µV	0.060 µV	0.065 µV	0.087 µV	0.175 µV	0.35 µV	0.7 µV	1.4 µV	2.8 µV
0x007F	50 Hz	0.142 µV	0.142 µV	0.144 µV	0.145 µV	0.170 µV	0.305 µV	0.380 µV	0.7 µV	2.3 µV	2.8 µV
0x0007	1 kHz	0.620 µV	0.620 µV	0.625 µV	0.625 µV	0.770 µV	1.310 µV	1.650 µV	2.520 µV	7.600 µV	7.600 µV
0x0000	8 kHz	2.000 µV	2.000 µV	2.000 µV	2.000 µV	2.650 µV	4.960 µV	8.020 µV	15.0 µV	55.0 µV	55.0 µV

[1] The maximum absolute input voltage allowed is –200 mV to +300 mV relative to ground.

Table 32. Typical Output RMS Noise (Referred to ADC Voltage Attenuator Input) of Voltage Channel ADC

ADCFLT	Data Update Rate	28.8 V ADC Input Range
0xBF1D	4 Hz	65 µV
0x961F	10 Hz	65 µV
0x0007	1 kHz	180 µV
0x0000	8 kHz	1600 µV

Table 33. Typical Output RMS Noise of Temperature Channel ADC

ADCFLT	Data Update Rate	0 V to 1.2 V ADC Input Range
0xBF1D	4 Hz	2.8 µV
0x961F	10 Hz	2.8 µV
0x0007	1 kHz	7.5 µV
0x0000	8 kHz	55 µV

ADC CALIBRATION

As shown in detail in the top-level diagrams (Figure 17 and Figure 18), the signal flow through all ADC channels can be described in as follows:

1. An input voltage is applied through an input buffer (and through PGA in the case of the I-ADC) to the Σ-Δ modulator.
2. The modulator output is applied to a programmable digital decimation filter.
3. The filter output result is averaged if chopping is used.
4. An offset value (ADCxOF) is subtracted from the result.
5. The result is scaled by a gain value (ADCxGN).
6. The result is formatted as twos complement/offset binary, rounded to 16 bits, or clamped to ±full scale.

Each ADC has a specific offset and gain correction or calibration coefficient associated with it that is stored in MMR-based offset and gain registers (ADCxOF and ADCxGN). The offset and gain registers can be used to remove offsets and gain errors within the part as well as system-level offset and gain errors external to the part.

These registers are configured at power-on with a factory-programmed calibration value. These factory-set calibration values vary from part to part, reflecting the manufacturing variability of internal ADC circuits. However, these registers can also be overwritten by user code if the ADC is in idle mode and are automatically overwritten if an offset or gain calibration cycle is initiated by the user through the mode bits in the ADCMDE[2:0] MMR. Two types of automatic calibration are available to the user, namely, self-calibration or system calibration.

Self-Calibration

In self-calibration of offset errors, the ADC generates its calibration coefficient based on an internally generated 0 V, whereas in self-calibration of gain errors the coefficient is based on the full-scale voltage. Although self-calibration can correct offset and gain errors within the ADC, it cannot compensate for external errors in the system, such as shunt resistor tolerance/drift and external offset voltages.

Note that in self-calibration mode, ADC0GN must contain the values for PGA = 1 before a calibration scheme is started.

System Calibration

In system calibration of offset errors, the ADC generates its calibration coefficient based on an externally generated zero-scale voltage, whereas in system calibration of gain errors the coefficient is based on the full-scale voltage. The calibration coefficient is applied to the external ADC input for the duration of the calibration cycle.

The duration of an offset calibration is a single conversion cycle ($3/f_{ADC}$ chop off, $2/f_{ADC}$ chop on) before returning the ADC to idle mode. A gain calibration is a two-stage process and, therefore, takes twice as long as an offset calibration cycle. When a calibration cycle is initiated, any ongoing ADC conversion is immediately halted, the calibration is automatically performed at the ADC update rate programmed in ADCFLT, and the ADC is always returned to idle after any calibration cycle. It is strongly recommended that ADC calibration be initiated at as low an ADC update rate as possible (and therefore requires a high SF value in ADCFLT) to minimize the impact of ADC noise during calibration.

Using the Offset and Gain Calibration

If the chop enable bit (ADCFLT[15]) is enabled, internal ADC offset errors are minimized and an offset calibration may not be required. If chopping is disabled, however, an initial offset calibration is required and may need to be repeated, particularly after a large change in temperature.

Depending on system accuracy requirements, a gain calibration, especially in the context of the I-ADC (with internal PGA), may need to be performed at all relevant system gain ranges. If it is not possible to apply an external full-scale current on all gain ranges, apply a lower current and then scale the result produced by the calibration. For example, apply a 50% current and then divide the ADC0GN value produced by 2 and write this value back into ADC0GN. Note that there is a lower limit for the input signal that can be applied during a system calibration because ADC0GN is only a 16-bit register. The input span (that is, the difference between the system zero-scale value and the system full-scale value) should be greater than 40% of the nominal full-scale input range (that is, >40% of VREF/gain).

The on-chip Flash/EE memory can be used to store multiple calibration coefficients. These calibration coefficients can be copied directly into the relevant calibration registers by user code and are based on the system configuration. In general, the simplest way to use the calibration registers is to let the ADC calculate the values required as part of the ADC automatic calibration modes.

A factory-programmed or end-of-line calibration for the I-ADC is a two-step procedure:

1. Apply 0 A current. Configure the ADC in the required PGA setting and write to ADCMDE[2:0] to perform a system zero-scale calibration. This writes a new offset calibration value into ADC0OF.

2. Apply a full-scale current for the selected PGA setting. Write to ADCMDE to perform a system full-scale calibration. This writes a new gain calibration value into ADC0GN.

OSC0TRM Register

Name: OSC0TRM

Address: 0xFFFF042C

Default Value: 0xX8

Access: Read/write

Function: This 8-bit register controls the low power oscillator trim.

Table 46. OSC0TRM MMR Bit Designations

Bit	Description
7 to 4	Reserved. Should be written as 0s.
3 to 0	User-defined trim bits.

OSC0CON Register

Name: OSC0CON

Address: 0xFFFF0440

Default Value: 0x00

Access: Read/write

Function: This 8-bit register controls the low power oscillator calibration routine.

Table 47. OSC0CON MMR Bit Designations

Bit	Description
7 to 5	Reserved. Should be written as 0.
4	Calibration source. Set to select external 32.768 kHz crystal. Cleared to select internal precision 131 kHz oscillator.
3	Calibration reset. Set to reset the calibration counters and disable the calibration logic. Cleared by user code after a calibration reset.
2	OSC0VAL1 reset. Set by user code to clear OSC0VAL1. Cleared by user code after an OSC0VAL1 reset.
1	OSC0VAL0 reset. Set by user code to clear OSC0VAL0. Cleared by user code after an OSC0VAL0 reset.
0	Calibration enable. Set to begin calibration. Cleared to abort calibration.

OSC0STA Register

Name: OSC0STA

Address: 0xFFFF0444

Default Value: 0x00

Access: Read access only

Function: This 8-bit register provides the status of the low power oscillator calibration routine.

Table 48. OSC0STA MMR Bit Designations

Bit	Description
7 to 2	Reserved.
1	Calibration complete. Set by hardware upon completion of a calibration cycle. Cleared by a read of OSC0VAL1.
0	Calibration busy. Set by hardware if calibration is in progress. Cleared by hardware if calibration is completed.

OSC0VAL0 Register

Name: OSC0VAL0

Address: 0xFFFF0448

Default Value: 0x00

Access: Read access only

Function: This 9-bit counter is clocked from either the 131 kHz precision oscillator or the 32.768 kHz external crystal.

OSC0VAL1 Register

Name: OSC0VAL1

Address: 0xFFFF044C

Default Value: 0x00

Access: Read access only

Function: This 10-bit counter is clocked from the low power 131 kHz oscillator.

TIMER2—WAKE-UP TIMER

Timer2 is a 32-bit wake-up up/down counter timer with a programmable prescaler. The prescaler is clocked directly from one of four clock sources, namely, the core clock (which is the default selection), the low power 32.768 kHz oscillator, the external 32.768 kHz watch crystal, or the precision 32.768 kHz oscillator. The selected clock source can be scaled by a factor of 1, 16, 256, or 32,768. The wake-up timer continues to run when the core clock is disabled. When the core is operating at 20.48 MHz and at CD = 0 with a prescaler of 1, a minimum resolution of 48.83 ns results.

The counter can be formatted as a plain 32-bit value or as time expressed as hours:minutes:seconds:hundredths.

Timer2 reloads the value from T2LD when Timer2 overflows.

The Timer2 interface consists of four MMRS.

- T2LD and T2VAL are 32-bit registers and hold 32-bit unsigned integers. T2VAL is a read only register.
- T2CLRI is an 8-bit register. Writing any value to this register clears the Timer2 interrupt.
- T2CON is a configuration MMR and is described in Table 54.

Timer2 Load Register

Name: T2LD

Address: 0xFFFF0340

Default Value: 0x00000000

Access: Read/write

Function: T2LD is a 32-bit register that holds the 32-bit value that is loaded into the counter.

Timer2 Clear Register

Name: T2CLRI

Address: 0xFFFF034C

Access: Write only

Function: This 8-bit, write only MMR is written (with any value) by user code to clear the interrupt.

Timer2 Value Register

Name: T2VAL

Address: 0xFFFF0344

Default Value: 0xFFFFFFFF

Access: Read only

Function: T2VAL is a 32-bit register that holds the current value of Timer2.

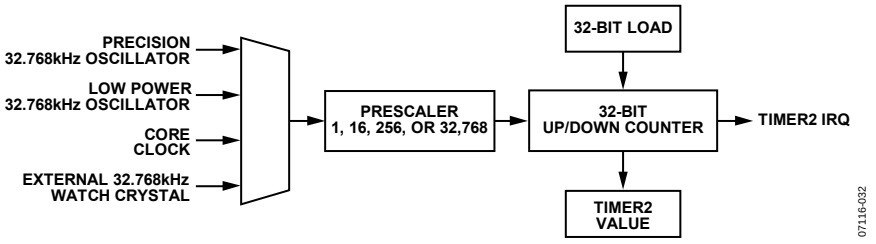

Figure 36. Timer2 Block Diagram

Timer3 Control Register

Name: T3CON

Address: 0xFFFF0368

Default Value: 0x0000

Access: Read/write

Function: This 16-bit MMR configures the mode of operation of Timer3 as described in Table 55.

Table 55. T3CON MMR Bit Designations

Bit	Description
15 to 9	Reserved. These bits are reserved and should be written as 0 by user code.
8	Count up/count down enable. Set by user code to configure Timer3 to count up. Cleared by user code to configure Timer3 to count down.
7	Timer3 enable. Set by user code to enable Timer3. Cleared by user code to disable Timer3.
6	Timer3 operating mode. Set by user code to configure Timer3 to operate in periodic mode. Cleared by user to configure Timer3 to operate in free running mode.
5	Watchdog timer mode enable. Set by user code to enable watchdog mode. Cleared by user code to disable watchdog mode.
4	Reserved. This bit is reserved and should be written as 0 by user code.
3 to 2	Timer3 clock (32.768 kHz) prescaler. 00 = source clock/1 (default). 01 = source clock/16. 10 = source clock/256. 11 = reserved.
1	Watchdog timer IRQ enable. Set by user code to produce an IRQ instead of a reset when the watchdog reaches 0. Cleared by user code to disable the IRQ option.
0	PD_OFF. Set by user code to stop Timer3 when the peripherals are powered down using Bit 4 in the POWCON MMR. Cleared by user code to enable Timer3 when the peripherals are powered down using Bit 4 in the POWCON MMR.

GENERAL-PURPOSE I/O

The ADuC7034 features nine general-purpose bidirectional input/output (GPIO) pins. In general, many of the GPIO pins have multiple functions that can be configured by user code. By default, the GPIO pins are configured in GPIO mode. All GPIO pins have an internal pull-up resistor with a sink capability of 0.8 mA and a source capability of 0.1 mA.

The nine GPIOs are grouped into three ports: Port0, Port1, and Port2. Port0 is five bits wide. Port1 and Port2 are each two bits wide. The GPIO assignment within each port is detailed in Table 57. A typical GPIO structure is shown Figure 39.

External interrupts are present on GPIO_0, GPIO_5, GPIO_7, and GPIO_8. These interrupts are level triggered and active high. Because these interrupts are not latched, the interrupt source must be present until either IRQSTA or FIQSTA are interrogated. The interrupt source must be active for at least one CD-divided core clock to guarantee recognition.

All port pins are configured and controlled by four sets (one set for each port) of four port-specific MMRs as follows:

- GPxCON: Portx control register
- GPxDAT: Portx configuration and data register
- GPxSET: Data set Portx
- GPxCLR: Data clear Portx

where x corresponds to the port number (0, 1, or 2).

During normal operation, user code can control the function and state of the external GPIO pins by these general-purpose registers. All GPIO pins retain their external level (high or low) during power-down (POWCON) mode.

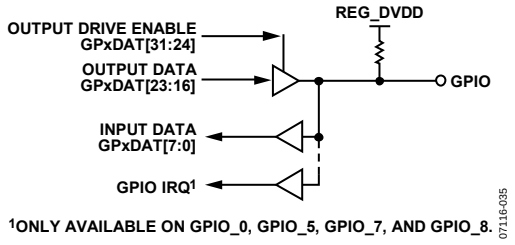

Figure 39. ADuC7034 GPIO

Table 57. External GPIO Pin to Internal Port Signal Assignments

Port	GPIO PIN	PORT SIGNAL	Functionality (Defined by GPxCON)
Port0	GPIO_0	P0.0	General-purpose I/O.
		IRQ0	External Interrupt Request 0
		$\overline{SS}$	Slave select I/O for SPI.
	GPIO_1	P0.1	General-purpose I/O.
		SCLK	Serial clock I/O for SPI.
	GPIO_2	P0.2	General-purpose I/O.
		MISO	Master input, slave output for SPI.
	GPIO_3	P0.3	General-purpose I/O.
		MOSI	Master output, slave input for SPI.
	GPIO_4	P0.4	General-purpose I/O
		ECLK	2.56 MHz clock output.
		P0.5[1]	High voltage serial interface.
		P0.6[1]	High voltage serial interface.
Port1	GPIO_5	P1.0	General-purpose I/O.
		IRQ1	External Interrupt Request 1
		RxD	Pin for UART.
	GPIO_6	P1.1	General-purpose I/O.
		TxD	Pin for UART.
Port2	GPIO_7	P2.0	General-purpose I/O.
		IRQ4	External Interrupt Request 4.
		LIN Output Pin.	Used to read directly from LIN pin for conformance testing.
	GPIO_8	P2.1	General-purpose I/O.
		IRQ5	External Interrupt Request 5.
		LIN HV Input Pin.	Used to directly drive LIN pin for conformance testing.
	GPIO_11[2]	P2.4[2]	General-purpose I/O.
		LINRX	LIN input pin.
	GPIO_12[2]	P2.5[2]	General-purpose I/O.
		LINTX	LIN output pin.
	GPIO_13[1]	P2.6[1]	General-purpose I/O, STI data output.

[1] These signals are internal signals only and do not appear on an external pin. These pins are used along with HVCON as the 2-wire interface to the high voltage interface circuits.
[2] These pins/signals are internal signals only and do not appear on an external pin. Both signals are used to provide external pin diagnostic write (GPIO_12) and readback (GPIO_11) capability.

GPIO Port2 Control Register

Name: GP2CON

Address: 0xFFFF0D08

Default Value: 0x01000000

Access: Read/write

Function: This 32-bit MMR selects the pin function for each Port2 pin.

Table 60. GP2CON MMR Bit Designations

Bit	Description
31 to 25	Reserved. These bits are reserved and should be written as 0 by user code.
24	GPIO_13 function select bit. Set to 1 by user code to route the STI data output to the STI pin. Cleared to 0 by user code, and then the STI data is not routed to the external STI pin even if the STI interface is enabled correctly.
23 to 21	Reserved. These bits are reserved and should be written as 0 by user code.
20	GPIO_12 function select bit. Set to 1 by user code to route the UART TxD (transmit data) to the LIN/BSD data pin. This configuration is used in LIN mode. Cleared to 0 by user code to route the LIN/BSD transmit data to an internal general-purpose I/O (GPIO_12) pad that can then be written via the GP2DAT MMR. This configuration is used in BSD mode to allow user code to write output data to the BSD interface, and it can also be used to support diagnostic write capability to the high voltage I/O pins (see HVCFG1[2:0]).
19 to 17	Reserved. These bits are reserved and should be written as 0 by user code.
16	GPIO_11 function select bit. Set to 1 by user code to route input data from the LIN/BSD interface to both the LIN/BSD hardware timing/synchronization logic and to the UART RxD (receive data). This mode must be configured by user code when using LIN or BSD modes. Cleared to 0 by user code to internally disable the LIN/BSD input data path. In this configuration, GPIO_11 is used to support diagnostic readback on all external high voltage I/O pins (see HVCFG1[2:0]).
15 to 5	Reserved. These bits are reserved and should be written as 0 by user code.
4	GPIO_8 function select bit. Set to 1 by user code to route the LIN/BSD input data to the GPIO_8 pin. This mode can be used to drive the LIN transceiver interface as a standalone component without any interaction from MCU or UART. Cleared to 0 by user code to configure the GPIO_8 pin as a general-purpose I/O (GPIO) pin.
3 to 1	Reserved. These bits are reserved and should be written as 0 by user code.
0	GPIO_7 function select bit. Set to 1 by user code to route data driven into the GPIO_7 pin through the on-chip LIN transceiver to be output at the LIN/BSD pin. This mode can be used to drive the LIN transceiver interface as a standalone component without any interaction from MCU or UART. Cleared to 0 by user code to configure the GPIO_7 pin as a general-purpose I/O (GPIO) pin.

GPIO Port0 Data Register

Name: GP0DAT

Address: 0xFFFF0D20

Default Value: 0x000000XX

Access: Read/write

Function: This 32-bit MMR configures the direction of the GPIO pins assigned to Port0 (see Table 57). This register also sets the output value for GPIO pins configured as outputs and reads the status of GPIO pins configured as inputs.

Table 61. GP0DAT MMR Bit Designations

Bit	Description
31 to 29	Reserved. These bits are reserved and should be written as 0 by user code.
28	Port0.4 direction select bit. Set to 1 by user code to configure the GPIO pin assigned to Port0.4 as an output. Cleared to 0 by user code to configure the GPIO pin assigned to Port0.4 as an input.
27	Port0.3 direction select bit. Set to 1 by user code to configure the GPIO pin assigned to Port0.3 as an output. Cleared to 0 by user code to configure the GPIO pin assigned to Port0.3 as an input.
26	Port0.2 direction select bit. Set to 1 by user code to configure the GPIO pin assigned to Port0.2 as an output. Cleared to 0 by user code to configure the GPIO pin assigned to Port0.2 as an input.
25	Port0.1 direction select bit. Set to 1 by user code to configure the GPIO pin assigned to Port0.1 as an output. Cleared to 0 by user code to configure the GPIO pin assigned to Port0.1 as an input.
24	Port0.0 direction select bit. Set to 1 by user code to configure the GPIO pin assigned to Port0.0 as an output. Cleared to 0 by user code to configure the GPIO pin assigned to Port0.0 as an input.
23 to 21	Reserved. These bits are reserved and should be written as 0 by user code.
20	Port0.4 data output. The value written to this bit appears directly on the GPIO pin assigned to Port0.4.
19	Port0.3 data output. The value written to this bit appears directly on the GPIO pin assigned to Port0.3.
18	Port0.2 data output. The value written to this bit appears directly on the GPIO pin assigned to Port0.2.
17	Port0.1 data output. The value written to this bit appears directly on the GPIO pin assigned to Port0.1.
16	Port0.0 data output. The value written to this bit appears directly on the GPIO pin assigned to Port0.0.
15 to 5	Reserved. These bits are reserved and should be written as 0 by user code.
4	Port0.4 data input. This bit is a read only bit that reflects the current status of the GPIO pin assigned to Port0.4. User code should write 0 to this bit.
3	Port0.3 data input. This bit is a read only bit that reflects the current status of the GPIO pin assigned to Port0.3. User code should write 0 to this bit.
2	Port0.2 data input. This bit is a read only bit that reflects the current status of the GPIO pin assigned to Port0.2. User code should write 0 to this bit.
1	Port0.1 data input. This bit is a read only bit that reflects the current status of the GPIO pin assigned to Port0.1. User code should write 0 to this bit.
0	Port0.0 data input. This bit is a read only bit that reflects the current status of the GPIO pin assigned to Port0.0. User code should write 0 to this bit.

GPIO Port0 Set Register

Name: GP0SET

Address: 0xFFFF0D24

Access: Write only

Function: This 32-bit MMR allows user code to individually bit-address external GPIO pins to set them high only. User code can accomplish this using the GP0SET MMR without having to modify or maintain the status of the GPIO pins (as user code requires when using GP0DAT).

Table 64. GP0SET MMR Bit Designations

Bit	Description
31 to 21	Reserved. These bits are reserved and should be written as 0 by user code.
20	Port0.4 set bit. Set to 1 by user code to set the external GPIO_4 pin high. Clearing this bit to 0 via user software has no effect on the external GPIO_4 pin.
19	Port0.3 set bit. Set to 1 by user code to set the external GPIO_3 pin high. Clearing this bit to 0 via user software has no effect on the external GPIO_3 pin.
18	Port0.2 set bit. Set to 1 by user code to set the external GPIO_2 pin high. Clearing this bit to 0 via user software has no effect on the external GPIO_2 pin.
17	Port0.1 set bit. Set to 1 by user code to set the external GPIO_1 pin high. Clearing this bit to 0 via user software has no effect on the external GPIO_1 pin.
16	Port0.0 set bit. Set to 1 by user code to set the external GPIO_0 pin high. Clearing this bit to 0 via user software has no effect on the external GPIO_0 pin.
15 to 0	Reserved. These bits are reserved and should be written as 0 by user code.

GPIO Port1 Set Register

Name: GP1SET

Address: 0xFFFF0D34

Access: Write only

Function: This 32-bit MMR allows user code to individually bit-address external GPIO pins to set them high only. User code can accomplish this using the GP1SET MMR without having to modify or maintain the status of the GPIO pins (as user code requires when using GP1DAT).

Table 65. GP1SET MMR Bit Designations

Bit	Description
31 to 18	Reserved. These bits are reserved and should be written as 0 by user code.
17	Port1.1 set bit. Set to 1 by user code to set the external GPIO_6 pin high. Clearing this bit to 0 via user software has no effect on the external GPIO_6 pin.
16	Port1.0 set bit. Set to 1 by user code to set the external GPIO_5 pin high. Clearing this bit to 0 via user software has no effect on the external GPIO_5 pin.
15 to 0	Reserved. These bits are reserved and should be written as 0 by user code.

HIGH VOLTAGE PERIPHERAL CONTROL INTERFACE

The ADuC7034 integrates several high voltage circuit functions that are controlled and monitored through a registered interface consisting of two MMRs, namely, HVCON and HVDAT. The HVCON register acts as a command byte interpreter, allowing the microcontroller to indirectly read or write 8-bit data (the value in HVDAT) from or to one of four high voltage status or configuration registers. These high voltage status and configuration registers are not MMRs but are registers commonly referred to as indirect registers, that is, they can only be accessed (as the name suggests) indirectly via the HVCON and HVDAT MMRs.

The physical interface between the HVCON register and the indirect high voltage registers is a 2-wire (data and clock) serial interface based on a 2.56 MHz serial clock. Therefore, there is a finite 10 µs (maximum) latency between the MCU core writing a command into HVCON and the command or data reaching the indirect high voltage registers. There is also a finite 10 µs latency between the MCU core writing a command into HVCON and the indirect register data being read back into the HVDAT register. A busy bit (for example, Bit 0 of the HVCON when read by MCU) can be polled by the MCU to confirm when a read/write command is complete.

The following high voltage circuit functions are controlled and monitored via this interface. Figure 40 shows the top-level architecture of the high voltage interface and the following related circuits:

- Precision oscillator
- Wake-up (WU) pin functionality
- Power supply monitor (PSM)
- Low voltage flag (LVF)
- LIN operating modes
- STI diagnostics
- High voltage diagnostics
- High voltage attenuator-buffer circuit
- High voltage (HV) temperature monitor

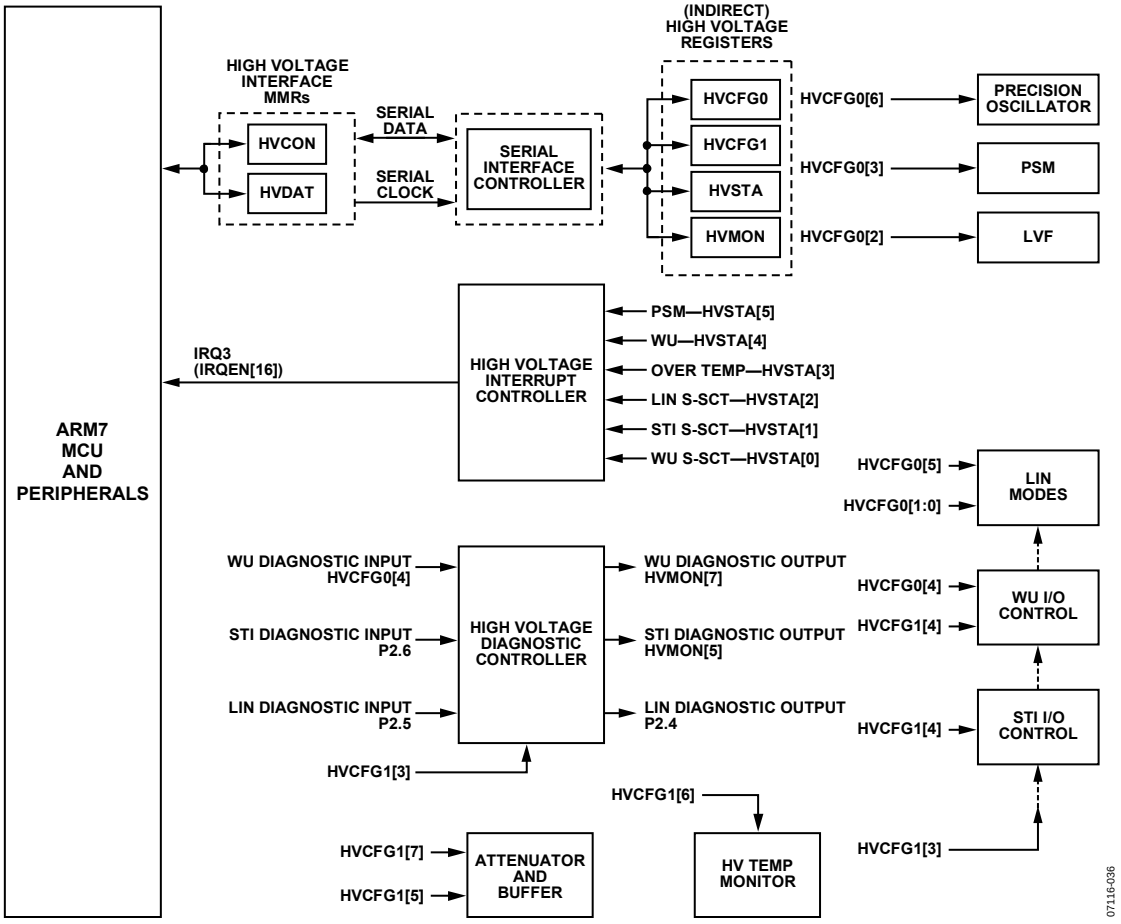

Figure 40. High Voltage Interface, Top-Level Block Diagram

UART REGISTER DEFINITION

The UART interface consists of the following nine registers:

- COMTX: 8-bit transmit register
- COMRX: 8-bit receive register
- COMDIV0: divisor latch (low byte)
- COMDIV1: divisor latch (high byte)
- COMCON0: line control register
- COMSTA0: line status register
- COMIEN0: interrupt enable register
- COMIID0: interrupt identification register
- COMDIV2: 16-bit fractional baud divider register

COMTX, COMRX, and COMDIV0 share the same address location. COMTX and COMRX can be accessed when Bit 7 in the COMCON0 register is cleared, and COMDIV0 can be accessed when Bit 7 of COMCON0 is set.

UART TX Register

Name: COMTX

Address: 0xFFFF0700

Access: Write only

Function: Write to this 8-bit register to transmit data using the UART.

UART RX Register

Name: COMRX

Address: 0xFFFF0700

Default Value: 0x00

Access: Read only

Function: This 8-bit register is read from to receive data transmitted using the UART.

UART Divisor Latch Register 0

Name: COMDIV0

Address: 0xFFFF0700

Default Value: 0x00

Access: Read/write

Function: This 8-bit register contains the LSB of the divisor latch that controls the baud rate at which the UART operates.

UART Divisor Latch Register 1

Name: COMDIV1

Address: 0xFFFF0704

Default Value: 0x00

Access: Read/write

Function: This 8-bit register contains the MSB of the divisor latch that controls the baud rate at which the UART operates.

UART Control Register 0

Name: COMCON0

Address: 0xFFFF070C

Default Value: 0x00

Access: Read/write

Function: This 8-bit register controls the operation of the UART in conjunction with COMCON1.

UART Interrupt Enable Register 0

Name: COMIEN0

Address: 0xFFFF0704

Default Value: 0x00

Access: Read/write

Function: The 8-bit register enables and disables the individual UART interrupt sources.

Table 83. COMIEN0 MMR Bit Designations

Bit	Name	Description
7 to 4	N/A	Reserved. Not used.
3	N/A	Reserved. This bit should be written as 0.
2	ELSI	RxD status interrupt enable bit. Set by the user to enable generation of an interrupt if any of the COMSTA0[3:1] register bits are set. Cleared by the user.
1	ETBEI	Enable transmit buffer empty interrupt. Set by the user to enable an interrupt when the buffer is empty during a transmission, that is, when COMSTA[5] is set. Cleared by the user.
0	ERBFI	Enable receive buffer full interrupt. Set by the user to enable an interrupt when the buffer is full during a reception. Cleared by the user.

UART Interrupt Identification Register 0

Name: COMIID0

Address: 0xFFFF0708

Default Value: 0x01

Access: Read only

Function: This 8-bit register reflects the source of the UART interrupt.

Table 84. COMIID0 MMR Bit Designations

Bits[2:1] Status Bits	Bit 0 NINT	Priority	Description	Clearing Operation
00	1	N/A	No interrupt	N/A
11	0	1	Receive line status interrupt	Read COMSTA0
10	0	2	Receive buffer full interrupt	Read COMRX
01	0	3	Transmit buffer empty interrupt	Write data to COMTX or read COMIID0
00	0	4	Modem status interrupt	Read COMSTA1 register

SPI Status Register

Name: SPISTA

Address: 0xFFFF0A00

Default Value: 0x00

Access: Read only

Function: The 8-bit MMR represents the current status of the serial peripheral interface.

Table 89. SPISTA MMR Bit Designations

Bit	Description
7 to 6	Reserved.
5	SPIRX data register overflow status bit. Set if SPIRX is overflowing. Cleared by reading the SPIRX register.
4	SPIRX data register IRQ. Set automatically if Bit 3 or Bit 5 is set. Cleared by reading the SPIRX register.
3	SPIRX data register full status bit. Set automatically if valid data is present in the SPIRX register. Cleared by reading the SPIRX register.
2	SPITX data register underflow status bit. Set automatically if SPITX is underflowing. Cleared by writing in the SPITX register.
1	SPITX data register IRQ. Set automatically if Bit 0 is cleared or Bit 2 is set. Cleared by either writing in the SPITX register or, if the transmission is finished, by disabling the SPI.
0	SPITX data register empty status bit. Set by writing to SPITX to send data. This bit is set during transmission of data. Cleared when SPITX is empty.

LIN Hardware Synchronization Status Register

Name: LHSSTA

Address: 0xFFFF0780

Default Value: 0x00

Access: Read only

Function: The LHS status register is an 8-bit register whose bits reflect the current operating status of the LIN interface.

Table 91. LHSSTA MMR Bit Designations

Bit	Description
7	Reserved. These read only bits are reserved for future use.
6	Rising edge detected (BSD mode only). Set to 1 by hardware to indicate a rising edge has been detected on the BSD bus. Cleared to 0 after user code reads the LHSSTA MMR.
5	LHS reset complete flag. Set to 1 by hardware to indicate a LHS reset command has completed successfully. Cleared to 0, after user code reads the LHSSTA MMR.
4	Break field error. Set to 1 by hardware and generates an LHS interrupt (IRQEN[7]) when the 12-bit break timer (LHSVAL1) register overflows to indicate the LIN bus has stayed low too long, thus suggesting a possible LIN bus error. Cleared to 0 after user code reads the LHSSTA MMR.
3	LHS compare interrupt. Set to 1 by hardware when the value in LHSVAL0 (LIN synchronization bit timer) equals the value in the LHSCMP register. Cleared to 0 after user code reads the LHSSTA MMR.
2	Stop condition interrupt. Set to 1 by hardware when a stop condition is detected. Cleared to 0 after user code reads LHSSTA MMR.
1	Start condition interrupt. Set to 1 by hardware when a start condition is detected. Cleared to 0 after user code reads LHSSTA MMR.
0	Break timer compare interrupt. Set to 1 by hardware when a valid LIN break condition is detected. A LIN break condition is generated when the LIN break timer value reaches the break timer compare value (see LHSVAL1 in the LIN Hardware Break Timer1 Register section for more information). Cleared to 0 after user code reads the LHSSTA MMR.

Bit	Description
6	Mode of operation bit. Set to 1 by user code to select BSD mode of operation. Cleared to 0 by user code to select LIN mode of operation.
5	Enable compare interrupt bit. Set to 1 by user code to generate an LHS interrupt (IRQEN[7]) when the value in LHSVAL0 (the LIN synchronization bit timer) equals the value in the LHSCMP register. The LHS compare interrupt bit (LHSSTA[3]) is set when this interrupt occurs. This configuration is used in BSD write mode to allow user code to correctly time the output pulse widths of BSD bits to be transmitted. Cleared to 0 by user code to disable compare interrupts.
4	Enable stop interrupt. Set to 1 by user code to generate an interrupt when a stop condition occurs. Cleared to 0 by user code to disable interrupts when a stop condition occurs.
3	Enable start interrupt. Set to 1 by user code to generate an interrupt when a start condition occurs. Cleared to 0 by user code to disable interrupts when a start condition occurs.
2	LIN sync enable bit. Set to 1 by user code to enable LHS functionality. Cleared to 0 by user code to disable LHS functionality.
1	Edge counter clear bit. Set to 1 by user code to clear the internal edge counters in the LHS peripheral. Cleared automatically to 0 after a 15 µs delay.
0	LHS reset bit. Set to 1 by user code to reset all LHS logic to default conditions. Cleared automatically to 0 after a 15 µs delay.

[1] In BSD mode, LHSCON0[6] is set to 1. Because of the finite propagation delay in the BSD transmit (from the MCU to the external pin) and receive (from the external pin to the MCU) paths, user code must not switch between BSD write and read modes until the MCU confirms that the external BSD pin is deasserted. Failure to adhere to this recommendation can result in the generation of an inadvertent break condition interrupt after user code switches from BSD write mode to BSD read mode. A stop condition interrupt can be used to ensure that this scenario is avoided.

LIN Hardware Synchronization Control Register 1

Name: LHSCON1

Address: 0xFFFF078C

Default Value: 0x32

Access: Read/write

Function: The LHS control register is an 8-bit register that is used in conjunction with the LHSCON0 register to configure the LIN mode of operation.

Table 93. LHSCON1 MMR Bit Designations

Bit	Description
7 to 4	LIN stop edge count. These bits are set by user code to the number of falling or rising edges on which to stop the internal LIN synchronization counter. The stop value of this counter can be read by user code via LHSVAL0. The type of edge, either rising or falling, is configured by LHSCON0[7]. The default value of these bits is 0x3, which configures the hardware to stop counting on the third falling edge. It should be noted that the first falling edge is considered to be the falling edge at the start of the LIN break pulse.
3 to 0	LIN start edge count. These four bits are set by user code to the number of falling edges that must occur before the internal LIN synchronization timer starts counting. The stop value of this counter can be read by user code via LHSVAL0. The default value of these bits is 0x2, which configures the hardware to start counting on the second falling edge. Note that the first falling edge is considered to be the falling edge at the start of the LIN break pulse.