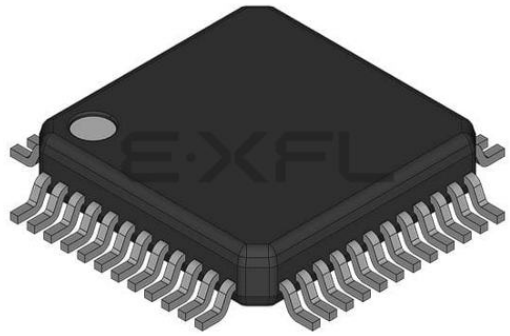

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	40MHz
Connectivity	SCI, SPI
Peripherals	POR, WDT
Number of I/O	21
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	2.25V ~ 3.6V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc56f8122vfae

1.1.5 Energy Information

- Fabricated in high-density CMOS with 5V-tolerant, TTL-compatible digital inputs
- On-board 3.3V down to 2.6V voltage regulator for powering internal logic and memories
- On-chip regulators for digital and analog circuitry to lower cost and reduce noise
- Wait and Stop modes available
- ADC smart power management
- Each peripheral can be individually disabled to save power

1.2 Device Description

The 56F8322 and 56F8122 are members of the 56800E core-based family of controllers. Each combines, on a single chip, the processing power of a Digital Signal Processor (DSP) and the functionality of a microcontroller with a flexible set of peripherals to create an extremely cost-effective solution. Because of their low cost, configuration flexibility, and compact program code, the 56F8322 and 56F8122 are well-suited for many applications. These devices include many peripherals that are especially useful for *automotive* control (56F8322 only); industrial control and networking; motion control; home appliances; general purpose inverters; smart sensors; fire and security systems; power management; and medical monitoring applications.

The 56800E core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The MCU-style programming model and optimized instruction set allow straightforward generation of efficient, compact DSP and control code. The instruction set is also highly efficient for C Compilers to enable rapid development of optimized control applications.

The 56F8322 and 56F8122 support program execution from internal memories. Two data operands can be accessed from the on-chip data RAM per instruction cycle. These devices also provide one external dedicated interrupt line and up to 21 General Purpose Input/Output (GPIO) lines, depending on peripheral configuration.

1.2.1 56F8322 Features

The 56F8322 controller includes 32KB of Program Flash and 8KB of Data Flash, each programmable through the JTAG port, and 4KB of Program RAM and 8KB of Data RAM. A total of 8KB of Boot Flash is incorporated for easy customer inclusion of field-programmable software routines that can be used to program the main Program and Data Flash memory areas. Both Program and Data Flash memories can be independently bulk erased or erased in pages. Program Flash page erase size is 1KB. Boot and Data Flash page erase size is 512 bytes. The Boot Flash memory can also be either bulk or page erased.

A key application-specific feature of the 56F8322 is the inclusion of one Pulse Width Modulator (PWM) module. This module incorporates three complementary, individually programmable PWM signal output pairs and is also capable of supporting six independent PWM functions to enhance motor control functionality. Complementary operation permits programmable dead time insertion, distortion correction via current sensing by software, and separate top and bottom output polarity control. The up-counter value

1.4 Architecture Block Diagram

Note: *Features in italics are NOT available in the 56F8122 device and are shaded in the following figures.*

The 56F8322/56F8122 architecture is shown in **Figure 1-1** and **Figure 1-2**. **Figure 1-1** illustrates how the 56800E system buses communicate with internal memories and the IPBus Bridge. **Table 1-2** lists the internal buses in the 56800E architecture and provides a brief description of their function. **Figure 1-2** shows the peripherals and control blocks connected to the IPBus Bridge. The figures do not show the on-board regulator and power and ground signals. They also do not show the multiplexing between peripherals or the dedicated GPIOs. Please see **Part 2 Signal/Connection Descriptions**, to see which signals are multiplexed with those of other peripherals.

Also shown in **Figure 1-2** are connections between the *PWM*, Timer C and ADC blocks. These connections allow the *PWM and/or* Timer C to control the timing of the start of ADC conversions. The Timer C, Channel 2, output can generate periodic start (SYNC) signals to the ADC to start its conversions. *In another operating mode, the PWM load interrupt (SYNC output) signal is routed internally to the Timer C, Channel 2, input as indicated. The timer can then be used to introduce a controllable delay before generating its output signal. The timer output then triggers the ADC.* To fully understand this interaction, please see the **56F8300 Peripheral User Manual** for clarification on the operation of all three of these peripherals.

Table 2-2 Signal and Package Information for the 48-Pin LQFP (Continued)

Signal Name	Pin No.	Type	State During Reset	Signal Description
PHASEA0	38	Schmitt Input	Input, pull-up enabled	**Phase A** — Quadrature Decoder 0, PHASEA input
(TA0)		Schmitt Input/ Output		**TA0** — Timer A, Channel 0
(GPIOB7)		Schmitt Input/ Output		**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(oscillator_ clock)		Output		**Clock Output** - can be used to monitor the internal oscillator clock signal (see **Section 6.5.7** CLKO Select Register, SIM_CLKOSR). In the 56F8322, the default state after reset is PHASEA0. In the 56F8122, the default state is not one of the functions offered and must be reconfigured.
PHASEB0	37	Schmitt Input	Input, pull-up enabled	**Phase B** — Quadrature Decoder 0, PHASEB input
(TA1)		Schmitt Input/ Output		**TA1** — Timer A ,Channel 1
(GPIOB6)		Schmitt Input/ Output		**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(SYS_CLK2)		Output		**Clock Output** - can be used to monitor the internal SYS_CLK2 signal (see **Section 6.5.7** CLKO Select Register, SIM_CLKOSR). In the 56F8322, the default state after reset is PHASEB0. In the 56F8122, the default state is not one of the functions offered and must be reconfigured.

Table 2-2 Signal and Package Information for the 48-Pin LQFP (Continued)

Signal Name	Pin No.	Type	State During Reset	Signal Description
PWMA4 **(MOSI1)** **(GPIOA4)**	8	Output Schmitt Input/ Output Schmitt Input/ Output	In reset, output is disabled, pull-up is enabled	**PWMA4** — This is one of six PWMA output pins. **SPI 1 Master Out/Slave In** — This serial data pin is an output from a master device and an input to a slave device. The master device places data on the MOSI line a half-cycle before the clock edge the slave device uses to latch the data. **Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin. In the 56F8322, the default state after reset is PWMA4. In the 56F8122, the default state is not one of the functions offered and must be reconfigured.
PWMA5 **(SCLK1)** **(GPIOA5)**	9	Output Schmitt Input/ Output Schmitt Input/ Output	In reset, output is disabled, pull-up is enabled	**PWMA5** — This is one of six PWMA output pins. **SPI 1 Serial Clock** — In the master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input. A Schmitt trigger input is used for noise immunity. **Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin. In the 56F8322, the default state after reset is PWMA5. In the 56F8122, the default state is not one of the functions offered and must be reconfigured.
FAULTA0 **(GPIOA6)**	12	Schmitt Input Schmitt Input/ Output	Input	**FAULTA0** — This fault input pin is used for disabling selected PWMA outputs in cases where fault conditions originate off-chip. **Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin. In the 56F8322, the default state after reset is FAULTA0. In the 56F8122, the default state is not one of the functions offered and must be reconfigured.
ANA0	20	Input	Analog Input	**ANA0 - 2** — Analog inputs to ADCA, Channel 0
ANA1	21			
ANA2	22			
ANA4	23	Input	Analog Input	**ANA4 - 6** — Analog inputs to ADCA, Channel 1
ANA5	24			
ANA6	25			

3.3 Use of On-Chip Relaxation Oscillator

An internal relaxtion oscillator can supply the reference frequency when an external frequency source of crystal is not used. During a boot or reset sequence, the relaxation oscillator is enabled by default, and the PRECS bit in the PLLCR word is set to 0. If an external oscillator is connected, the relaxation oscillator can be deselected instead by setting the PRECS bit in the PLLCR to 1. If a changeover between internal and external oscillators is required at start up, internal device circuits compensate for any asynchronous transitions between the two clock signals so that no glitches occur in the resulting master clock to the chip. When changing clocks, the user must ensure that the clock source is not switched until the desired clock is enabled and stable.

To compensate for variances in the device manufacturing process, the accuracy of the relaxation oscillator can be incrementally adjusted to within $\pm$ 0.1% of 8MHz by trimming an internal capacitor. Bits 0-9 of the OSCTL (oscillator control) register allow the user to set in an additional offset (trim) to this preset value to increase or decrease capacitance. Upon power-up, the default value of this trim is 512 units. Each unit added or deleted changes the output frequency by about 0.1%, allowing incremental adjustment until the desired frequency accuracy is achieved.

The internal oscillator is calibrated at the factory to 8MHz and the TRIM value is stored in the Flash information block and loaded to the FMOPT1 register at reset. When using the relaxation oscillator, the boot code should read the FMOPT1 register and set this value as OSCTL TRIM. For further information, see the **56F8300 Peripheral User Manual**.

3.4 Internal Clock Operation

At reset, both oscillators will be powered up; however, the relaxation oscillator will be the default clock reference for the PLL. Software should power down the block not being used and program the PLL for the correct frequency.

Table 4-8 Quad Timer A Registers Address Map (Continued) (TMRA_BASE = $00 F040)

Register Acronym	Address Offset	Register Description
TMRA0_CMPLD2	$9	Comparator Load Register 2
TMRA0_COMSCR	$A	Comparator Status and Control Register
		Reserved
TMRA1_CMP1	$10	Compare Register 1
TMRA1_CMP2	$11	Compare Register 2
TMRA1_CAP	$12	Capture Register
TMRA1_LOAD	$13	Load Register
TMRA1_HOLD	$14	Hold Register
TMRA1_CNTR	$15	Counter Register
TMRA1_CTRL	$16	Control Register
TMRA1_SCR	$17	Status and Control Register
TMRA1_CMPLD1	$18	Comparator Load Register 1
TMRA1_CMPLD2	$19	Comparator Load Register 2
TMRA1_COMSCR	$1A	Comparator Status and Control Register
		Reserved
TMRA2_CMP1	$20	Compare Register 1
TMRA2_CMP2	$21	Compare Register 2
TMRA2_CAP	$22	Capture Register
TMRA2_LOAD	$23	Load Register
TMRA2_HOLD	$24	Hold Register
TMRA2_CNTR	$25	Counter Register
TMRA2_CTRL	$26	Control Register
TMRA2_SCR	$27	Status and Control Register
TMRA2_CMPLD1	$28	Comparator Load Register 1
TMRA2_CMPLD2	$29	Comparator Load Register 2
TMRA2_COMSCR	$2A	Comparator Status and Control Register
		Reserved
TMRA3_CMP1	$30	Compare Register 1
TMRA3_CMP2	$31	Compare Register 2
TMRA3_CAP	$32	Capture Register
TMRA3_LOAD	$33	Load Register
TMRA3_HOLD	$34	Hold Register
TMRA3_CNTR	$35	Counter Register
TMRA3_CTRL	$36	Control Register
TMRA3_SCR	$37	Status and Control Register
TMRA3_CMPLD1	$38	Comparator Load Register 1
TMRA3_CMPLD2	$39	Comparator Load Register 2
TMRA3_COMSCR	$3A	Comparator Status and Control Register

Table 4-12 Interrupt Control Registers Address Map (Continued) (ITCN_BASE = $00 F1A0)

Register Acronym	Address Offset	Register Description
IRQP 0	$11	IRQ Pending Register 0
IRQP 1	$12	IRQ Pending Register 1
IRQP 2	$13	IRQ Pending Register 2
IRQP 3	$14	IRQ Pending Register 3
IRQP 4	$15	IRQ Pending Register 4
IRQP 5	$16	IRQ Pending Register 5
		Reserved
ICTL	$1D	Interrupt Control Register

Table 4-13 Analog to Digital Converter Registers Address Map (ADCA_BASE = $00 F200)

Register Acronym	Address Offset	Register Description
ADCA_CR1	$0	Control Register 1
ADCA_CR2	$1	Control Register 2
ADCA_ZCC	$2	Zero Crossing Control Register
ADCA_LST 1	$3	Channel List Register 1
ADCA_LST 2	$4	Channel List Register 2
ADCA_SDIS	$5	Sample Disable Register
ADCA_STAT	$6	Status Register
ADCA_LSTAT	$7	Limit Status Register
ADCA_ZCSTAT	$8	Zero Crossing Status Register
ADCA_RSLT 0	$9	Result Register 0
ADCA_RSLT 1	$A	Result Register 1
ADCA_RSLT 2	$B	Result Register 2
ADCA_RSLT 3	$C	Result Register 3
ADCA_RSLT 4	$D	Result Register 4
ADCA_RSLT 5	$E	Result Register 5
ADCA_RSLT 6	$F	Result Register 6
ADCA_RSLT 7	$10	Result Register 7
ADCA_LLMT 0	$11	Low Limit Register 0
ADCA_LLMT 1	$12	Low Limit Register 1
ADCA_LLMT 2	$13	Low Limit Register 2
ADCA_LLMT 3	$14	Low Limit Register 3
ADCA_LLMT 4	$15	Low Limit Register 4
ADCA_LLMT 5	$16	Low Limit Register 5
ADCA_LLMT 6	$17	Low Limit Register 6
ADCA_LLMT 7	$18	Low Limit Register 7
ADCA_HLMT 0	$19	High Limit Register 0

5.4 Block Diagram

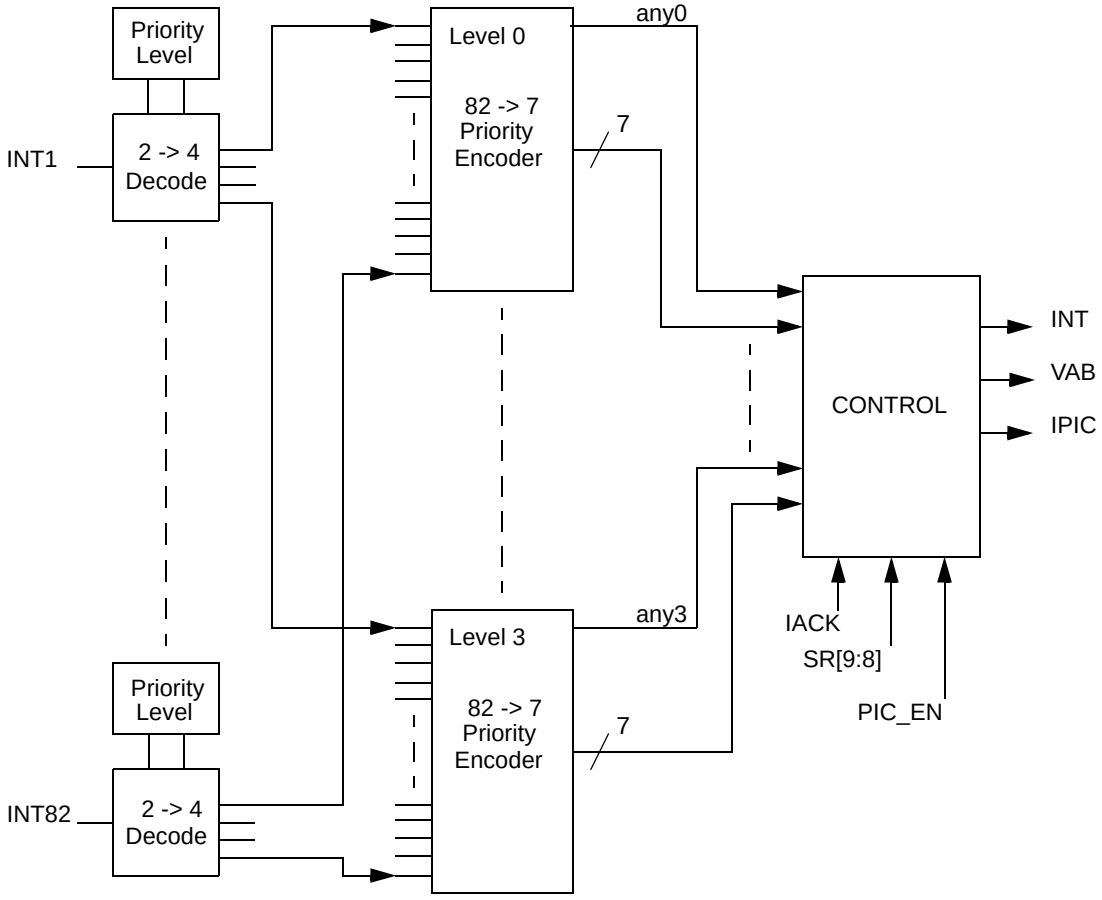


Figure 5-1 Interrupt Controller Block Diagram

5.5 Operating Modes

The ITCN module design contains two major modes of operation:

- **Functional Mode**
  The ITCN is in this mode by default.
- **Wait and Stop Modes**
  During Wait and Stop modes, the system clocks and the 56800E core are turned off. The ITCN will signal a pending IRQ to the System Integration Module (SIM) to restart the clocks and service the IRQ. An IRQ can only wake up the core if the IRQ is enabled prior to entering the Wait or Stop mode. Also, the IRQA signal automatically becomes low-level sensitive in these modes, even if the control register bits are set to make them falling-edge sensitive. This is because there is no clock available to detect the falling edge.

  A peripheral which requires a clock to generate interrupts will not be able to generate interrupts during Stop mode. The FlexCAN module can wake the device from Stop mode, and a reset will do just that, or IRQA and IRQB can wake it up.

5.6.2.1 Reserved—Bits 15–6

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.2.2 EOnCE Receive Register Full Interrupt Priority Level (RX_REG IPL)—Bits 5–4

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.2.3 EOnCE Transmit Register Empty Interrupt Priority Level (TX_REG IPL)—Bits 3–2

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.2.4 EOnCE Trace Buffer Interrupt Priority Level (TRBUF IPL)—Bits 1–0

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.3 Interrupt Priority Register 2 (IPR2)

Base + $2	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	FMCBE IPL		FMCC IPL		FMERR IPL		LOCK IPL		LVI IPL		0	0	0	0	IRQA IPL	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-5 Interrupt Priority Register 2 (IPR2)

5.7 Resets

5.7.1 Reset Handshake Timing

The ITCN provides the 56800E core with a reset vector address whenever $\overline{\text{RESET}}$ is asserted. The reset vector will be presented until the second rising clock edge after $\overline{\text{RESET}}$ is released.

5.7.2 ITCN After Reset

After reset, all of the ITCN registers are in their default states. This means all interrupts are disabled, except the core IRQs with fixed priorities:

- Illegal Instruction
- SW Interrupt 3
- HW Stack Overflow
- Misaligned Long Word Access
- SW Interrupt 2
- SW Interrupt 1
- SW Interrupt 0
- SW Interrupt LP

These interrupts are enabled at their fixed priority levels.

Part 6 System Integration Module (SIM)

6.1 Introduction

The SIM module is a system catchall for the glue logic that ties together the system-on-chip. It controls distribution of resets and clocks and provides a number of control features. The system integration module is responsible for the following functions:

- Reset sequencing
- Clock control & distribution
- Stop/Wait control
- Pull-up enables for selected peripherals
- System status registers
- Registers for software access to the JTAG ID of the chip
- Enforcing Flash security

These are discussed in more detail in the sections that follow.

6.5.4 Most Significant Half of JTAG ID (SIM_MSH_ID)

This read-only register displays the most significant half of the JTAG ID for the chip. This register reads $01F4.

Base + $6	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0
Write																
RESET	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0

Figure 6-6 Most Significant Half of JTAG ID (SIM_MSH_ID)

6.5.5 Least Significant Half of JTAG ID (SIM_LSH_ID)

This read-only register displays the least significant half of the JTAG ID for the chip. This register reads $001D.

Base + $7	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1

Figure 6-7 Least Significant Half of JTAG ID (SIM_LSH_ID)

6.5.6 SIM Pull-up Disable Register (SIM_PUDR)

Most of the pins on the chip have on-chip pull-up resistors. Pins which can operate as GPIO can have these resistors disabled via the GPIO function. Non-GPIO pins can have their pull-ups disabled by setting the appropriate bit in this register. Disabling pull-ups is done on a peripheral-by-peripheral basis (for pins not muxed with GPIO). Each bit in the register (see **Figure 6-8**) corresponds to a functional group of pins. See **Table 2-2** to identify which pins can deactivate the internal pull-up resistor.

Base + $8	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	$\overline{\text{RESET}}$	IRQ	0	0	0	0	0	0	JTAG	0	0	0
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-8 SIM Pull-up Disable Register (SIM_PUDR)

6.5.6.1 Reserved—Bits 15–12

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.6.2 $\overline{\text{RESET}}$—Bit 11

This bit controls the pull-up resistors on the $\overline{\text{RESET}}$ pin.

6.5.6.3 IRQ—Bit 10

This bit controls the pull-up resistors on the $\overline{\text{IRQA}}$ pin.

6.5.6.4 Reserved—Bits 9–4

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.6.5 JTAG—Bit 3

This bit controls the pull-up resistors on the $\overline{\text{TRST}}$ (This pin is always tied inactive on the 56F8322), TMS and TDI pins.

6.5.6.6 Reserved—Bits 2–0

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.7 CLKO Select Register (SIM_CLKOSR)

The CLKO select register can be used to multiplex out any one of the clocks generated inside the clock generation and SIM modules. The default value is SYS_CLK. All other clocks primarily muxed out are for test purposes only, and are subject to significant unspecified latencies at high frequencies.

The upper four bits of the GPIOB register can function as GPIO, Quad Decoder #0 signals, or as additional clock output signals. GPIO has priority and is enabled/disabled via the GPIOB_PER. If GPIOB[7:4] are programmed to operate as peripheral outputs, then the choice between Quad Decoder #0 and additional clock outputs is made here in the CLKOSR. The default state is for the peripheral function of GPIOB[7:4] to be programmed as Quad Decoder #0. This can be changed by altering $\overline{\text{PHASE0}}$ through $\overline{\text{INDEX}}$ as shown in **Figure 6-9**.

The CLKOUT pin is not bonded out in this device. Instead, it is offered only as a pad for die-level testing.

Base + $A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	$\overline{\text{PHSA}}$	$\overline{\text{PHSB}}$	$\overline{\text{INDEX}}$	$\overline{\text{HOME}}$	CLK DIS	CLKOSEL				
Write																
RESET	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Figure 6-9 CLKO Select Register (SIM_CLKOSR)

6.5.7.1 Reserved—Bits 15–10

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.7.2 PHASEA0 ($\overline{\text{PHSA}}$)—Bit 9

- 0 = Peripheral output function of GPIOB[7] is defined to be PHASEA0
- 1 = Peripheral output function of GPI B[7] is defined to be the oscillator clock (MSTR_OSC, see **Figure 3-4**)

6.5.7.3 PHASEB0 ($\overline{\text{PHSB}}$)—Bit 8

- 0 = Peripheral output function of GPIOB[6] is defined to be PHASEB0
- 1 = Peripheral output function of GPIOB[6] is defined to be SYS_CLK2

10.2 DC Electrical Characteristics

Note: *The 56F8122 device is specified to meet Industrial requirements only; PWM, CAN and Quad Decoder are NOT available on the 56F8122 device.*

Table 10-5 DC Electrical Characteristics

At Recommended Operating Conditions; see Table 10-4

Characteristic	Symbol	Notes	Min	Typ	Max	Unit	Test Conditions
Output High Voltage	V_{OH}		2.4	—	—	V	$I_{OH} = I_{OHmax}$
Output Low Voltage	V_{OL}		—	—	0.4	V	$I_{OL} = I_{OLmax}$
Digital Input Current High pull-up enabled or disabled	I_{IH}	Pin Groups 1, 3, 4	—	0	+/- 2.5	µA	V_{IN} = 3.0V to 5.5V
Digital Input Current High with pull-down	I_{IH}	Pin Group 5	40	80	160	µA	V_{IN} = 3.0V to 5.5V
ADC Input Current High	I_{IHADC}	Pin Group 7	—	0	+/- 3.5	µA	$V_{IN} = V_{DDA}$
Digital Input Current Low pull-up enabled	I_{IL}	Pin Groups 1, 3, 4	-200	-100	-50	µA	V_{IN} = 0V
Digital Input Current Low pull-up disabled	I_{IL}	Pin Groups 1, 3, 4	—	0	+/- 2.5	µA	V_{IN} = 0V
Digital Input Current Low with pull-down	I_{IL}	Pin Group 5	—	0	+/- 2.5	µA	V_{IN} = 0V
ADC Input Current Low	I_{ILADC}	Pin Group 7	—	0	+/- 3.5	µA	V_{IN} = 0V
EXTAL Input Current Low clock input	I_{EXTAL}		—	0	+/- 2.5	µA	$V_{IN} = V_{DDA}$ or 0V
XTAL Input Current Low clock input	I_{XTAL}	CLKMODE = High	—	0	+/- 2.5	µA	$V_{IN} = V_{DDA}$ or 0V
		CLKMODE = Low	—	—	200	µA	$V_{IN} = V_{DDA}$ or 0V
Output Current High Impedance State	I_{OZ}	Pin Groups 1, 2, 3	—	0	+/- 2.5	µA	V_{OUT} = 3.0V to 5.5V or 0V
Schmitt Trigger Input Hysteresis	V_{HYS}	Pin Groups 1, 3, 4, 5	—	0.3	—	V	—
Input Capacitance (EXTAL/XTAL)	C_{INC}		—	4.5	—	pF	—
Output Capacitance (EXTAL/XTAL)	C_{OUTC}		—	5.5	—	pF	—
Input Capacitance	C_{IN}		—	6	—	pF	—
Output Capacitance	C_{OUT}		—	6	—	pF	—

See Pin Groups in Table 10-1

10.2.2 Temperature Sense

Note: *Temperature Sensor is NOT available in the 56F8122 device.*

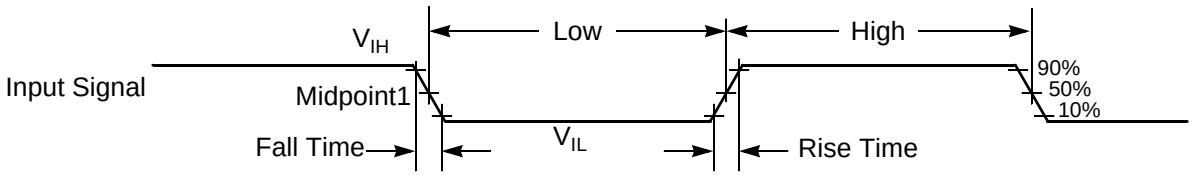
Table 10-11 Temperature Sense Parametrics

Characteristics	Symbol	Min	Typical	Max	Unit
Slope (Gain)[1]	m	—	7.762	—	mV/°C
Room Trim Temp. [1, 2]	T_{RT}	24	26	28	°C
Hot Trim Temp. (Industrial)[1,2]	T_{HT}	122	125	128	°C
Hot Trim Temp. (Automotive)[1,2]	T_{HT}	147	150	153	°C
Output Voltage @ V_{DDA_ADC} = 3.3V, T_J =0°C[1]	V_{TS0}	—	1.370	—	V
Supply Voltage	V_{DDA_ADC}	3.0	3.3	3.6	V
Supply Current - OFF	I_{DD-OFF}	—	—	10	µA
Supply Current - ON	I_{DD-ON}	—	—	250	µA
Accuracy[3,1] from -40°C to 150°C Using V_{TS} = mT + V_{TS0}	T_{ACC}	-6.7	0	6.7	°C
Resolution[4, 5,1]	R_{ES}	—	0.104	—	°C / bit

1. Includes the ADC conversion of the analog Temperature Sense voltage.
2. The ADC is not calibrated for the conversion of the Temperature Sensor trim value stored in the Flash Memory at FMOPT0 and FMOPT1.
3. See Application Note, AN1980, for methods to increase accuracy.
4. Assuming a 12-bit range from 0V to 3.3V.
5. Typical resolution calculated using equation, $R_{ES} = \frac{(V_{REFH} - V_{REFLO}) \times 1}{2^{12} \quad m}$

10.3 AC Electrical Characteristics

Tests are conducted using the input levels specified in **Table 10-5**. Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured between the 10% and 90% points, as shown in **Figure 10-1**.



Note: The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

Figure 10-1 Input Signal Measurement References

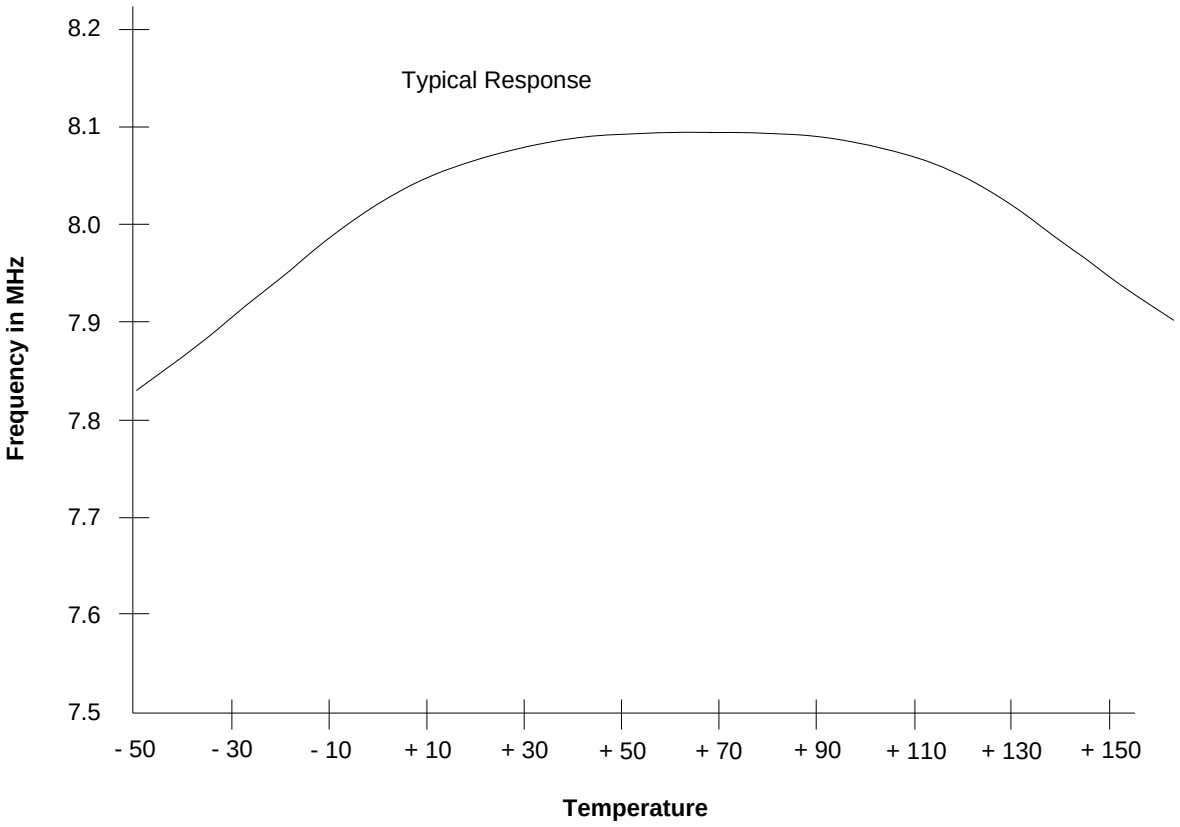


Figure 10-4 Frequency versus Temperature

10.8 Reset, Stop, Wait, Mode Select, and Interrupt Timing

Note: All address and data buses described here are internal.

Table 10-17 Reset, Stop, Wait, Mode Select, and Interrupt Timing[1,2]

Characteristic	Symbol	Typical Min	Typical Max	Unit	See Figure
Minimum $\overline{\text{RESET}}$ Assertion Duration	t_{RA}	16T	—	ns	10-5
Edge-sensitive Interrupt Request Width	t_{IRW}	1.5T	—	ns	10-6
$\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$ Assertion to General Purpose Output Valid, caused by first instruction execution in the interrupt service routine	t_{IG}	18T	—	ns	10-7
	$t_{IG - FAST}$	14T	—		
$\overline{\text{IRQA}}$ Width Assertion to Recover from Stop State[3]	t_{IW}	1.5T	—	ns	10-8

1. In the formulas, T = clock cycle. For an operating frequency of 60MHz, T = 16.67ns. At 8MHz (used during Reset and Stop modes), T = 125ns.
2. Parameters listed are guaranteed by design.
3. The interrupt instruction fetch is visible on the pins only in Mode 3.

10.13 Controller Area Network (CAN) Timing

Note: *CAN is NOT available in the 56F8122 device.*

Table 10-22 CAN Timing[1]

Characteristic	Symbol	Min	Max	Unit	See Figure
Baud Rate	BR_{CAN}	—	1	Mbps	—
Bus Wake-up detection	T_{WAKEUP}	T_{IPBUS}	—	µs	10-17

1. Parameters listed are guaranteed by design

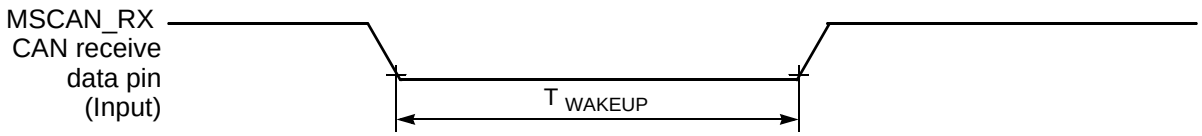


Figure 10-17 Bus Wakeup Detection

10.14 JTAG Timing

Table 10-23 JTAG Timing

Characteristic	Symbol	Min	Max	Unit	See Figure
TCK frequency of operation using EOnCE[1]	f_{OP}	DC	SYS_CLK/8	MHz	10-18
TCK frequency of operation not using EOnCE[1]	f_{OP}	DC	SYS_CLK/4	MHz	10-18
TCK clock pulse width	t_{PW}	50	—	ns	10-18
TMS, TDI data set-up time	t_{DS}	5	—	ns	10-19
TMS, TDI data hold time	t_{DH}	5	—	ns	10-19
TCK low to TDO data valid	t_{DV}	—	30	ns	10-19
TCK low to TDO tri-state	t_{TS}	—	30	ns	10-19

1. TCK frequency of operation must be less than 1/8 the processor rate.

Table 10-24 ADC Parameters (Continued)

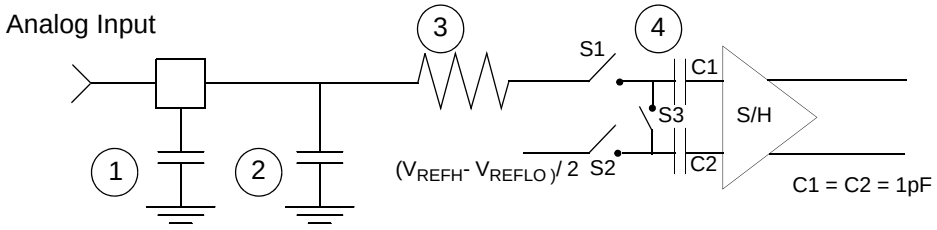
Characteristic	Symbol	Min	Typ	Max	Unit
ADC channel power-up time	t_{ADPU}	5	6	16	t_{AIC} cycles[3]
ADC reference circuit power-up time[4]	t_{VREF}	—	—	25	ms
Conversion time	t_{ADC}	—	6	—	t_{AIC} cycles[3]
Sample time	t_{ADS}	—	1	—	t_{AIC} cycles[3]
Input capacitance	C_{ADI}	—	5	—	pF
Input injection current[5], per pin	I_{ADI}	—	—	3	mA
Input injection current, total	I_{ADIT}	—	—	20	mA
V_{REFH} current	I_{VREFH}	—	1.2	3	mA
ADC A current	I_{ADCA}	—	25	—	mA
ADC B current	I_{ADCB}	—	25	—	mA
Quiescent current	I_{ADCQ}	—	0	10	μA
Uncalibrated Gain Error (ideal)	E_{GAIN}	—	+/- .004	+/- .01	—
Uncalibrated Offset Voltage	V_{OFFSET}	—	+/- 26	+/- 32	mV
Calibrated Absolute Error[6]	AE_{CAL}	—	See **Figure 10-20**	—	LSBs
Calibration Factor 1[7]	CF1	—	0.008597	—	—
Calibration Factor 2[7]	CF2	—	-2.8	—	—
Crosstalk between channels	—	—	-60	—	dB
Common Mode Voltage	V_{common}	—	$(V_{REFH} - V_{REFLO}) / 2$	—	V
Signal-to-noise ratio	SNR	—	64.6	—	db
Signal-to-noise plus distortion ratio	SINAD	—	59.1	—	db
Total Harmonic Distortion	THD	—	60.6	—	db
Spurious Free Dynamic Range	SFDR	—	61.1	—	db
Effective Number Of Bits[8]	ENOB	—	9.6	—	Bits

1. INL measured from $V_{in} = .1V_{REFH}$ to $V_{in} = .9V_{REFH}$
   10% to 90% Input Signal Range
2. LSB = Least Significant Bit
3. ADC clock cycles
4. Assumes each voltage reference pin is bypassed with 0.1μF ceramic capacitors to ground
5. The current that can be injected or sourced from an unselected ADC signal input without impacting the performance of the ADC. This allows the ADC to operate in noisy industrial environments where inductive flyback is possible.
6. Absolute error includes the effects of both gain error and offset error.
7. Please see the **56F8300 Peripheral User's Manual** for additional information on ADC calibration.
8. ENOB = (SINAD - 1.76)/6.02

10.16 Equivalent Circuit for ADC Inputs

Figure 10-21 illustrates the ADC input circuit during sample and hold. S1 and S2 are always open/closed at the same time that S3 is closed/open. When S1/S2 closed & S3 open, one input of the sample and hold circuit moves to (V_{REFH}-V_{REFLO})/2, while the other charges to the analog input voltage. When the switches are flipped, the charge on C1 and C2 are averaged via S3, with the result that a single-ended analog input is switched to a differential voltage centered about (V_{REFH}-V_{REFLO})/2. The switches switch on every cycle of the ADC clock (open one-half ADC clock, closed one-half ADC clock). Note that there are additional capacitances associated with the analog input pad, routing, etc., but these do not filter into the S/H output voltage, as S1 provides isolation during the charge-sharing phase.

One aspect of this circuit is that there is an on-going input current, which is a function of the analog input voltage, V_{REF} and the ADC clock frequency.



1. Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling; 1.8pf
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing; 2.04pf
3. Equivalent resistance for the ESD isolation resistor and the channel select mux; 500 ohms
4. Sampling capacitor at the sample and hold circuit. Capacitor C1 is normally disconnected from the input and is only connected to it at sampling time; 1pf

Figure 10-21 Equivalent Circuit for A/D Loading

10.17 Power Consumption

See **Section 10.1** for a list of IDD requirements for the device. This section provides additional detail which can be used to optimize power consumption for a given application.

Power consumption is given by the following equation:

Total power = A: internal [static component]
+B: internal [state-dependent component]
+C: internal [dynamic component]
+D: external [dynamic component]
+E: external [static]

A, the internal [static component], is comprised of the DC bias currents for the oscillator, leakage currents, PLL, and voltage references. These sources operate independently of processor state or operating frequency.

B, the internal [state-dependent component], reflects the supply current required by certain on-chip resources only when those resources are in use. These include RAM, Flash memory and the ADCs.

11.2 56F8122 Package and Pin-Out Information

This section contains package and pin-out information for the 56F8122. This device comes in a 48-pin Low-profile Quad Flat Pack (LQFP). **Figure 11-1** shows the package outline for the 48-pin LQFP, **Figure 12-1** shows the mechanical parameters for this package, and **Table 11-1** lists the pin-out for the 48-pin LQFP.

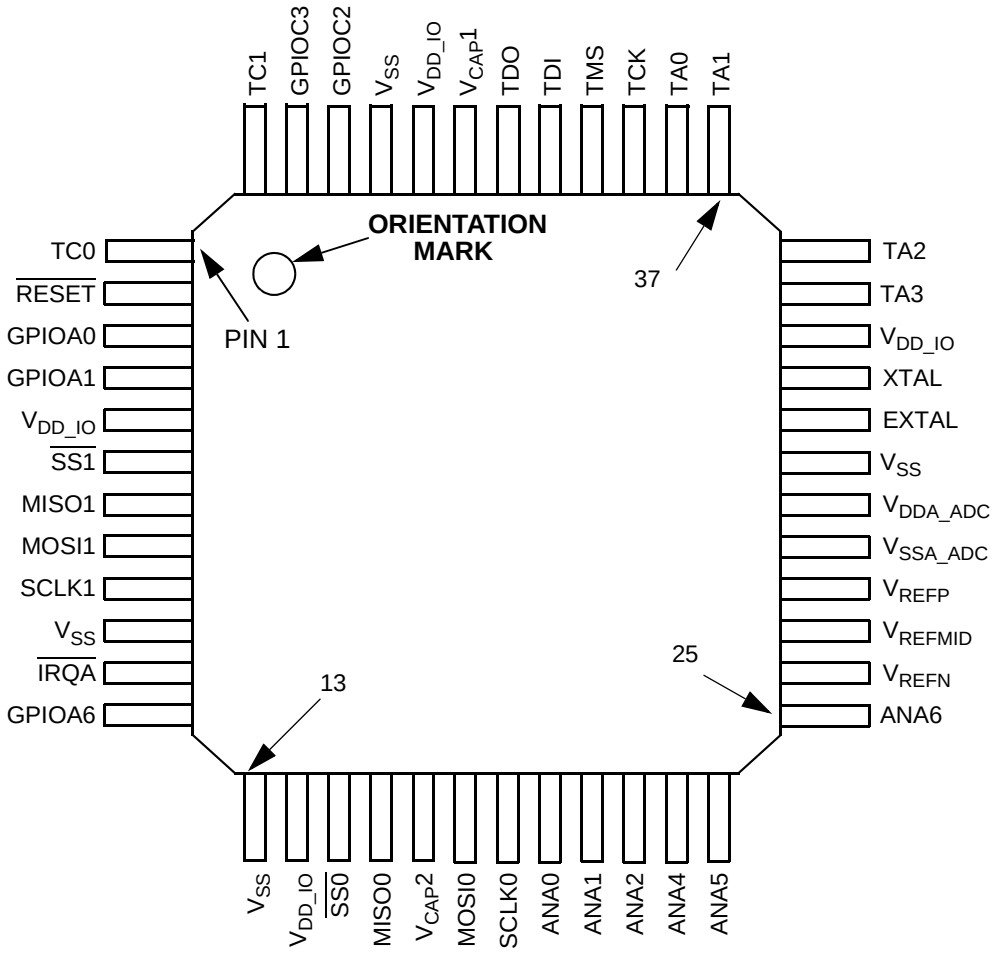
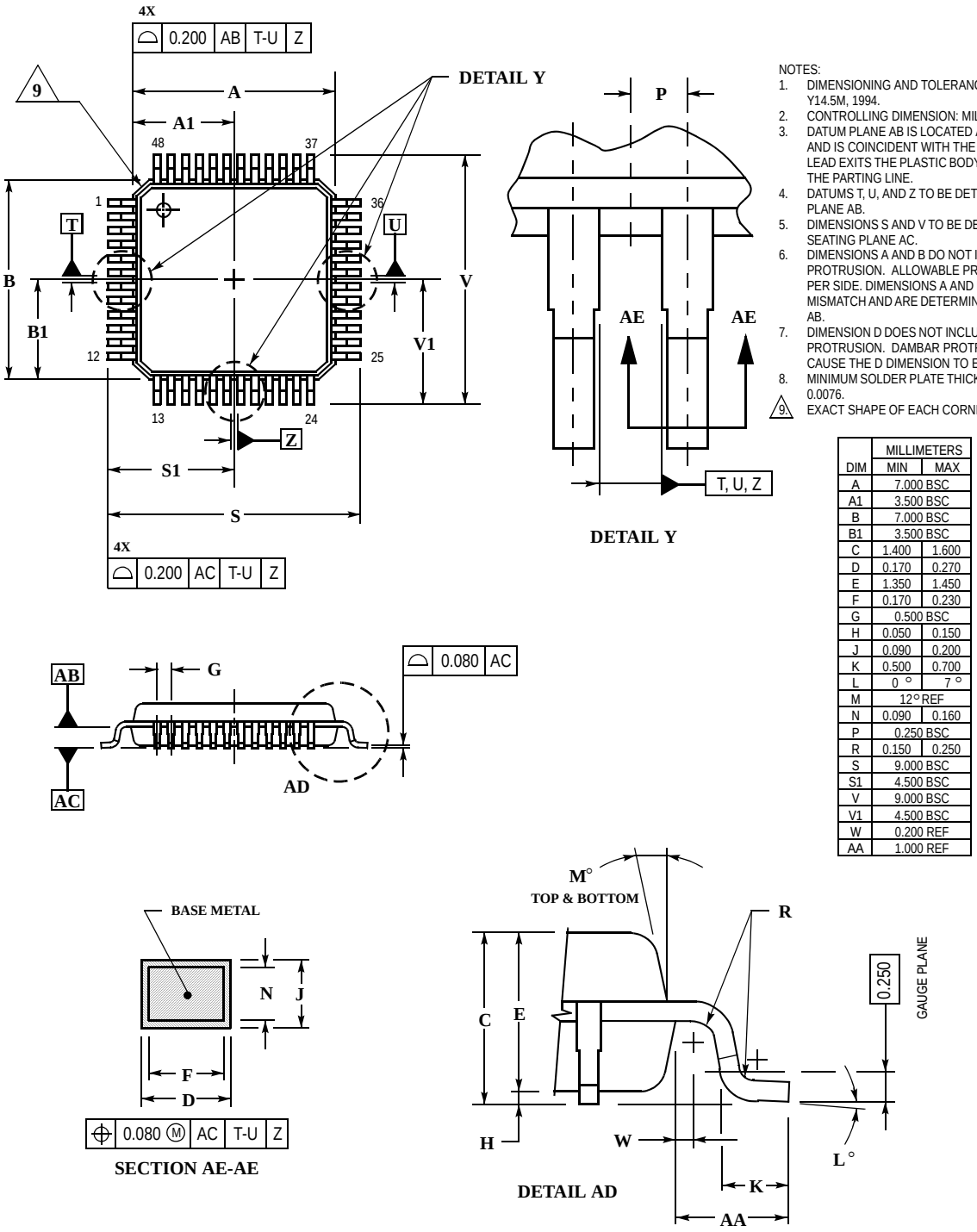


Figure 11-2 Top View, 56F8122 48-Pin LQFP Package



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS T, U, AND Z TO BE DETERMINED AT DATUM PLANE AB.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE AC.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350.
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

	MILLIMETERS	
DIM	MIN	MAX
A	7.000 BSC	
A1	3.500 BSC	
B	7.000 BSC	
B1	3.500 BSC	
C	1.400	1.600
D	0.170	0.270
E	1.350	1.450
F	0.170	0.230
G	0.500 BSC	
H	0.050	0.150
J	0.090	0.200
K	0.500	0.700
L	0 °	7 °
M	12° REF	
N	0.090	0.160
P	0.250 BSC	
R	0.150	0.250
S	9.000 BSC	
S1	4.500 BSC	
V	9.000 BSC	
V1	4.500 BSC	
W	0.200 REF	
AA	1.000 REF	

Figure 11-3 48-Pin LQFP Mechanical Information

Please see **www.freescale.com** for the most current case outline.