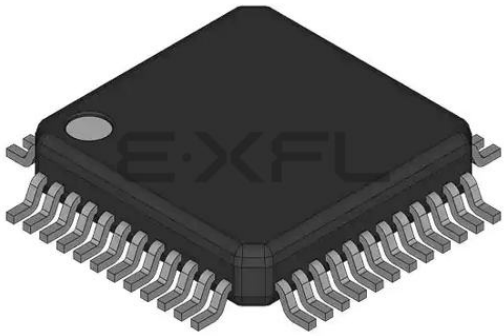

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	60MHz
Connectivity	CANbus, SCI, SPI
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	21
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 16
Voltage - Supply (Vcc/Vdd)	2.25V ~ 3.6V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc56f8322mfae

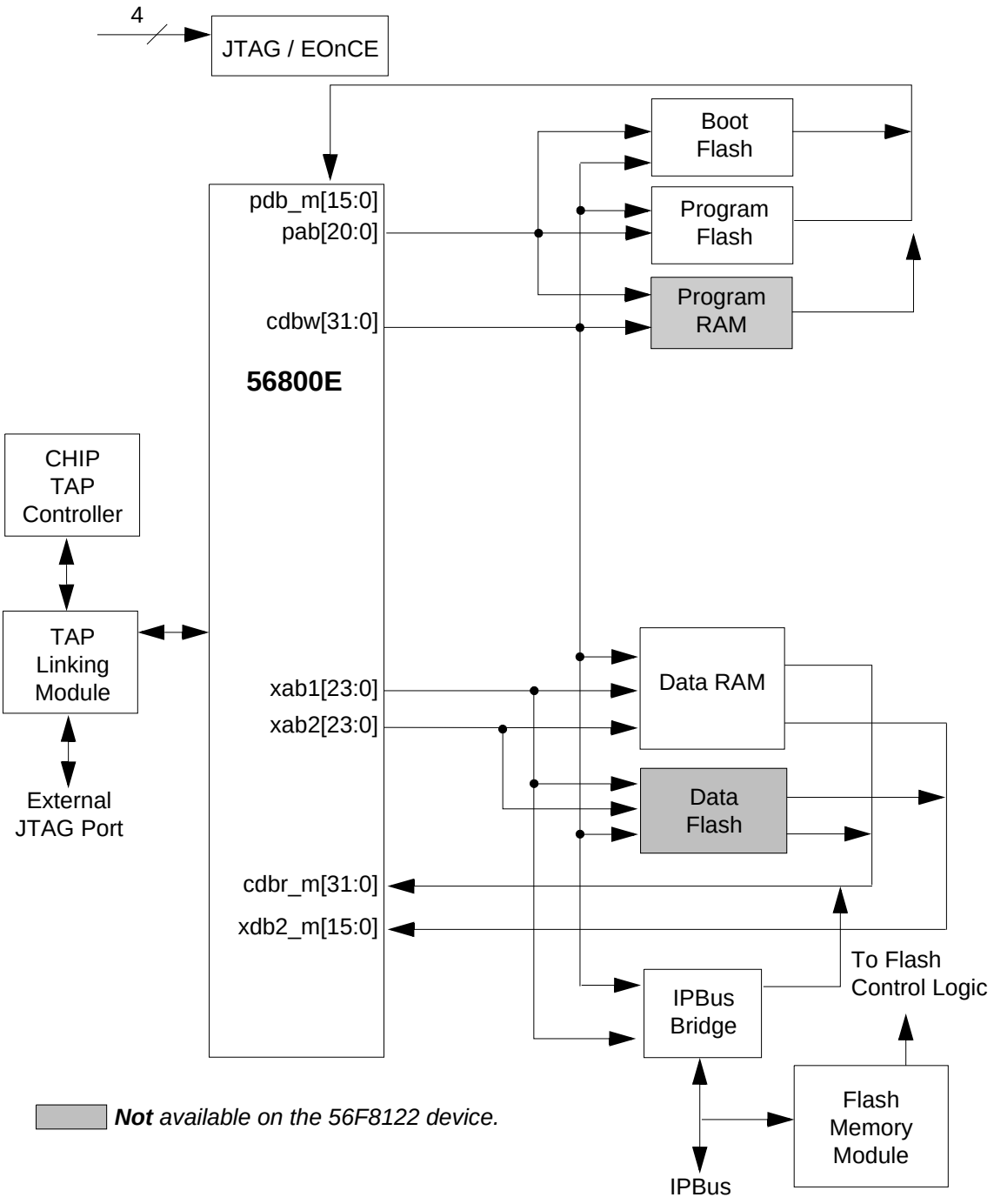

Figure 1-1 System Bus Interfaces

Note: Flash memories are encapsulated within the Flash Memory Module (FM). Flash control is accomplished by the I/O to the FM over the peripheral bus, while reads and writes are completed between the core and the Flash memories.

Note: The primary data RAM port is 32 bits wide. Other data ports are 16 bits.

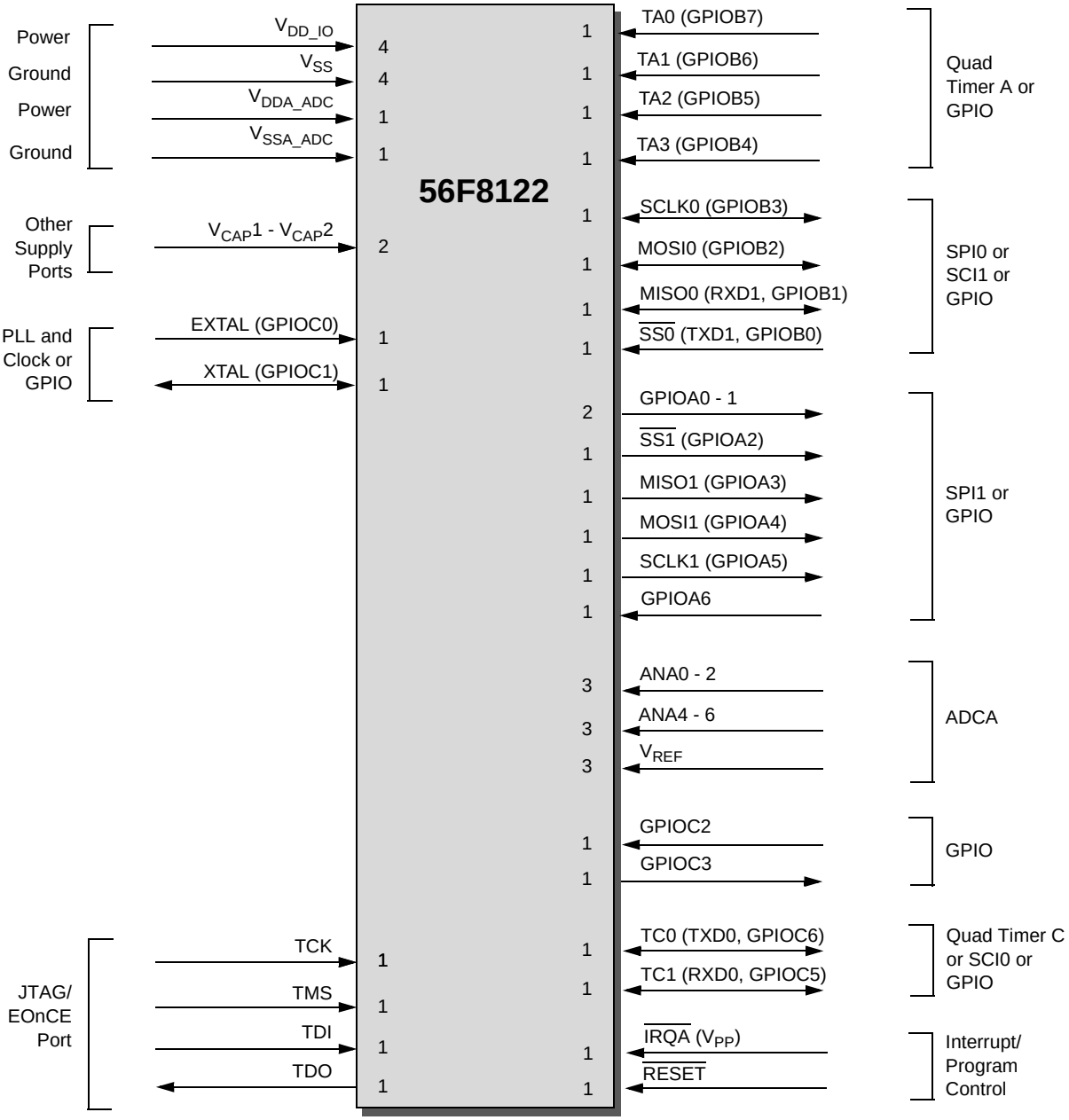

Figure 2-2 56F8122 Signals Identified by Functional Group (48-Pin LQFP)

2.2 Signal Pins

After reset, each pin is configured for its primary function (listed first). In the 56F8122, after reset, each pin must be configured for the desired function. The initialization software will configure each pin for the function listed first for each pin, as shown in **Table 2-2**. Any alternate functionality must be programmed.

Note: *Signals in italics are not available in the 56F8122 device.*

If the "State During Reset" lists more than one state for a pin, the first state is the actual reset state. Other states show the reset condition of the alternate function, which you get if the alternate pin function is selected without changing the configuration of the alternate peripheral. For example, the SCLK0/GPIOB3 pin shows that it is tri-stated during reset. If the GPIOB_PER is changed to select the GPIO function of the pin, it will become an input if no other registers are changed.

Table 2-2 Signal and Package Information for the 48-Pin LQFP

Signal Name	Pin No.	Type	State During Reset	Signal Description
V_{DD_IO}	5	Supply		**I/O Power** — This pin supplies 3.3V power to the chip I/O interface and also the Processor core throught the on-chip voltage regulator, if it is enabled.
V_{DD_IO}	14			
V_{DD_IO}	34			
V_{DD_IO}	44			
V_{DDA_ADC}	30	Supply		**ADC Power** — This pin supplies 3.3V power to the ADC modules. It must be connected to a clean analog power supply.
V_{SS}	10	Supply		**Ground** — These pins provide ground for chip logic and I/O drivers.
V_{SS}	13			
V_{SS}	31			
V_{SS}	45			
V_{SSA_ADC}	29	Supply		**ADC Analog Ground** — This pin supplies an analog ground to the ADC modules.
$V_{CAP}1$	43	Supply	Supply	V_{CAP}**1 - 2** — Connect each pin to a 2.2µF or greater bypass capacitor in order to bypass the core logic voltage regulator, required for proper chip operation.
$V_{CAP}2$	17			

Table 2-2 Signal and Package Information for the 48-Pin LQFP (Continued)

Signal Name	Pin No.	Type	State During Reset	Signal Description
PWMA4 **(MOSI1)** **(GPIOA4)**	8	Output Schmitt Input/ Output Schmitt Input/ Output	In reset, output is disabled, pull-up is enabled	**PWMA4** — This is one of six PWMA output pins. **SPI 1 Master Out/Slave In** — This serial data pin is an output from a master device and an input to a slave device. The master device places data on the MOSI line a half-cycle before the clock edge the slave device uses to latch the data. **Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin. In the 56F8322, the default state after reset is PWMA4. In the 56F8122, the default state is not one of the functions offered and must be reconfigured.
PWMA5 **(SCLK1)** **(GPIOA5)**	9	Output Schmitt Input/ Output Schmitt Input/ Output	In reset, output is disabled, pull-up is enabled	**PWMA5** — This is one of six PWMA output pins. **SPI 1 Serial Clock** — In the master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input. A Schmitt trigger input is used for noise immunity. **Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin. In the 56F8322, the default state after reset is PWMA5. In the 56F8122, the default state is not one of the functions offered and must be reconfigured.
FAULTA0 **(GPIOA6)**	12	Schmitt Input Schmitt Input/ Output	Input	**FAULTA0** — This fault input pin is used for disabling selected PWMA outputs in cases where fault conditions originate off-chip. **Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin. In the 56F8322, the default state after reset is FAULTA0. In the 56F8122, the default state is not one of the functions offered and must be reconfigured.
ANA0	20	Input	Analog Input	**ANA0 - 2** — Analog inputs to ADCA, Channel 0
ANA1	21			
ANA2	22			
ANA4	23	Input	Analog Input	**ANA4 - 6** — Analog inputs to ADCA, Channel 1
ANA5	24			
ANA6	25			

Table 4-13 Analog to Digital Converter Registers Address Map (Continued) (ADCA_BASE = $00 F200)

Register Acronym	Address Offset	Register Description
ADCA_HLMT 1	$1A	High Limit Register 1
ADCA_HLMT 2	$1B	High Limit Register 2
ADCA_HLMT 3	$1C	High Limit Register 3
ADCA_HLMT 4	$1D	High Limit Register 4
ADCA_HLMT 5	$1E	High Limit Register 5
ADCA_HLMT 6	$1F	High Limit Register 6
ADCA_HLMT 7	$20	High Limit Register 7
ADCA_OFS 0	$21	Offset Register 0
ADCA_OFS 1	$22	Offset Register 1
ADCA_OFS 2	$23	Offset Register 2
ADCA_OFS 3	$24	Offset Register 3
ADCA_OFS 4	$25	Offset Register 4
ADCA_OFS 5	$26	Offset Register 5
ADCA_OFS 6	$27	Offset Register 6
ADCA_OFS 7	$28	Offset Register 7
ADCA_POWER	$29	Power Control Register
ADCA_CAL	$2A	ADC Calibration Register

Table 4-14 Temperature Sensor Register Address Map (TSENSOR_BASE = $00 F270)

Temperature Sensor is NOT available in the 56F8122 device

Register Acronym	Address Offset	Register Description
TSENSOR_CNTL	$0	Control Register

Table 4-15 Serial Communication Interface 0 Registers Address Map (SCI0_BASE = $00 F280)

Register Acronym	Address Offset	Register Description
SCI0_SCIBR	$0	Baud Rate Register
SCI0_SCICR	$1	Control Register
		Reserved
SCI0_SCISR	$3	Status Register
SCI0_SCIDR	$4	Data Register

Table 4-27 FlexCAN Registers Address Map (Continued) (FC_BASE = $00 F800)

FlexCAN is NOT available in the 56F8122 device

Register Acronym	Address Offset	Register Description
FCMB3_CONTROL	$58	Message Buffer 3 Control / Status Register
FCMB3_ID_HIGH	$59	Message Buffer 3 ID High Register
FCMB3_ID_LOW	$5A	Message Buffer 3 ID Low Register
FCMB3_DATA	$5B	Message Buffer 3 Data Register
FCMB3_DATA	$5C	Message Buffer 3 Data Register
FCMB3_DATA	$5D	Message Buffer 3 Data Register
FCMB3_DATA	$5E	Message Buffer 3 Data Register
		Reserved
FCMB4_CONTROL	$60	Message Buffer 4 Control / Status Register
FCMB4_ID_HIGH	$61	Message Buffer 4 ID High Register
FCMB4_ID_LOW	$62	Message Buffer 4 ID Low Register
FCMB4_DATA	$63	Message Buffer 4 Data Register
FCMB4_DATA	$64	Message Buffer 4 Data Register
FCMB4_DATA	$65	Message Buffer 4 Data Register
FCMB4_DATA	$66	Message Buffer 4 Data Register
		Reserved
FCMB5_CONTROL	$68	Message Buffer 5 Control / Status Register
FCMB5_ID_HIGH	$69	Message Buffer 5 ID High Register
FCMB5_ID_LOW	$6A	Message Buffer 5 ID Low Register
FCMB5_DATA	$6B	Message Buffer 5 Data Register
FCMB5_DATA	$6C	Message Buffer 5 Data Register
FCMB5_DATA	$6D	Message Buffer 5 Data Register
FCMB5_DATA	$6E	Message Buffer 5 Data Register
		Reserved
FCMB6_CONTROL	$70	Message Buffer 6 Control / Status Register
FCMB6_ID_HIGH	$71	Message Buffer 6 ID High Register
FCMB6_ID_LOW	$72	Message Buffer 6 ID Low Register
FCMB6_DATA	$73	Message Buffer 6 Data Register
FCMB6_DATA	$74	Message Buffer 6 Data Register
FCMB6_DATA	$75	Message Buffer 6 Data Register
FCMB6_DATA	$76	Message Buffer 6 Data Register
		Reserved
FCMB7_CONTROL	$78	Message Buffer 7 Control / Status Register
FCMB7_ID_HIGH	$79	Message Buffer 7 ID High Register
FCMB7_ID_LOW	$7A	Message Buffer 7 ID Low Register
FCMB7_DATA	$7B	Message Buffer 7 Data Register

5.6.2.1 Reserved—Bits 15–6

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.2.2 EOnCE Receive Register Full Interrupt Priority Level (RX_REG IPL)—Bits 5–4

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.2.3 EOnCE Transmit Register Empty Interrupt Priority Level (TX_REG IPL)—Bits 3–2

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.2.4 EOnCE Trace Buffer Interrupt Priority Level (TRBUF IPL)—Bits 1–0

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.3 Interrupt Priority Register 2 (IPR2)

Base + $2	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	FMCBE IPL		FMCC IPL		FMERR IPL		LOCK IPL		LVI IPL		0	0	0	0	IRQA IPL	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-5 Interrupt Priority Register 2 (IPR2)

5.6.8.5 Timer C, Channel 1 Interrupt Priority Level (TMRC1 IPL)—Bits 1–0

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.9 Interrupt Priority Register 8 (IPR8)

Base + $8	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	SCI0_RCV IPL		SCI0_RERR IPL		0	0	SCI0_TIDL IPL		SCI0_XMIT IPL		TMRA3 IPL		TMRA2 IPL		TMRA1 IPL	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-11 Interrupt Priority Register 8 (IPR8)

5.6.9.1 SCI0 Receiver Full Interrupt Priority Level (SCI0_RCV IPL)—Bits 15–14

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.9.2 SCI0 Receiver Error Interrupt Priority Level (SCI0_RERR IPL)—Bits 13–12

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.9.3 Reserved—Bits 11–10

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.10.5 ADC A Zero Crossing or Limit Error Interrupt Priority Level (ADCA_ZC IPL)—Bits 7–6

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.10.6 Reserved—Bits 5–4

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.10.7 ADC A Conversion Complete Interrupt Priority Level (ADCA_CC IPL)—Bits 3–2

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.10.8 Reserved—Bits 1–0

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.11 Vector Base Address Register (VBA)

Base + $A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	VECTOR BASE ADDRESS												
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-13 Vector Base Address Register (VBA)

5.6.11.1 Reserved—Bits 15–13

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.11.2 Interrupt Vector Base Address (VECTOR BASE ADDRESS)—Bits 12–0

The contents of this register determine the location of the Vector Address Table. The value in this register is used as the upper 13 bits of the interrupt vector address. The lower eight bits of the ISR address are determined based upon the highest-priority interrupt; see **Section 5.3.1** for details.

6.5.1.2 OnCE Enable (ONCE EBL)—Bit 5

- 0 = OnCE clock to 56800E core enabled when core TAP is enabled
- 1 = OnCE clock to 56800E core is always enabled

6.5.1.3 Software Reset (SW RST)—Bit 4

Writing 1 to this field will cause the part to reset.

6.5.1.4 Stop Disable (STOP_DISABLE)—Bits 3–2

- 00 = Stop mode will be entered when the 56800E core executes a STOP instruction
- 01 = The 56800E STOP instruction will not cause entry into Stop mode; STOP_DISABLE can be reprogrammed in the future
- 10 = The 56800E STOP instruction will not cause entry into Stop mode; STOP_DISABLE can then only be changed by resetting the device
- 11 = Same operation as 10

6.5.1.5 Wait Disable (WAIT_DISABLE)—Bits 1–0

- 00 = Wait mode will be entered when the 56800E core executes a WAIT instruction
- 01 = The 56800E WAIT instruction will not cause entry into Wait mode; WAIT_DISABLE can be reprogrammed in the future
- 10 = The 56800E WAIT instruction will not cause entry into Wait mode; WAIT_DISABLE can then only be changed by resetting the device
- 11 = Same operation as 10

6.5.2 SIM Reset Status Register (SIM_RSTSTS)

Bits in this register are set upon any system reset and are initialized only by a Power-On Reset (POR). A reset (other than POR) will only set bits in the register; bits are not cleared. Only software should clear this register.

Base + $1	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	0	SWR	COPR	EXTR	POR	0	0
Write																
RESET	0	0	0	0	0	0	0	0	0	0					0	0

Figure 6-4 SIM Reset Status Register (SIM_RSTSTS)

6.5.2.1 Reserved—Bits 15–6

This bit field is reserved or not implemented. It is read as zero and cannot be modified by writing.

6.5.2.2 Software Reset (SWR)—Bit 5

When 1, this bit indicates that the previous reset occurred as a result of a software reset (write to SW RST bit in the SIM_CONTROL register). This bit will be cleared by any hardware reset or by software. Writing a 0 to this bit position will set the bit, while writing a 1 to the bit will clear it.

6.5.6.3 IRQ—Bit 10

This bit controls the pull-up resistors on the $\overline{\text{IRQA}}$ pin.

6.5.6.4 Reserved—Bits 9–4

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.6.5 JTAG—Bit 3

This bit controls the pull-up resistors on the $\overline{\text{TRST}}$ (This pin is always tied inactive on the 56F8322), TMS and TDI pins.

6.5.6.6 Reserved—Bits 2–0

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.7 CLKO Select Register (SIM_CLKOSR)

The CLKO select register can be used to multiplex out any one of the clocks generated inside the clock generation and SIM modules. The default value is SYS_CLK. All other clocks primarily muxed out are for test purposes only, and are subject to significant unspecified latencies at high frequencies.

The upper four bits of the GPIOB register can function as GPIO, Quad Decoder #0 signals, or as additional clock output signals. GPIO has priority and is enabled/disabled via the GPIOB_PER. If GPIOB[7:4] are programmed to operate as peripheral outputs, then the choice between Quad Decoder #0 and additional clock outputs is made here in the CLKOSR. The default state is for the peripheral function of GPIOB[7:4] to be programmed as Quad Decoder #0. This can be changed by altering $\overline{\text{PHASE0}}$ through $\overline{\text{INDEX}}$ as shown in **Figure 6-9**.

The CLKOUT pin is not bonded out in this device. Instead, it is offered only as a pad for die-level testing.

Base + $A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	$\overline{\text{PHSA}}$	$\overline{\text{PHSB}}$	$\overline{\text{INDEX}}$	$\overline{\text{HOME}}$	CLK DIS	CLKOSEL				
Write																
RESET	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Figure 6-9 CLKO Select Register (SIM_CLKOSR)

6.5.7.1 Reserved—Bits 15–10

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.7.2 PHASEA0 ($\overline{\text{PHSA}}$)—Bit 9

- 0 = Peripheral output function of GPIOB[7] is defined to be PHASEA0
- 1 = Peripheral output function of GPI B[7] is defined to be the oscillator clock (MSTR_OSC, see **Figure 3-4**)

6.5.7.3 PHASEB0 ($\overline{\text{PHSB}}$)—Bit 8

- 0 = Peripheral output function of GPIOB[6] is defined to be PHASEB0
- 1 = Peripheral output function of GPIOB[6] is defined to be SYS_CLK2

As shown in **Figure 6-10**, the GPIO has the final control over which pin controls the I/O. SIM_GPS simply decides which peripheral will be routed to the I/O.

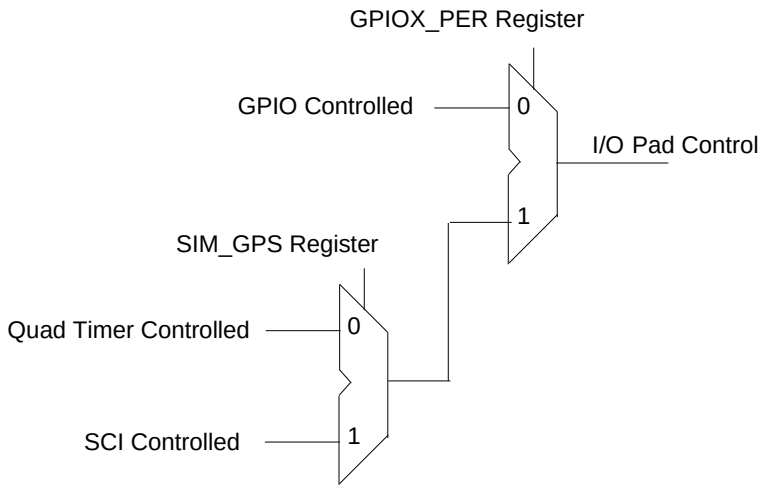

Figure 6-10 Overall Control of Pads Using SIM_GPS Control

Base + $B	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	C6	C5	B1	B0	A5	A4	A3	A2
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-11 GPIO Peripheral Select Register (SIM_GPS)

6.5.8.1 Reserved—Bits 15–8

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.8.2 GPIO C6 (C6)—Bit 7

This bit selects the alternate function for GPIOC6.

- 0 = TC0 (default)
- 1 = TXD0

6.5.8.3 GPIOC5 (C5)—Bit 6

This bit selects the alternate function for GPIOC5.

- 0 = TC1 (default)
- 1 = RXD0

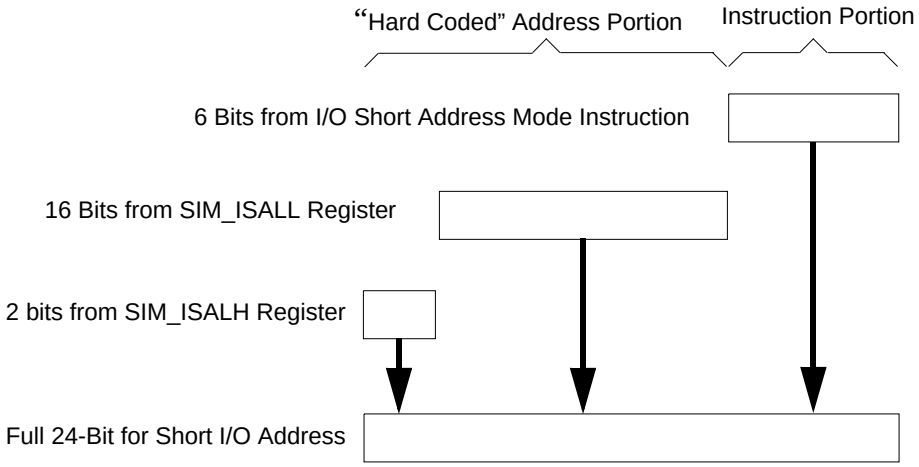

Figure 6-13 I/O Short Address Determination

With this register set, an interrupt driver can set the SIM_ISALL register pair to point to its peripheral registers and then use the I/O Short addressing mode to reference them. The ISR should restore this register to its previous contents prior to returning from interrupt.

Note: The default value of this register set points to the EOnCE registers.

Note: The pipeline delay between setting this register set and using short I/O addressing with the new value is five cycles.

Base + $D	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	1	1	1	1	1	1	1	1	1	1	1	1	1	1	ISAL[23:22]	
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 6-14 I/O Short Address Location High Register (SIM_ISALH)

6.5.10.1 Input/Output Short Address Low (ISAL[23:22])—Bit 1–0

This field represents the upper two address bits of the “hard coded” I/O short address.

Base + $E	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	ISAL[21:6]															
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 6-15 I/O Short Address Location Low Register (SIM_ISALL)

6.8 Stop and Wait Mode Disable Function

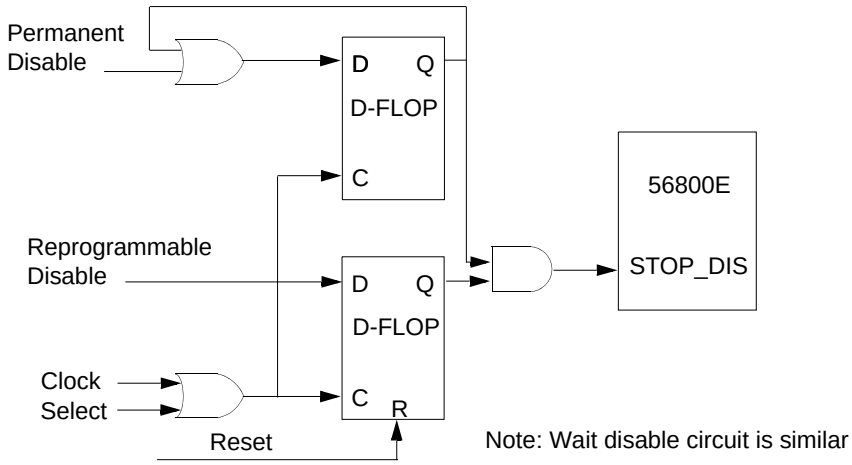

Figure 6-16 Internal Stop Disable Circuit

The 56800E core contains both STOP and WAIT instructions. Both put the CPU to sleep. For lowest power consumption in Stop mode, the PLL can be shut down. This must be done explicitly before entering Stop mode, since there is no automatic mechanism for this. When the PLL is shut down, the 56800E system clock must be set equal to the prescaler output.

Some applications require the 56800E STOP and WAIT instructions be disabled. To disable those instructions, write to the SIM control register (SIM_CONTROL) described in **Section 6.5.1** . This procedure can be on either a permanent or temporary basis. Permanently assigned applications last only until their next reset.

6.9 Resets

The SIM supports four sources of reset. The two asynchronous sources are the external $\overline{\text{RESET}}$ pin and the Power-On Reset (POR). The two synchronous sources are the software reset, which is generated within the SIM itself, by writing to the SIM_CONTROL register, and the COP reset.

Reset begins with the assertion of any of the reset sources. Release of reset to various blocks is sequenced to permit proper operation of the device. A POR reset is declared when reset is removed and any of the three voltage detectors (1.8V POR, 2.2V core voltage, or 2.7V I/O voltage) indicate a low supply voltage condition. POR will continue to be asserted until all voltage detectors indicate a stable supply is available (note that as power is removed POR is not declared until the 1.8V core voltage threshold is reached.) A POR reset is then extended for 64 clock cycles to permit stabilization of the clock source, followed by a 32 clock window in which SIM clocking is initiated. It is then followed by a 32 clock window in which peripherals are released to implement Flash security, and, finally, followed by a 32 clock window in which the core is initialized. After completion of the described reset sequence, application code will begin execution.

Resets may be asserted asynchronously, but are always released internally on a rising edge of the system clock.

Part 8 General Purpose Input/Output (GPIO)

8.1 Introduction

This section is intended to supplement the GPIO information found in the **56F8300 Peripheral User Manual** and contains only chip-specific information. This information supercedes the generic information in the **56F8300 Peripheral User Manual**.

8.2 Configuration

There are three GPIO ports defined on the 56F8322/56F8122. The width of each port and the associated peripheral function is shown in **Table 8-1** and **Table 8-2**. The specific mapping of GPIO port pins is shown in **Table 8-3**.

Table 8-1 56F8322 GPIO Ports Configuration

GPIO Port	Port Width	Available Pins in 56F8322	Peripheral Function	Reset Function
A	12	7	PWM, SPI 1	PWM
B	8	8	SPI 0, DEC 0, TMRA, SCI 1	SPI 0, DEC 0
C	7	6	XTAL, EXTAL, CAN, TMRC, SCI 0	XTAL, EXTAL, CAN, TMRC

Table 8-2 56F8122 GPIO Ports Configuration

GPIO Port	Port Width	Available Pins in 56F8122	Peripheral Function	Reset Function
A	12	7	SPI 1	Must be reconfigured
B	8	8	SPI 0, SCI1, TMRA	SPI 0, other pins must be reconfigured
C	7	6	XTAL, EXTAL, TMRC, SCI 0	XTAL, EXTAL, TMRC; other pins must be reconfigured

Table 10-2 56F8322/56F8122 ElectroStatic Discharge (ESD) Protection

Characteristic	Min	Typ	Max	Unit
ESD for Human Body Model (HBM)	2000	—	—	V
ESD for Machine Model (MM)	200	—	—	V
ESD for Charge Device Model (CDM)	500	—	—	V

Table 10-3 Thermal Characteristics[6]

Characteristic	Comments	Symbol	Value	Unit	Notes
			48-pin LQFP		
Junction to ambient Natural Convection		$R_{\theta JA}$	41	°C/W	2
Junction to ambient (@1m/sec)		$R_{\theta JMA}$	34	°C/W	2
Junction to ambient Natural Convection	Four layer board (2s2p)	$R_{\theta JMA}$ (2s2p)	34	°C/W	1,2
Junction to ambient (@1m/sec)	Four layer board (2s2p)	$R_{\theta JMA}$	29	°C/W	1,2
Junction to case		$R_{\theta JC}$	8	°C/W	3
Junction to center of case		Ψ_{JT}	2	°C/W	4, 5
I/O pin power dissipation		$P_{I/O}$	User-determined	W	
Power dissipation		P_D	$P_D = (I_{DD} \times V_{DD} + P_{I/O})$	W	
Maximum allowed P_D		P_{DMAX}	$(TJ - TA) / R\theta JA$[7]	W	

1. Theta-JA determined on 2s2p test boards is frequently lower than would be observed in an application. Determined on 2s2p thermal test board.
2. Junction to ambient thermal resistance, Theta-JA (R_{qJA}), was simulated to be equivalent to the JEDEC specification JESD51-2 in a horizontal configuration in natural convection. Theta-JA was also simulated on a thermal test board with two internal planes (2s2p, where “s” is the number of signal layers and “p” is the number of planes) per JESD51-6 and JESD51-7. The correct name for Theta-JA for forced convection or with the non-single layer boards is Theta-JMA.
3. Junction to case thermal resistance, Theta-JC (R_{qJC}), was simulated to be equivalent to the measured values using the cold plate technique with the cold plate temperature used as the "case" temperature. The basic cold plate measurement technique is described by MIL-STD 883D, Method 1012.1. This is the correct thermal metric to use to calculate thermal performance when the package is being used with a heat sink.
4. Thermal Characterization Parameter, Psi-JT (Y_{JT}), is the "resistance" from junction to reference point thermocouple on top center of case as defined in JESD51-2. Y_{JT} is a useful value to use to estimate junction temperature in steady-state customer environments.
5. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
6. See **Section 12.1** for more details on thermal design considerations.
7. TJ = Junction temperature
   TA = Ambient temperature

Note: *The 56F8122 device is guaranteed to 40MHz and specified to meet Industrial requirements only; PWM, CAN and Quad Decoder are NOT available on the 56F8122 device.*

Table 10-4 Recommended Operating Conditions

(V_{REFLO} = 0V, V_{SS} = V_{SSA_ADC} = 0V, V_{DDA} = V_{DDA_ADC} = $V_{DDA\_OSC\_PLL}$)

Characteristic	Symbol	Notes	Min	Typ	Max	Unit
Supply voltage	V_{DD_IO}		3	3.3	3.6	V
ADC Supply Voltage	V_{DDA_ADC}, V_{REFH}	V_{REFH} must be less than or equal to V_{DDA_ADC}	3	3.3	3.6	V
Oscillator / PLL Supply Voltage	$V_{DDA\_OSC\_PLL}$		3	3.3	3.6	V
Internal Logic Core Supply Voltage	V_{DD_CORE}	OCR_DIS is High	2.25	2.5	2.75	V
Device Clock Frequency	FSYSCLK		0	—	60/40	MHz
Input High Voltage (digital)	V_{IN}	Pin Groups 1, 3 ,4, 5	2	—	5.5	V
Input High Voltage (XTAL/EXTAL, XTAL is not driven by an external clock)	V_{IHC}	Pin Group 6	V_{DDA}-0.8	—	V_{DDA}+0.3	V
Input high voltage (XTAL/EXTAL, XTAL is driven by an external clock)	V_{IHC}	Pin Group 6	2	—	V_{DDA}+0.3	V
Input Low Voltage	V_{IL}	Pin Groups 1, 3, 4, 5, 6	-0.3	—	0.8	V
Output High Source Current V_{OH} = 2.4V (V_{OH} min.)	I_{OH}	Pin Groups 1, 2	—	—	-4	mA
		Pin Group 3	—	—	-12	
Output Low Sink Current V_{OL} = 0.4V (V_{OL} max)	I_{OL}	Pin Groups 1, 2	—	—	4	mA
		Pin Group 3	—	—	12	
Ambient Operating Temperature (Automotive)	T_A		-40	—	125	°C
Ambient Operating Temperature (Industrial)	T_A		-40	—	105	°C
Flash Endurance (Automotive) (Program Erase Cycles)	N_F	T_A = -40°C to 125°C	10,000	—	—	Cycles
Flash Endurance (Industrial) (Program Erase Cycles)	N_F	T_A = -40°C to 105°C	10,000	—	—	Cycles
Flash Data Retention	T_R	T_J <= 85°C avg	15	—	—	Years

Note: Total chip source or sink current cannot exceed 150mA.

Note: *Pins in italics are NOT available in the 56F8122 device.*

See Pin Groups in **Table 10-1**

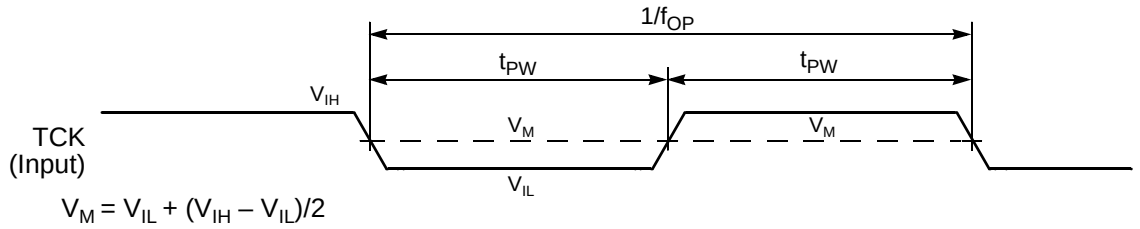

Figure 10-18 Test Clock Input Timing Diagram

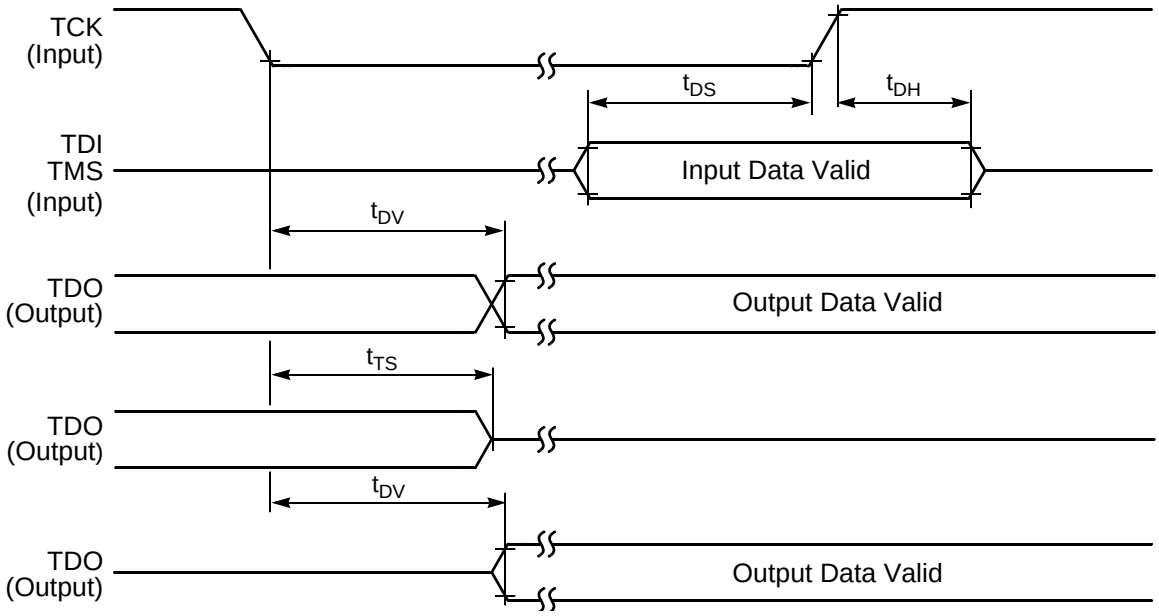

Figure 10-19 Test Access Port Timing Diagram

10.15 Analog-to-Digital Converter (ADC) Parameters

Table 10-24 ADC Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
Input voltages	V_{ADIN}	V_{REFL}	—	V_{REFH}	V
Resolution	R_{ES}	12	—	12	Bits
Integral Non-Linearity[1]	INL	—	+/- 2.4	+/- 3.2	LSB[2]
Differential Non-Linearity	DNL	—	+/- 0.7	< +1	LSB[2]
Monotonicity	GUARANTEED				
ADC internal clock	f_{ADIC}	0.5	—	5	MHz
Conversion range	R_{AD}	V_{REFL}	—	V_{REFH}	V

Table 11-1 56F8322 48-Pin LQFP Package Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	TC0	13	V_{SS}	25	ANA6	37	PHASEB
2	$\overline{\text{RESET}}$	14	V_{DD_IO}	26	V_{REFN}	38	PHASEA
3	PWMA0	15	$\overline{\text{SS0}}$	27	V_{REFMID}	39	TCK
4	PWMA1	16	MISO0	28	V_{REFP}	40	TMS
5	V_{DD_IO}	17	$V_{CAP}2$	29	V_{SSA_ADC}	41	TDI
6	PWMA2	18	MOSI0	30	V_{DDA_ADC}	42	TDO
7	PWMA3	19	SCLK0	31	V_{SS}	43	$V_{CAP}1$
8	PWMA4	20	ANA0	32	EXTAL	44	V_{DD_IO}
9	PWMA5	21	ANA1	33	XTAL	45	V_{SS}
10	V_{SS}	22	ANA2	34	V_{DD_IO}	46	CAN_RX
11	$\overline{\text{IRQA}}$	23	ANA4	35	HOME0	47	CAN_TX
12	FAULTA0	24	ANA5	36	INDEX0	48	TC1

11.2 56F8122 Package and Pin-Out Information

This section contains package and pin-out information for the 56F8122. This device comes in a 48-pin Low-profile Quad Flat Pack (LQFP). **Figure 11-1** shows the package outline for the 48-pin LQFP, **Figure 12-1** shows the mechanical parameters for this package, and **Table 11-1** lists the pin-out for the 48-pin LQFP.

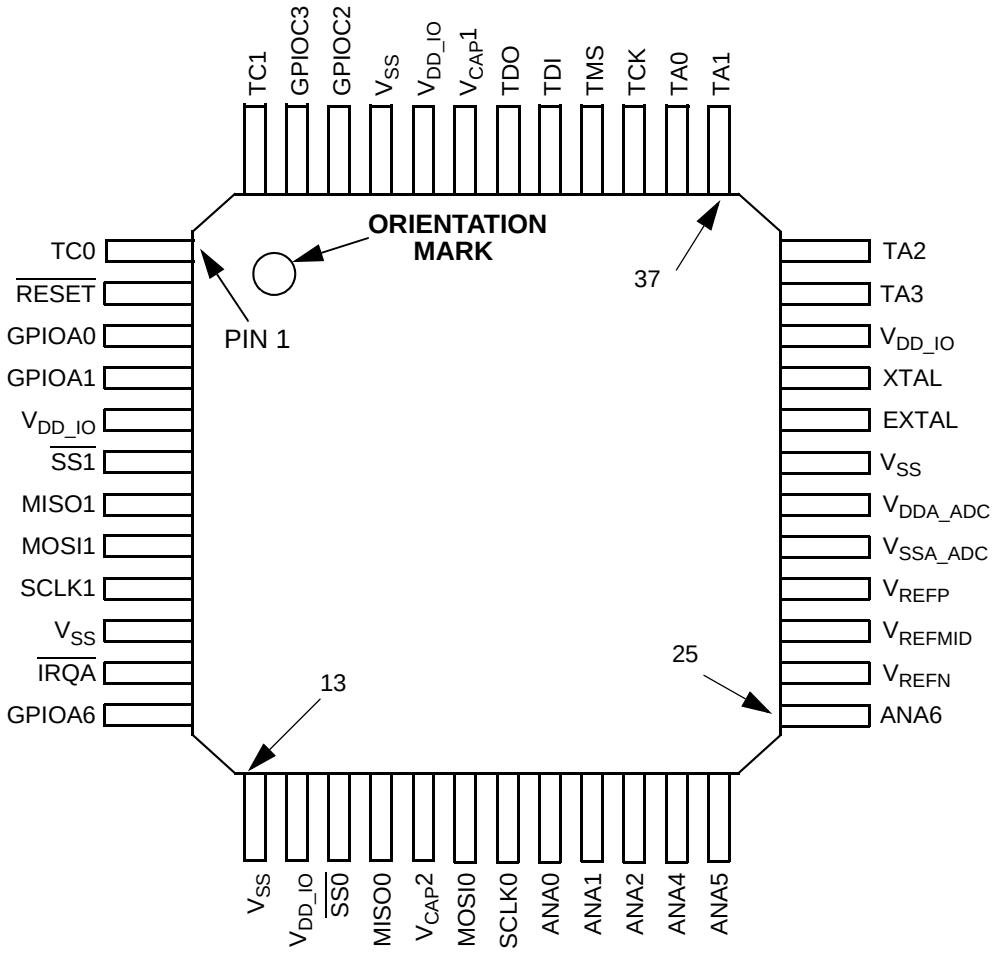

Figure 11-2 Top View, 56F8122 48-Pin LQFP Package