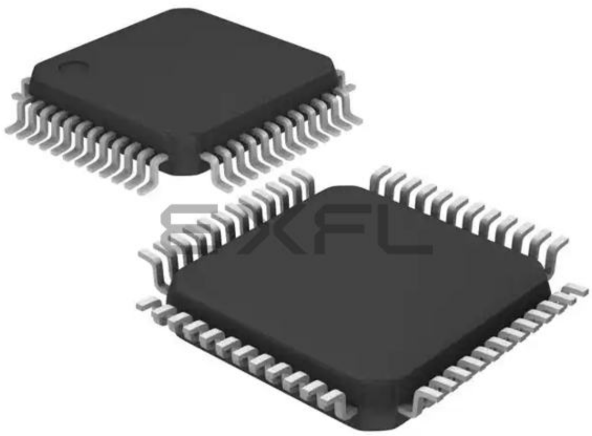

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	56800E
Core Size	16-Bit
Speed	60MHz
Connectivity	CANbus, SCI, SPI
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	21
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 16
Voltage - Supply (Vcc/Vdd)	2.25V ~ 3.6V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8322vfaer2

Part 1 Overview

1.1 56F8322/56F8122 Features

1.1.1 Core

- Efficient 16-bit 56800E family controller engine with dual Harvard architecture
- Up to 60 Million Instructions Per Second (MIPS) at 60MHz core frequency
- Single-cycle 16 × 16-bit parallel Multiplier-Accumulator (MAC)
- Four 36-bit accumulators, including extension bits
- Arithmetic and logic multi-bit shifter
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Three internal address buses
- Four internal data buses
- Instruction set supports both DSP and controller functions
- Controller-style addressing modes and instructions for compact code
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/EOnCE debug programming interface

1.1.2 Differences Between Devices

Table 1-1 outlines the key differences between the 56F8322 and 56F8122 devices.

Table 1-1 Device Differences

Feature	56F8322	56F8122
Guaranteed Speed	60MHz/60 MIPS	40MHz/40 MIPS
Program RAM	4KB	Not Available
Data Flash	8KB	Not Available
PWM	1 x 6	Not Available
CAN	1	Not Available
Quadrature Decoder	1 x 4	Not Available
Temperature Sensor	1	Not Available
Dedicated GPIO	—	5

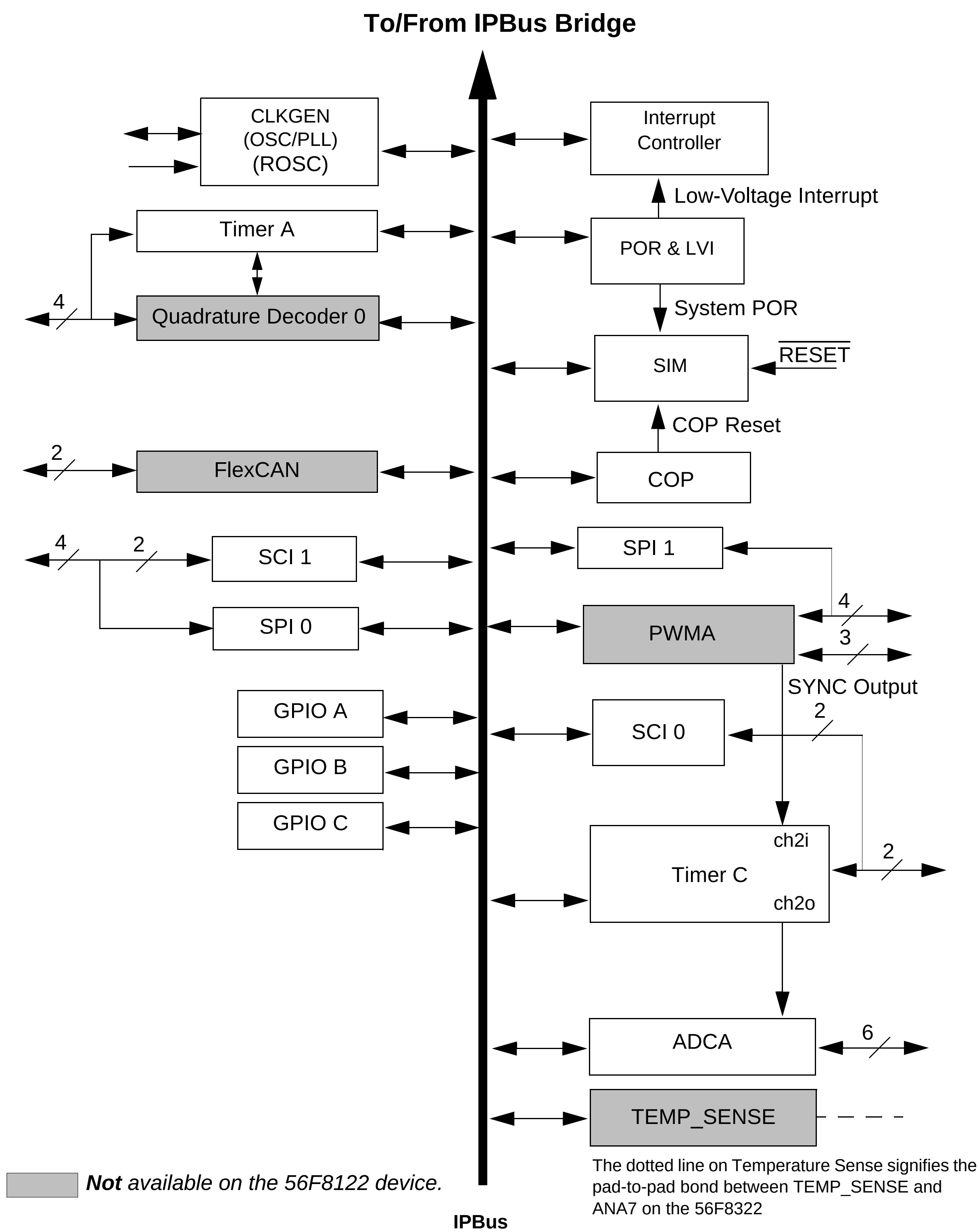

Figure 1-2 Peripheral Subsystem

Table 1-2 Bus Signal Names

Name	Function
Program Memory Interface	
pdb_m[15:0]	Program data bus for instruction word fetches or read operations.
cdbw[15:0]	Primary core data bus used for program memory writes. (Only these 16 bits of the cdbw[31:0] bus are used for writes to program memory.)
pab[20:0]	Program memory address bus. Data is returned on pdb_m bus.
Primary Data Memory Interface Bus	
cdbr_m[31:0]	Primary core data bus for memory reads. Addressed via xab1 bus.
cdbw[31:0]	Primary core data bus for memory writes. Addressed via xab1 bus.
xab1[23:0]	Primary data address bus. Capable of addressing bytes[1], words, and long data types. Data is written on cdbw and returned on cdbr_m. Also used to access memory-mapped I/O.
Secondary Data Memory Interface	
xdb2_m[15:0]	Secondary data bus used for secondary data address bus xab2 in the dual memory reads.
xab2[23:0]	Secondary data address bus used for the second of two simultaneous accesses. Capable of addressing only words. Data is returned on xdb2_m.
Peripheral Interface Bus	
IPBus [15:0]	Peripheral bus accesses all on-chip peripherals registers. This bus operates at the same clock rate as the Primary Data Memory and therefore generates no delays when accessing the processor. Write data is obtained from cdbw. Read data is provided to cdbr_m.

1. Byte accesses can only occur in the bottom half of the memory address space. The MSB of the address will be forced to 0.

2.2 Signal Pins

After reset, each pin is configured for its primary function (listed first). In the 56F8122, after reset, each pin must be configured for the desired function. The initialization software will configure each pin for the function listed first for each pin, as shown in **Table 2-2**. Any alternate functionality must be programmed.

Note: *Signals in italics are not available in the 56F8122 device.*

If the “State During Reset” lists more than one state for a pin, the first state is the actual reset state. Other states show the reset condition of the alternate function, which you get if the alternate pin function is selected without changing the configuration of the alternate peripheral. For example, the SCLK0/GPIOB3 pin shows that it is tri-stated during reset. If the GPIOB_PER is changed to select the GPIO function of the pin, it will become an input if no other registers are changed.

Table 2-2 Signal and Package Information for the 48-Pin LQFP

Signal Name	Pin No.	Type	State During Reset	Signal Description
V_{DD_IO}	5	Supply		**I/O Power** — This pin supplies 3.3V power to the chip I/O interface and also the Processor core throught the on-chip voltage regulator, if it is enabled.
V_{DD_IO}	14			
V_{DD_IO}	34			
V_{DD_IO}	44			
V_{DDA_ADC}	30	Supply		**ADC Power** — This pin supplies 3.3V power to the ADC modules. It must be connected to a clean analog power supply.
V_{SS}	10	Supply		**Ground** — These pins provide ground for chip logic and I/O drivers.
V_{SS}	13			
V_{SS}	31			
V_{SS}	45			
V_{SSA_ADC}	29	Supply		**ADC Analog Ground** — This pin supplies an analog ground to the ADC modules.
$V_{CAP}1$	43	Supply	Supply	**$V_{CAP}1$ - 2** — Connect each pin to a 2.2μF or greater bypass capacitor in order to bypass the core logic voltage regulator, required for proper chip operation.
$V_{CAP}2$	17			

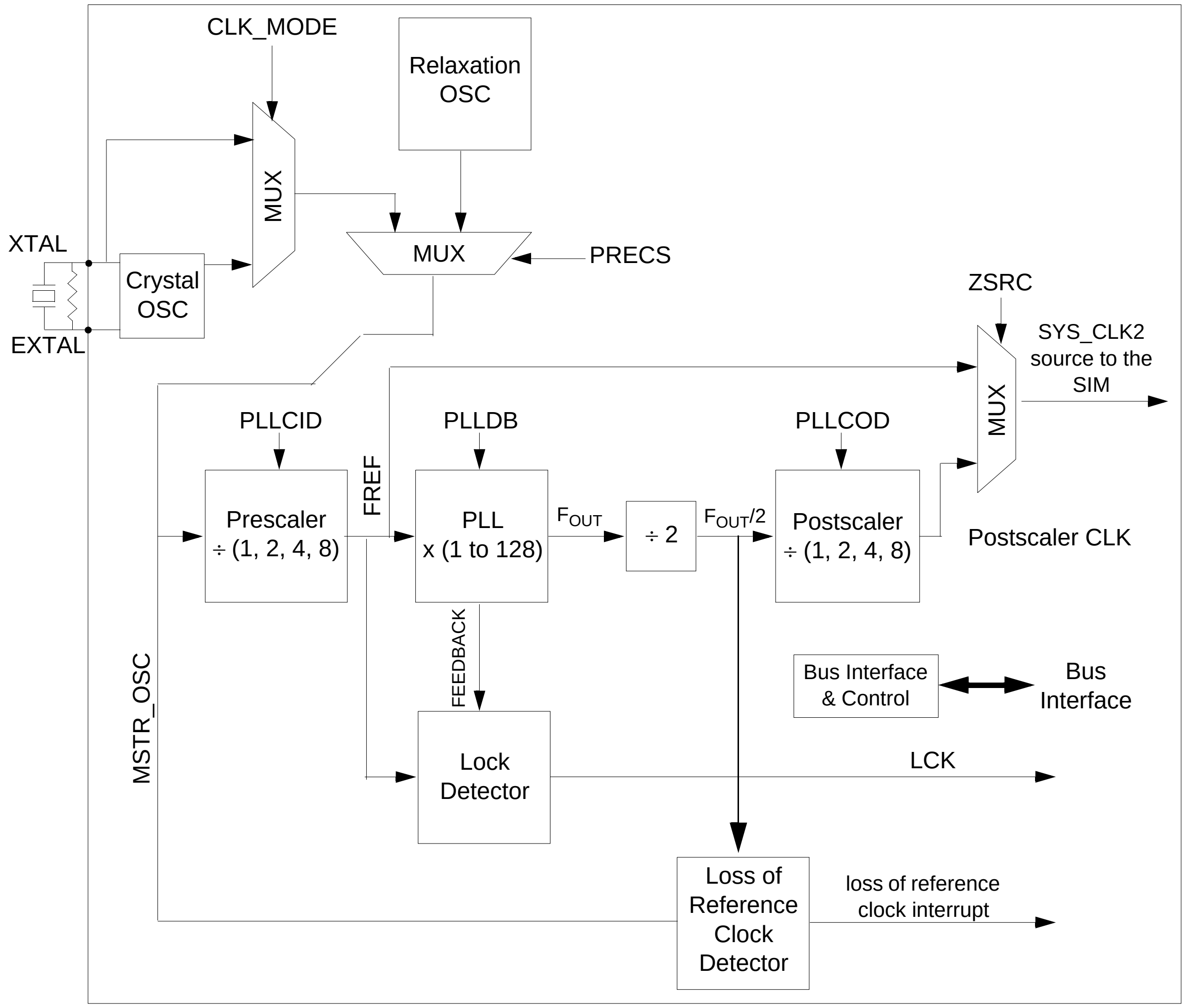

Figure 3-4 Internal Clock Operation

3.5 Registers

When referring to the register definitions for the OCCS in the **56F8300 Peripheral User Manual**, use the register definitions **with** the internal Relaxation Oscillator, since the 56F8322 and 56F8122 contain this oscillator.

4.6 EOnCE Memory Map

Table 4-6 EOnCE Memory Map

Address	Register Acronym	Register Name
		Reserved
X:$FF FF8A	OESCR	External Signal Control Register
		Reserved
X:$FF FF8E	OBCNTR	Breakpoint Unit [0] Counter
		Reserved
X:$FF FF90	OBMSK (32 bits)	Breakpoint 1 Unit [0] Mask Register
X:$FF FF91	—	Breakpoint 1 Unit [0] Mask Register
X:$FF FF92	OBAR2 (32 bits)	Breakpoint 2 Unit [0] Address Register
X:$FF FF93	—	Breakpoint 2 Unit [0] Address Register
X:$FF FF94	OBAR1 (24 bits)	Breakpoint 1 Unit [0] Address Register
X:$FF FF95	—	Breakpoint 1 Unit [0] Address Register
X:$FF FF96	OBCR (24 bits)	Breakpoint Unit [0] Control Register
X:$FF FF97	—	Breakpoint Unit [0] Control Register
X:$FF FF98	OTB (21-24 bits/stage)	Trace Buffer Register Stages
X:$FF FF99	—	Trace Buffer Register Stages
X:$FF FF9A	OTBPR (8 bits)	Trace Buffer Pointer Register
X:$FF FF9B	OTBCR	Trace Buffer Control Register
X:$FF FF9C	OBASE (8 bits)	Peripheral Base Address Register
X:$FF FF9D	OSR	Status Register
X:$FF FF9E	OSCNTR (24 bits)	Instruction Step Counter
X:$FF FF9F	—	Instruction Step Counter
X:$FF FFA0	OCR (bits)	Control Register
		Reserved
X:$FF FFFC	OCLSR (8 bits)	Core Lock / Unlock Status Register
X:$FF FFFD	OTXRXSR (8 bits)	Transmit and Receive Status and Control Register
X:$FF FFFE	OTX / ORX (32 bits)	Transmit Register / Receive Register
X:$FF FFFF	OTX1 / ORX1	Transmit Register Upper Word Receive Register Upper Word

4.7 Peripheral Memory Mapped Registers

On-chip peripheral registers are part of the data memory map on the 56800E series. These locations may be accessed with the same addressing modes used for ordinary Data memory, except all peripheral registers should be read/written using word accesses only.

Table 4-7 summarizes base addresses for the set of peripherals on the 56F8322 and 56F8122 devices. Peripherals are listed in order of the base address.

Table 4-13 Analog to Digital Converter Registers Address Map (Continued) (ADCA_BASE = $00 F200)

Register Acronym	Address Offset	Register Description
ADCA_HLMT 1	$1A	High Limit Register 1
ADCA_HLMT 2	$1B	High Limit Register 2
ADCA_HLMT 3	$1C	High Limit Register 3
ADCA_HLMT 4	$1D	High Limit Register 4
ADCA_HLMT 5	$1E	High Limit Register 5
ADCA_HLMT 6	$1F	High Limit Register 6
ADCA_HLMT 7	$20	High Limit Register 7
ADCA_OFS 0	$21	Offset Register 0
ADCA_OFS 1	$22	Offset Register 1
ADCA_OFS 2	$23	Offset Register 2
ADCA_OFS 3	$24	Offset Register 3
ADCA_OFS 4	$25	Offset Register 4
ADCA_OFS 5	$26	Offset Register 5
ADCA_OFS 6	$27	Offset Register 6
ADCA_OFS 7	$28	Offset Register 7
ADCA_POWER	$29	Power Control Register
ADCA_CAL	$2A	ADC Calibration Register

Table 4-14 Temperature Sensor Register Address Map (TSENSOR_BASE = $00 F270) *Temperature Sensor is NOT available in the 56F8122 device*

Register Acronym	Address Offset	Register Description
TSENSOR_CNTL	$0	Control Register

Table 4-15 Serial Communication Interface 0 Registers Address Map (SCI0_BASE = $00 F280)

Register Acronym	Address Offset	Register Description
SCI0_SCIBR	$0	Baud Rate Register
SCI0_SCICR	$1	Control Register
		Reserved
SCI0_SCISR	$3	Status Register
SCI0_SCIDR	$4	Data Register

Table 4-16 Serial Communication Interface 1 Registers Address Map (SCI1_BASE = $00 F290)

Register Acronym	Address Offset	Register Description
SCI1_SCIBR	$0	Baud Rate Register
SCI1_SCICR	$1	Control Register
		Reserved
SCI1_SCISR	$3	Status Register
SCI1_SCIDR	$4	Data Register

Table 4-17 Serial Peripheral Interface 0 Registers Address Map (SPI0_BASE = $00 F2A0)

Register Acronym	Address Offset	Register Description
SPI0_SPSCR	$0	Status and Control Register
SPI0_SPDSR	$1	Data Size Register
SPI0_SPDRR	$2	Data Receive Register
SPI0_SPDTR	$3	Data Transmitter Register

Table 4-18 Serial Peripheral Interface 1 Registers Address Map (SPI1_BASE = $00 F2B0)

Register Acronym	Address Offset	Register Description
SPI1_SPSCR	$0	Status and Control Register
SPI1_SPDSR	$1	Data Size Register
SPI1_SPDRR	$2	Data Receive Register
SPI1_SPDTR	$3	Data Transmitter Register

Table 4-19 Computer Operating Properly Registers Address Map (COP_BASE = $00 F2C0)

Register Acronym	Address Offset	Register Description
COPCTL	$0	Control Register
COPTO	$1	Time-Out Register
COPCTR	$2	Counter Register

Table 4-27 FlexCAN Registers Address Map (Continued)
(FC_BASE = $00 F800)
FlexCAN is NOT available in the 56F8122 device

Register Acronym	Address Offset	Register Description
FCMB7_DATA	$7C	Message Buffer 7 Data Register
FCMB7_DATA	$7D	Message Buffer 7 Data Register
FCMB7_DATA	$7E	Message Buffer 7 Data Register
		Reserved
FCMB8_CONTROL	$80	Message Buffer 8 Control / Status Register
FCMB8_ID_HIGH	$81	Message Buffer 8 ID High Register
FCMB8_ID_LOW	$82	Message Buffer 8 ID Low Register
FCMB8_DATA	$83	Message Buffer 8 Data Register
FCMB8_DATA	$84	Message Buffer 8 Data Register
FCMB8_DATA	$85	Message Buffer 8 Data Register
FCMB8_DATA	$86	Message Buffer 8 Data Register
		Reserved
FCMB9_CONTROL	$88	Message Buffer 9 Control / Status Register
FCMB9_ID_HIGH	$89	Message Buffer 9 ID High Register
FCMB9_ID_LOW	$8A	Message Buffer 9 ID Low Register
FCMB9_DATA	$8B	Message Buffer 9 Data Register
FCMB9_DATA	$8C	Message Buffer 9 Data Register
FCMB9_DATA	$8D	Message Buffer 9 Data Register
FCMB9_DATA	$8E	Message Buffer 9 Data Register
		Reserved
FCMB10_CONTROL	$90	Message Buffer 10 Control / Status Register
FCMB10_ID_HIGH	$91	Message Buffer 10 ID High Register
FCMB10_ID_LOW	$92	Message Buffer 10 ID Low Register
FCMB10_DATA	$93	Message Buffer 10 Data Register
FCMB10_DATA	$94	Message Buffer 10 Data Register
FCMB10_DATA	$95	Message Buffer 10 Data Register
FCMB10_DATA	$96	Message Buffer 10 Data Register
		Reserved
FCMB11_CONTROL	$98	Message Buffer 11 Control / Status Register
FCMB11_ID_HIGH	$99	Message Buffer 11 ID High Register
FCMB11_ID_LOW	$9A	Message Buffer 11 ID Low Register
FCMB11_DATA	$9B	Message Buffer 11 Data Register
FCMB11_DATA	$9C	Message Buffer 11 Data Register
FCMB11_DATA	$9D	Message Buffer 11 Data Register
FCMB11_DATA	$9E	Message Buffer 11 Data Register
		Reserved

5.6.3.1 Flash Memory Command, Data, Address Buffers Empty Interrupt Priority Level (FMCBE IPL)—Bits 15–14

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.3.2 Flash Memory Command Complete Priority Level (FMCC IPL)—Bits 13–12

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.3.3 Flash Memory Error Interrupt Priority Level (FMERR IPL)—Bits 11–10

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.3.4 PLL Loss of Lock Interrupt Priority Level (LOCK IPL)—Bits 9–8

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.10.5 ADC A Zero Crossing or Limit Error Interrupt Priority Level (ADCA_ZC IPL)—Bits 7–6

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.10.6 Reserved—Bits 5–4

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.10.7 ADC A Conversion Complete Interrupt Priority Level (ADCA_CC IPL)—Bits 3–2

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.10.8 Reserved—Bits 1–0

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.11 Vector Base Address Register (VBA)

Base + $A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	VECTOR BASE ADDRESS												
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-13 Vector Base Address Register (VBA)

5.6.11.1 Reserved—Bits 15–13

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.11.2 Interrupt Vector Base Address (VECTOR BASE ADDRESS)—Bits 12–0

The contents of this register determine the location of the Vector Address Table. The value in this register is used as the upper 13 bits of the interrupt vector address. The lower eight bits of the ISR address are determined based upon the highest-priority interrupt; see **Section 5.3.1** for details.

5.6.14.2 Fast Interrupt 0 Vector Address High (FIVAH0)—Bits 4–0

The upper five bits of the vector address used for Fast Interrupt 0. This register is combined with FIVAL0 to form the 21-bit vector address for Fast Interrupt 0 defined in the FIM0 register.

5.6.15 Fast Interrupt 1 Match Register (FIM1)

Base + $E	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 1						
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-17 Fast Interrupt 1 Match Register (FIM1)

5.6.15.1 Reserved—Bits 15–7

This bit field is reserved or not implemented. It is read as 0, but cannot be modified by writing.

5.6.15.2 Fast Interrupt 1 Vector Number (FAST INTERRUPT 1)—Bits 6–0

This value determines which IRQ will be a Fast Interrupt 1. Fast interrupts vector directly to a service routine based on values in the Fast Interrupt Vector Address registers without having to go to a jump table first; see **Section 5.3.3** for details. IRQs used as fast interrupts *must* be set to priority level 2. Unexpected results will occur if a fast interrupt vector is set to any other priority. Fast interrupts automatically become the highest-priority level 2 interrupt, regardless of their location in the interrupt table, prior to being declared as fast interrupt. Fast Interrupt 0 has priority over Fast Interrupt 1. To determine the vector number of each IRQ, refer to **Table 4-3**.

5.6.16 Fast Interrupt 1 Vector Address Low Register (FIVAL1)

Base + $F	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	FAST INTERRUPT 1 VECTOR ADDRESS LOW															
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-18 Fast Interrupt 1 Vector Address Low Register (FIVAL1)

5.6.16.1 Fast Interrupt 1 Vector Address Low (FIVAL1)—Bits 15–0

The lower 16 bits of the vector address used for Fast Interrupt 1. This register is combined with FIVAH1 to form the 21-bit vector address for Fast Interrupt 1 defined in the FIM1 register.

5.6.17 Fast Interrupt 1 Vector Address High Register (FIVAH1)

Base + $10	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 1 VECTOR ADDRESS HIGH				
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-19 Fast Interrupt 1 Vector Address High Register (FIVAH1)

5.6.20 IRQ Pending 2 Register (IRQP2)

Base + $13	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	PENDING [48:33]															
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 5-22 IRQ Pending 2 Register (IRQP2)

5.6.20.1 IRQ Pending (PENDING)—Bits 48–33

This register combines with the other five to represent the pending IRQs for interrupt vector numbers 2 through 81.

- 0 = IRQ pending for this vector number
- 1 = No IRQ pending for this vector number

5.6.21 IRQ Pending 3 Register (IRQP3)

Base + $14	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	PENDING [64:49]															
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 5-23 IRQ Pending 3 Register (IRQP3)

5.6.21.1 IRQ Pending (PENDING)—Bits 64–49

This register combines with the other five to represent the pending IRQs for interrupt vector numbers 2 through 81.

- 0 = IRQ pending for this vector number
- 1 = No IRQ pending for this vector number

5.6.22 IRQ Pending 4 Register (IRQP4)

Base + $15	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	PENDING [80:65]															
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 5-24 IRQ Pending 4 Register (IRQP4)

5.6.22.1 IRQ Pending (PENDING)—Bits 80–65

This register combines with the other five to represent the pending IRQs for interrupt vector numbers 2 through 81.

- 0 = IRQ pending for this vector number
- 1 = No IRQ pending for this vector number

5.7 Resets

5.7.1 Reset Handshake Timing

The ITCN provides the 56800E core with a reset vector address whenever $\overline{\text{RESET}}$ is asserted. The reset vector will be presented until the second rising clock edge after $\overline{\text{RESET}}$ is released.

5.7.2 ITCN After Reset

After reset, all of the ITCN registers are in their default states. This means all interrupts are disabled, except the core IRQs with fixed priorities:

- Illegal Instruction
- SW Interrupt 3
- HW Stack Overflow
- Misaligned Long Word Access
- SW Interrupt 2
- SW Interrupt 1
- SW Interrupt 0
- SW Interrupt LP

These interrupts are enabled at their fixed priority levels.

Part 6 System Integration Module (SIM)

6.1 Introduction

The SIM module is a system catchall for the glue logic that ties together the system-on-chip. It controls distribution of resets and clocks and provides a number of control features. The system integration module is responsible for the following functions:

- Reset sequencing
- Clock control & distribution
- Stop/Wait control
- Pull-up enables for selected peripherals
- System status registers
- Registers for software access to the JTAG ID of the chip
- Enforcing Flash security

These are discussed in more detail in the sections that follow.

6.5.2.3 COP Reset (COPR)—Bit 4

When 1, the COPR bit indicates the Computer Operating Properly (COP) timer-generated reset has occurred. This bit will be cleared by a Power-On Reset or by software. Writing a 0 to this bit position will set the bit, while writing a 1 to the bit will clear it.

6.5.2.4 External Reset (EXTR)—Bit 3

If 1, the EXTR bit indicates an external system reset has occurred. This bit will be cleared by a Power-On Reset or by software. Writing a 0 to this bit position will set the bit while writing a 1 to the bit position will clear it. Basically, when the EXTR bit is 1, the previous system reset was caused by the external $\overline{\text{RESET}}$ pin being asserted low.

6.5.2.5 Power-On Reset (POR)—Bit 2

When 1, the POR bit indicates a Power-On Reset occurred some time in the past. This bit can be cleared only by software or by another type of reset. Writing a 0 to this bit will set the bit, while writing a 1 to the bit position will clear the bit. In summary, if the bit is 1, the previous system reset was due to a Power-On Reset.

6.5.2.6 Reserved—Bits 1–0

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.3 SIM Software Control Registers (SIM_SCR0, SIM_SCR1, SIM_SCR2, and SIM_SCR3)

Only SIM_SCR0 is shown in this section. SIM_SCR1, SIM_SCR2, and SIM_SCR3 are identical in functionality.

Base + $2	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	FIELD															
Write																
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-5 SIM Software Control Register 0 (SIM_SCR0)

6.5.3.1 Software Control Data 1 (FIELD)—Bits 15–0

This register is reset only by the Power-On Reset (POR). It has no part-specific functionality and is intended for use by a software developer to contain data that will be unaffected by the other reset sources ($\overline{\text{RESET}}$ pin, software reset, and COP reset).

As shown in **Figure 6-10**, the GPIO has the final control over which pin controls the I/O. SIM_GPS simply decides which peripheral will be routed to the I/O.

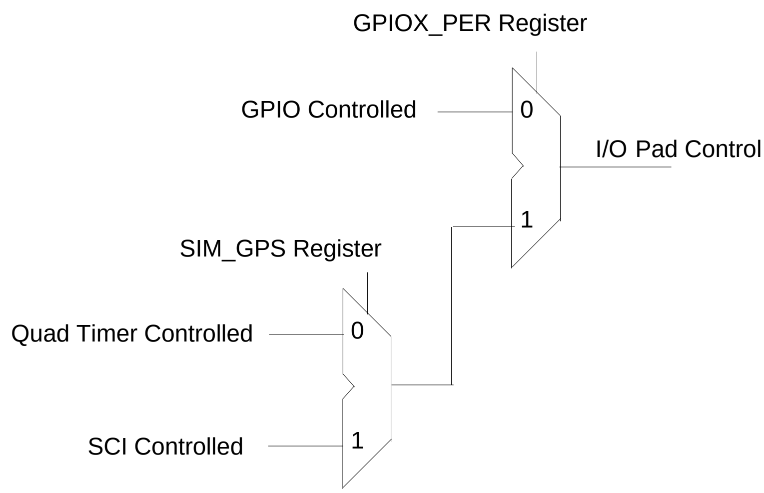

Figure 6-10 Overall Control of Pads Using SIM_GPS Control

Base + $B	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	C6	C5	B1	B0	A5	A4	A3	A2
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-11 GPIO Peripheral Select Register (SIM_GPS)

6.5.8.1 Reserved—Bits 15–8

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.8.2 GPIO C6 (C6)—Bit 7

This bit selects the alternate function for GPIOC6.

- 0 = TC0 (default)
- 1 = TXD0

6.5.8.3 GPIOC5 (C5)—Bit 6

This bit selects the alternate function for GPIOC5.

- 0 = TC1 (default)
- 1 = RXD0

6.8 Stop and Wait Mode Disable Function

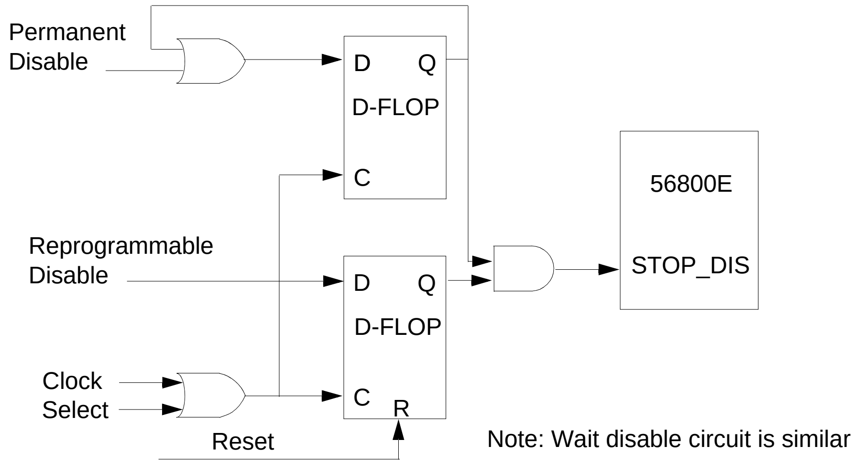

Figure 6-16 Internal Stop Disable Circuit

The 56800E core contains both STOP and WAIT instructions. Both put the CPU to sleep. For lowest power consumption in Stop mode, the PLL can be shut down. This must be done explicitly before entering Stop mode, since there is no automatic mechanism for this. When the PLL is shut down, the 56800E system clock must be set equal to the prescaler output.

Some applications require the 56800E STOP and WAIT instructions be disabled. To disable those instructions, write to the SIM control register (SIM_CONTROL) described in **Section 6.5.1** . This procedure can be on either a permanent or temporary basis. Permanently assigned applications last only until their next reset.

6.9 Resets

The SIM supports four sources of reset. The two asynchronous sources are the external $\overline{\text{RESET}}$ pin and the Power-On Reset (POR). The two synchronous sources are the software reset, which is generated within the SIM itself, by writing to the SIM_CONTROL register, and the COP reset.

Reset begins with the assertion of any of the reset sources. Release of reset to various blocks is sequenced to permit proper operation of the device. A POR reset is declared when reset is removed and any of the three voltage detectors (1.8V POR, 2.2V core voltage, or 2.7V I/O voltage) indicate a low supply voltage condition. POR will continue to be asserted until all voltage detectors indicate a stable supply is available (note that as power is removed POR is not declared until the 1.8V core voltage threshold is reached.) A POR reset is then extended for 64 clock cycles to permit stabilization of the clock source, followed by a 32 clock window in which SIM clocking is initiated. It is then followed by a 32 clock window in which peripherals are released to implement Flash security, and, finally, followed by a 32 clock window in which the core is initialized. After completion of the described reset sequence, application code will begin execution.

Resets may be asserted asynchronously, but are always released internally on a rising edge of the system clock.

Note: *The 56F8122 device is specified to meet Industrial requirements only; PWM, CAN and Quad Decoder are NOT available on the 56F8122 device.*

Table 10-1 Absolute Maximum Ratings

($V_{SS} = V_{SSA\_ADC} = 0$)

Characteristic	Symbol	Notes	Min	Max	Unit
Supply voltage	V_{DD_IO}		- 0.3	4.0	V
ADC Supply Voltage	V_{DDA_ADC}, V_{REFH}	V_{REFH} must be less than or equal to V_{DDA_ADC}	- 0.3	4.0	V
Oscillator / PLL Supply Voltage	$V_{DDA\_OSC\_PLL}$		- 0.3	4.0	V
Internal Logic Core Supply Voltage	V_{DD_CORE}	OCR_DIS is High	- 0.3	3.0	V
Input Voltage (digital)	V_{IN}	Pin Groups 1, 3, 4, 5	-0.3	6.0	V
Input Voltage (analog)	V_{INA}	Pin Group 7	-0.3	4.0	V
Output Voltage	V_{OUT}	Pin Groups 1, 2, 3	-0.3	4.0 6.0[1]	V
Output Voltage (open drain)	V_{OD}	GPIO pins used in open drain mode	-0.3	6.0	V
Ambient Temperature (Automotive)	T_A		-40	125	°C
Ambient Temperature (Industrial)	T_A		-40	105	°C
Junction Temperature (Automotive)	T_J		-40	150	°C
Junction Temperature (Industrial)	T_J		-40	125	°C
Storage Temperature (Automotive)	T_{STG}		-55	150	°C
Storage Temperature (Industrial)	T_{STG}		-55	150	°C

1. If corresponding GPIO pin is configured as open drain.

Note: *Pins in italics are NOT available in the 56F8122 device.*

Pin Group 1: TC0-1, *FAULTA0*, $\overline{\text{SS0}}$, MISO0, MOSI0, SCLK0, *HOME0*, *INDEX0*, *PHASEA0*, *PHASEB0*, *CAN_RX*, *CAN_TX*

Pin Group 2: TDO

Pin Group 3: *PWMA0-5*

Pin Group 4: $\overline{\text{RESET}}$, TMS, TDI, $\overline{\text{IRQA}}$

Pin Group 5: TCK

Pin Group 6: XTAL, EXTAL

Pin Group 7: ANA0-6

10.10 Quad Timer Timing

Table 10-19 Timer Timing[1, 2]

Characteristic	Symbol	Min	Max	Unit	See Figure
Timer input period	P_{IN}	2T + 6	—	ns	10-13
Timer input high / low period	P_{INHL}	1T + 3	—	ns	10-13
Timer output period	P_{OUT}	1T - 3	—	ns	10-13
Timer output high / low period	P_{OUTHL}	0.5T - 3	—	ns	10-13

1. In the formulas listed, T = the clock cycle. For 60MHz operation, T = 16.67ns.
2. Parameters listed are guaranteed by design.

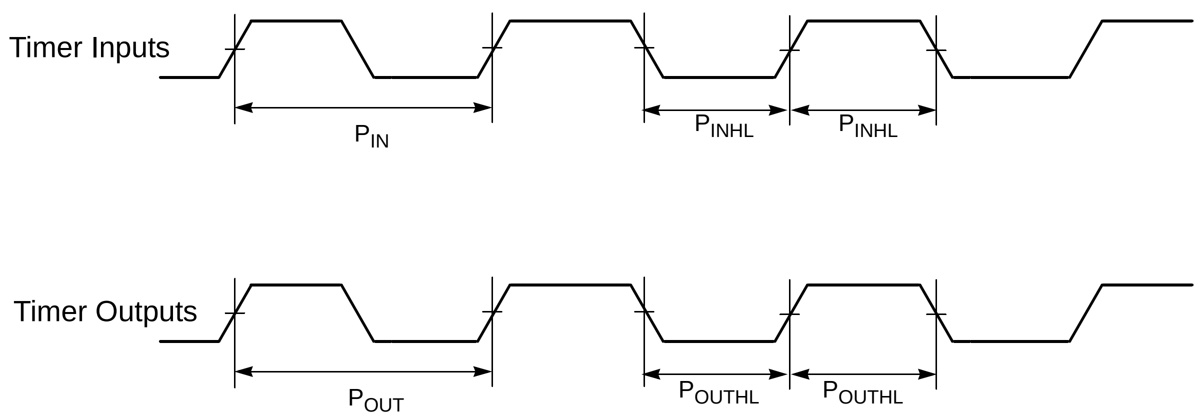

Figure 10-13 Timer Timing

10.11 Quadrature Decoder Timing

Note: *The Quadrature Decoder is NOT available in the 56F8122 device.*

Table 10-20 Quadrature Decoder Timing[1, 2]

Characteristic	Symbol	Min	Max	Unit	See Figure
Quadrature input period	P_{IN}	4T + 12	—	ns	10-14
Quadrature input high / low period	P_{HL}	2T + 6	—	ns	10-14
Quadrature phase period	P_{PH}	1T + 3	—	ns	10-14

1. In the formulas listed, T = the clock cycle. For 60MHz operation, T=16.67ns.
2. Parameters listed are guaranteed by design.

Part 11 Packaging

11.1 56F8322 Package and Pin-Out Information

This section contains package and pin-out information for the 56F8322. This device comes in a 48-pin Low-profile Quad Flat Pack (LQFP). **Figure 11-1** shows the package outline for the 48-pin LQFP, **Figure 12-1** shows the mechanical parameters for this package, and **Table 11-1** lists the pin-out for the 48-pin LQFP.

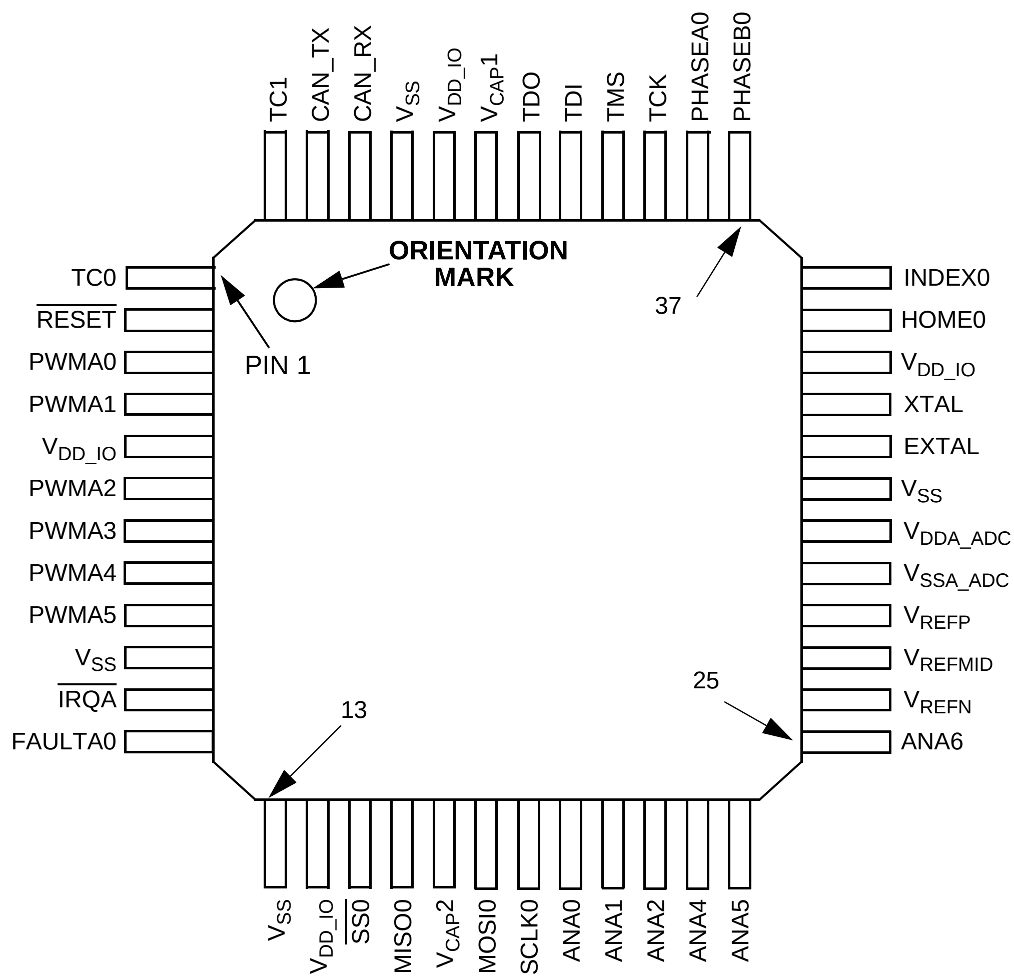

Figure 11-1 Top View, 56F8322 48-Pin LQFP Package