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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details	
Product Status	Active
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, SCI, UART/USART
Peripherals	POR, WDT
Number of I/O	34
Program Memory Size	64KB (64K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90387pmt-g-152

1. Product Lineup

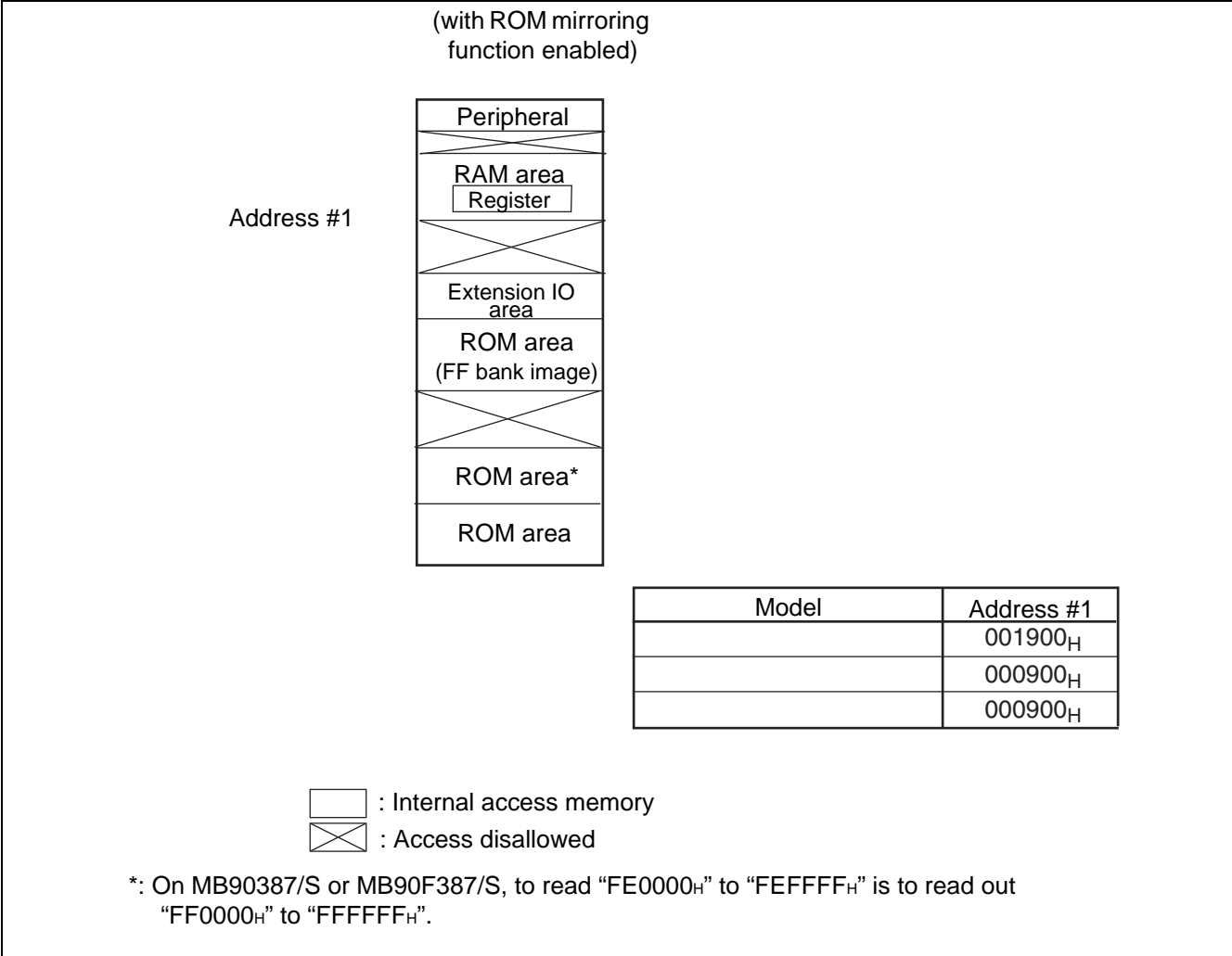| Part Number / Parameter	MB90F387 MB90F387S	MB90387 MB90387S	MB90V495G
Classification	Flash ROM	Mask ROM	Evaluation product
ROM capacity	64 Kbytes		−
RAM capacity	2 Kbytes		6 Kbytes
Process	CMOS		
Package	LQFP-48 (pin pitch 0.50 mm)		PGA-256
Operating power supply voltage	3.5 V to 5.5 V		4.5 V to 5.5 V
Special power supply for emulator*1	−		None
CPU functions	Number of basic instructions : 351 instructions Instruction bit length : 8 bits and 16 bits Instruction length : 1 byte to 7 bytes Data bit length : 1 bit, 8 bits, 16 bits		
	Minimum instruction execution time: 62.5 ns (at 16 MHz machine clock)		
	Interrupt processing time: 1.5 μs at minimum (at 16 MHz machine clock)		
Low power consumption (standby) mode	Sleep mode / Watch mode / Time-base timer mode / Stop mode / CPU intermittent		
I/O port	General-purpose input/output ports (CMOS output): 34 ports (36 ports*2) including 4 high-current output ports (P14 to P17)		
Time-base timer	18-bit free-run counter Interrupt cycle: 1.024 ms, 4.096 ms, 16.834 ms, 131.072 ms (with oscillation clock frequency at 4 MHz)		
Watchdog timer	Reset generation cycle: 3.58 ms, 14.33 ms, 57.23 ms, 458.75 ms (with oscillation clock frequency at 4 MHz)		
16-bit input/ output timer	16-bit free-run timer	Number of channels: 1 Interrupt upon occurrence of overflow	
	Input capture	Number of channels: 4 Retaining free-run timer value set by pin input (rising edge, falling edge, and both edges)	
16-bit reload timer	Number of channels: 2 16-bit reload timer operation Count clock cycle: 0.25 μs, 0.5 μs, 2.0 μs (at 16-MHz machine clock frequency) External event count is allowed.		
Watch timer	15-bit free-run counter Interrupt cycle: 31.25 ms, 62.5 ms, 12 ms, 250 ms, 500 ms, 1.0 s, 2.0 s (with 8.192 kHz sub clock)		
8/16-bit PPG timer	Number of channels: 2 (four 8-bit channels are available also.) PPG operation is allowed with four 8-bit channels or two 16-bit channels. Outputting pulse wave of arbitrary cycle or arbitrary duty is allowed. Count clock: 62.5 ns to 1 μs (with 16 MHz machine clock)		
Delay interrupt generator module	Interrupt generator module for task switching. Used for realtime OS.		
DTP/External interrupt	Number of inputs: 4 Activated by rising edge, falling edge, "H" level or "L" level input. External interrupt or expanded intelligent I/O service (EI²OS) is available.		

Pin No.	Pin Name	Circuit Type	Function
39	P42	D	General-purpose input/output port.
	SOT1		Serial data input pin for UART. Valid only when serial data input/output setting on UART is "enabled."
40	P43	D	General-purpose input/output port.
	TX		Transmission output pin for CAN. Valid only when output setting is "enabled."
41	P44	D	General-purpose input/output port.
	RX		Transmission output pin for CAN. Valid only when output setting is "enabled."
42 to 45	P30 to P33	D	General-purpose input/output ports.
46	X0A*	A	Pin for low-rate oscillation.
	P35*		General-purpose input/output port.
47	X1A*	A	Pin for low-rate oscillation.
	P36*		General-purpose input/output port.
48	AVss	–	Vss power source input pin for A/D converter.

*: MB90387, MB90F387:   X1A, X0A
   MB90387S, MB90F387S: P36, P35

6. I/O Circuit Type

Type	Circuit	Remarks
A	X1 X1A X0 X0A → Clock input / Standby control signal	■ High-rate oscillation feedback resistor, approx.1 MΩ ■ Low-rate oscillation feedback resistor, approx.10 MΩ
B	Vcc, R, R → Hysteresis input	■ Hysteresis input with pull-up resistor. ■ Pull-up resistor, approx.50 kΩ
C	R → Hysteresis input	■ Hysteresis input
D	Vcc, P-ch Digital output, N-ch Digital output, Vss, R, CMOS hysteresis input, Standby control	■ CMOS hysteresis input ■ CMOS level output ■ Standby control provided
E	Vcc, P-ch Digital output, N-ch Digital output, Vss, R, CMOS hysteresis input, Standby control, Analog input	■ CMOS hysteresis input ■ CMOS level output ■ Shared for analog input pin ■ Standby control provided

9.2 Memory Map

(with ROM mirroring
function enabled)

Address #1

Peripheral
RAM area
Register
Extension IO area
ROM area (FF bank image)
ROM area*
ROM area

Model	Address #1
	001900$_H$
	000900$_H$
	000900$_H$

☐ : Internal access memory

⊠ : Access disallowed

*: On MB90387/S or MB90F387/S, to read "FE0000$_H$" to "FEFFFF$_H$" is to read out "FF0000$_H$" to "FFFFFF$_H$".

Note: When internal ROM is operating, F²MC-16LX allows viewing ROM data image on FF bank at upper-level of 00 bank. This function is called "mirroring ROM," which allows effective use of C compiler small model.

F²MC-16LX assigns the same low order 16-bit address to FF bank and 00 bank, which allows referencing table in ROM without specifying "far" using pointer.

For example, when accessing to "00C000$_H$", ROM data at "FFC000$_H$" is accessed actually. However, because ROM area of FF bank exceeds 48 Kbytes, viewing all areas is not possible on 00 bank image. Because ROM data of "FF4000$_H$" to "FFFFFF$_H$" is viewed on "004000$_H$" to "00FFFF$_H$" image, store a ROM data table in area "FF4000$_H$" to "FFFFFF$_H$."

Address	Register Abbreviation	Register	Read/Write	Resource	Initial Value
$0000B0_H$	ICR00	Interrupt control register 00	R/W	Interrupt controller	00000111_B
$0000B1_H$	ICR01	Interrupt control register 01			00000111_B
$0000B2_H$	ICR02	Interrupt control register 02			00000111_B
$0000B3_H$	ICR03	Interrupt control register 03			00000111_B
$0000B4_H$	ICR04	Interrupt control register 04			00000111_B
$0000B5_H$	ICR05	Interrupt control register 05			00000111_B
$0000B6_H$	ICR06	Interrupt control register 06			00000111_B
$0000B7_H$	ICR07	Interrupt control register 07			00000111_B
$0000B8_H$	ICR08	Interrupt control register 08			00000111_B
$0000B9_H$	ICR09	Interrupt control register 09			00000111_B
$0000BA_H$	ICR10	Interrupt control register 10			00000111_B
$0000BB_H$	ICR11	Interrupt control register 11			00000111_B
$0000BC_H$	ICR12	Interrupt control register 12			00000111_B
$0000BD_H$	ICR13	Interrupt control register 13			00000111_B
$0000BE_H$	ICR14	Interrupt control register 14			00000111_B
$0000BF_H$	ICR15	Interrupt control register 15			00000111_B
$0000C0_H$ to $0000FF_H$	(Reserved area) *				
$001FF0_H$	PADR0	Detection address setting register 0 (low-order)	R/W	Address matching detection function	$XXXXXXXX_B$
$001FF1_H$		Detection address setting register 0 (middle-order)			$XXXXXXXX_B$
$001FF2_H$		Detection address setting register 0 (high-order)			$XXXXXXXX_B$
$001FF3_H$	PADR1	Detection address setting register 1 (low-order)	R/W		$XXXXXXXX_B$
$001FF4_H$		Detection address setting register 1 (middle-order)			$XXXXXXXX_B$
$001FF5_H$		Detection address setting register 1 (high-order)			$XXXXXXXX_B$
003900_H	TMR0/ TMRLR0	16-bit timer register 0/16-bit reload register	R,W	16-bit reload timer 0	$XXXXXXXX_B$
003901_H					$XXXXXXXX_B$
003902_H	TMR1/ TMRLR1	16-bit timer register 1/16-bit reload register	R,W	16-bit reload timer 1	$XXXXXXXX_B$
003903_H					$XXXXXXXX_B$
003904_H to $00390F_H$	(Reserved area) *				

Port 4 Pins Block Diagram

Standby control: Control among Stop mode (SPL=1), Time-base timer mode (SPL=1), and watch mode (SPL=1).
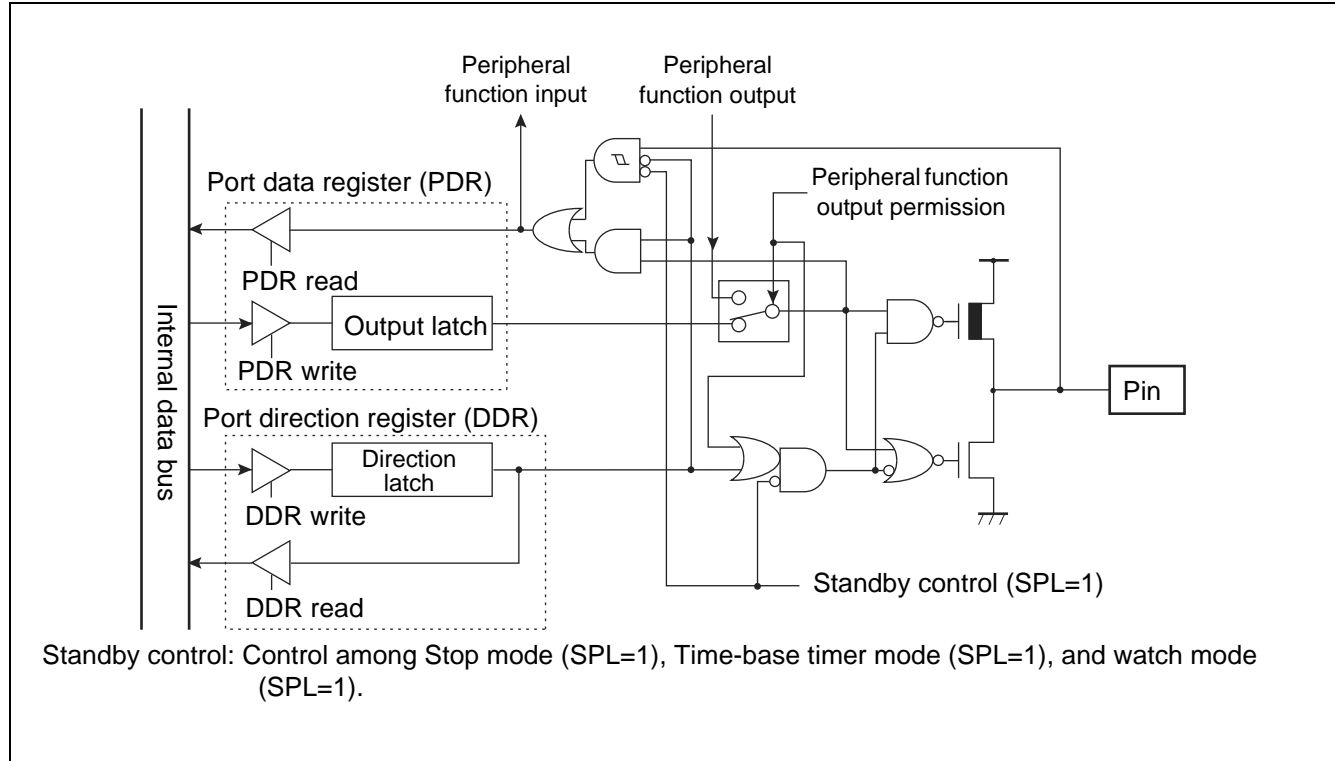
Port 4 Registers

■ Port 4 registers include port 4 data register (PDR4) and port 4 direction register (DDR4).

■ The bits configuring the register correspond to port 4 pins on a one-to-one basis.

Relation between Port 4 Registers and Pins

Port Name	Bits of Register and Corresponding Pins							
Port 4	PDR4, DDR4	–	–	–	bit4	bit3	bit2	bit1	bit0
	Corresponding pins	–	–	–	P44	P43	P42	P41	P40

Port 5 Pins Block Diagram

Standby control: Control among Stop mode (SPL=1), Time-base timer mode (SPL=1), and watch mode (SPL=1).
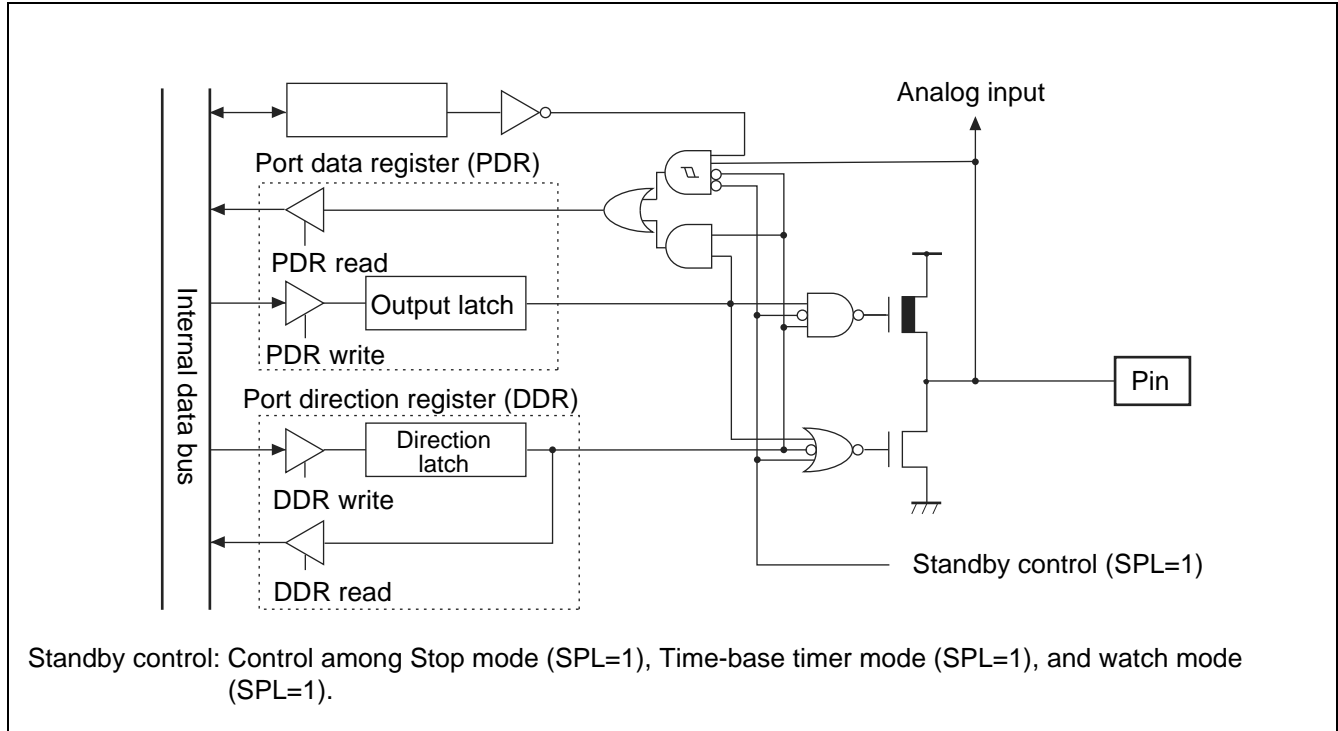
Port 5 Registers

■ Port 5 registers include port 5 data register (PDR5), port 5 direction register (DDR5), and analog input permission register (ADER).

■ Analog input permission register (ADER) allows or disallows input of analog signal to the analog input pin.

■ The bits configuring the register correspond to port 5 pins on a one-to-one basis.

Relation between Port 5 Registers and Pins

Port Name	Bits of Register and Corresponding Pins								
Port 5	PDR5, DDR5	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	ADER	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
	Corresponding pins	P57	P56	P55	P54	P53	P52	P51	P50

Input Capture Block Diagram
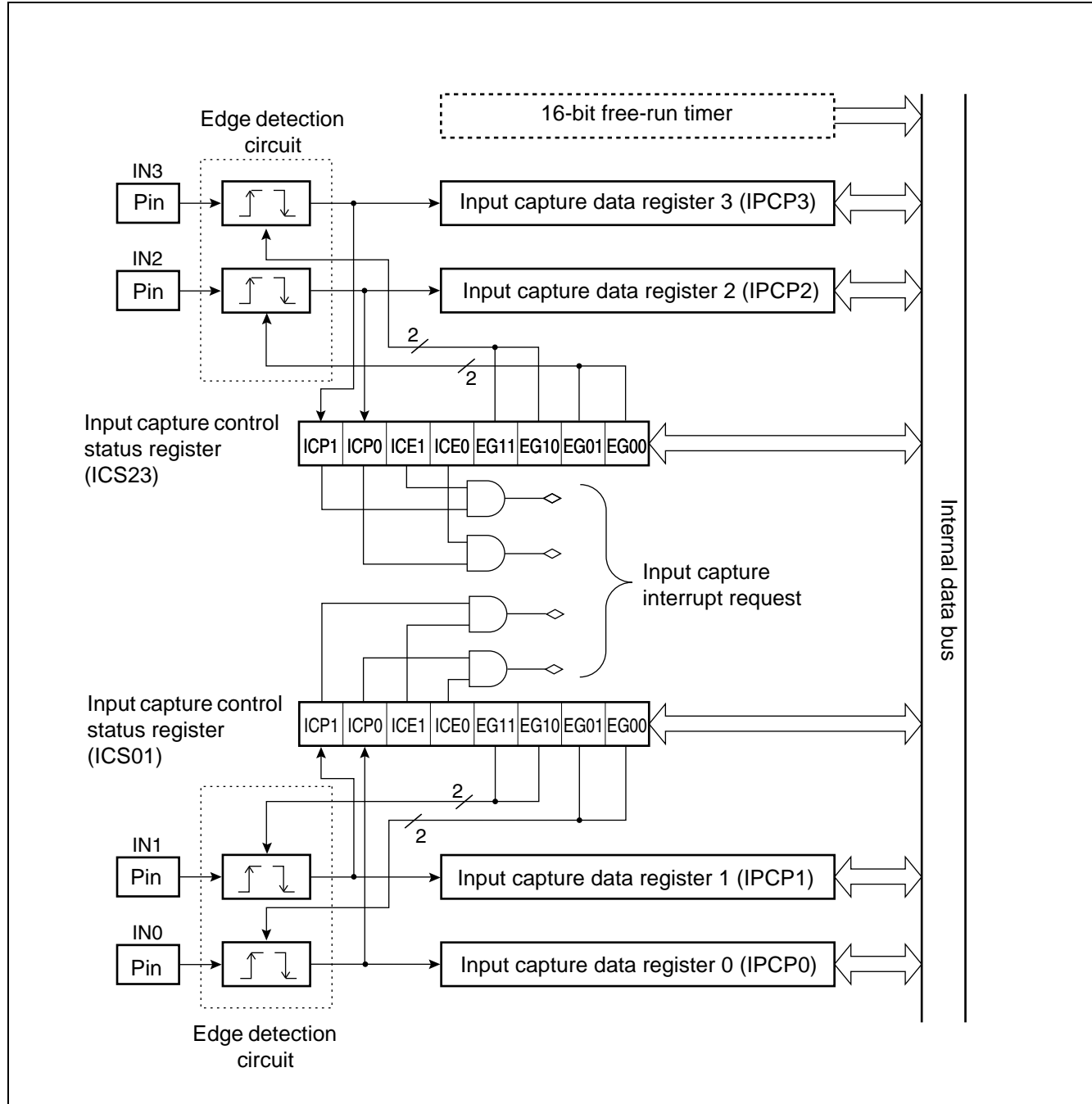
12.5 16-bit Reload Timer

The 16-bit reload timer has the following functions:

■ Count clock is selectable among 3 internal clocks and external event clock.

■ Activation trigger is selectable between software trigger and external trigger.

■ Generation of CPU interrupt is allowed upon occurrence of underflow on 16-bit timer register. Available as an interval timer using the interrupt function.

■ When underflow of 16-bit timer register (TMR) occurs, one of two reload modes is selectable between one-shot mode that halts counting operation of TMR, and reload mode that reloads 16-bit reload register value to TMR, continuing TMR counting operation.

■ The 16-bit reload timer is ready for expanded intelligent I/O service (EI²OS).

■ MB90385 series device has 2 channels of built-in 16-bit reload timer.

Operation Mode of 16-bit Reload Timer

Count Clock	Activation Trigger	Operation upon Underflow
Internal clock mode	Software trigger, external trigger	One-shot mode, reload mode
Event count mode	Software trigger	One-shot mode, reload mode

Internal Clock Mode

■ The 16-bit reload timer is set to internal clock mode, by setting count clock selection bit (TMCSR: CSL1, CSL0) to "00$_B$", "01$_B$", "10$_B$".

■ In the internal clock mode, the counter decrements in synchronization with the internal clock.

■ Three types of count clock cycles are selectable by count clock selection bit (TMCSR: CSL1, CSL0) in timer control status register.

■ Edge detection of software trigger or external trigger is specified as an activation trigger.

12.7 8/16-bit PPG Timer Outline

The 8/16-bit PPG timer is a 2-channel reload timer module (PPG0 and PPG1) that allows outputting pulses of arbitrary cycle and duty cycle. Combination of the two channels allows selection among the following operations:

■ 8-bit PPG output 2-channel independent operation mode

■ 16-bit PPG output operation mode

■ 8-bit and 8-bit PPG output operation mode

MB90385 series device has two 8/16-bit built-in PPG timers. This section describes functions of PPG0/1. PPG2/3 have the same functions as those of PPG0/1.

Functions of 8/16-bit PPG Timer

The 8/16-bit PPG timer is composed of four 8-bit reload register (PRLH0/PRLL0, PRLH1/PRLL1) and two PPG down counters (PCNT0, PCNT1).

■ Widths of "H" and "L" in output pulse are specifiable independently. Cycle and duty factor of output pulse is specifiable arbitrarily.

■ Count clock is selectable among 6 internal clocks.

■ The timer is usable as an interval timer, by generating interrupt requests for each interval.

■ The time is usable as a D/A converter, with an external circuit.

12.10 8/10-bit A/D Converter

The 8/10-bit A/D converter converts an analog input voltage into 8-bit or 10/bit digital value, using the RC-type successive approximation conversion method.

■ Input signal is selected among 8 channels of analog input pins.

■ Activation trigger is selected among software trigger, internal timer output, and external trigger.

Functions of 8/10-bit A/D Converter

The 8/10-bit A/D converter converts an analog voltage (input voltage) input to analog input pin into an 8-bit or 10-bit digital value (A/D conversion).

The 8/10-bit A/D converter has the following functions:

■ A/D conversion takes a minimum of 6.12 μs* for 1 channel, including sampling time. (A/D conversion)

■ Sampling of one channel takes a minimum of 2.0 μs*.

■ RC-type successive approximation conversion method, with sample & hold circuit is used for conversion.

■ Resolution of either 8 bits or 10 bits is specifiable.

■ A maximum of 8 channels of analog input pins are allowed for use.

■ Generation of interrupt request is allowed, by storing A/D conversion result in A/D data register.

■ Activation of EI²OS is allowed upon occurrence of an interrupt request. With use of EI²OS, data loss is avoided even if A/D conversion is performed successively.

■ An activation trigger is selectable among software trigger, internal timer output, and external trigger (fall edge).

: When operating with 16 MHz machine clock

8/10-bit A/D Converter Conversion Mode

Conversion Mode	Description
Singular conversion mode	The A/D conversion is performed form a start channel to an end channel sequentially. Upon completion of A/D conversion on an end channel, A/D conversion function stops.
Sequential conversion mode	The A/D conversion is performed form a start channel to an end channel sequentially. Upon completion of A/D conversion on an end channel, A/D conversion function resumes from the start channel.
Pausing conversion mode	The A/D conversion is performed by pausing at each channel. Upon completion of A/D conversion on an end channel, A/D conversion and pause functions resume from the start channel.

8/10-bit A/D Converter Block Diagram

TO   : Internal timer output
−   : Not defined
Reserved: Be sure to set to "0"
φ   : Machine clock
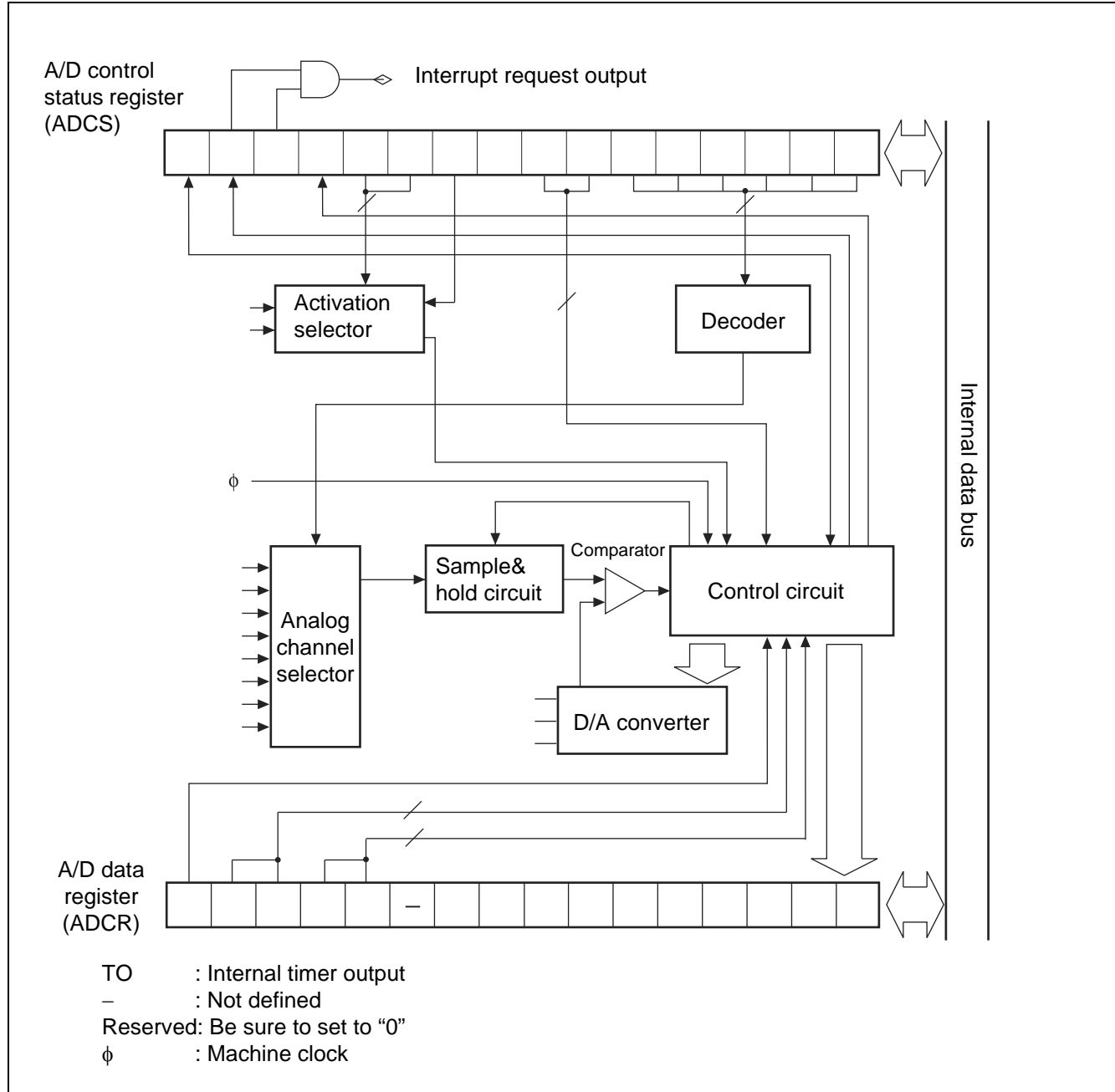
CAN Controller Block Diagram
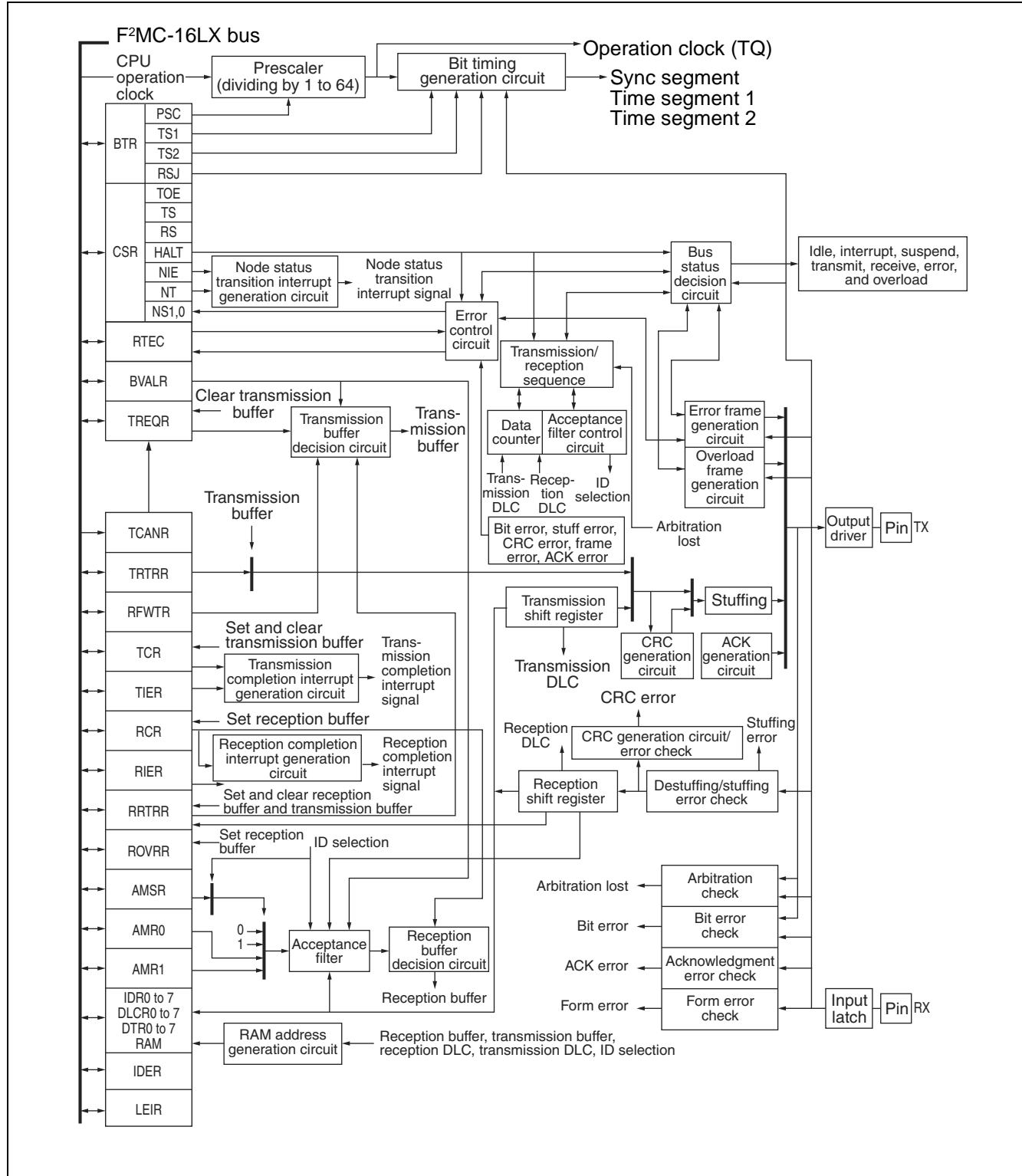
■ Use within recommended operating conditions.

■ Use at DC voltage (current).

■ The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.

■ The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.

■ Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.

■ Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.

■ Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.

■ Care must be taken not to leave the +B input pin open.

■ Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.

■ Sample recommended circuits:
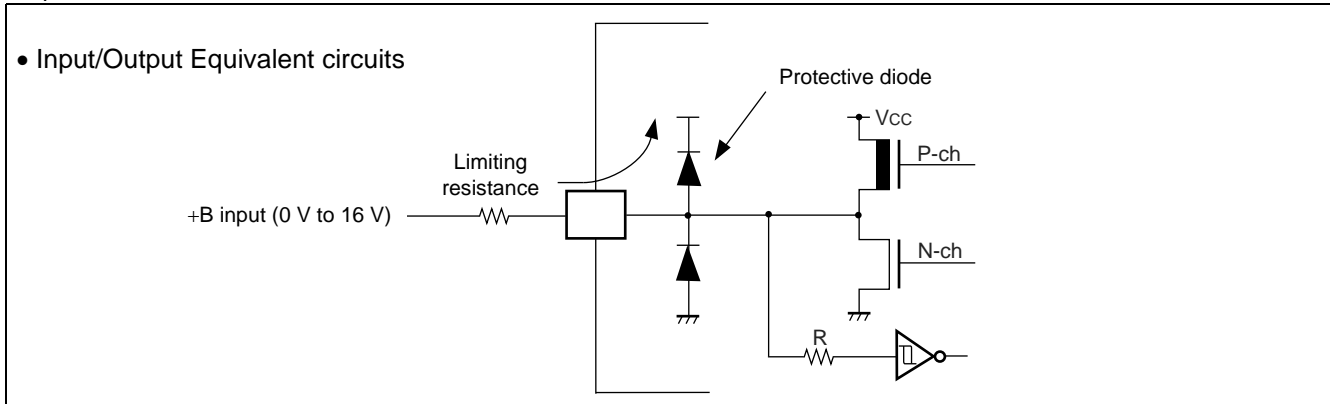
WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

$(V_{CC} = 5.0\ V \pm 10\%,\ V_{SS} = AV_{SS} = 0.0\ V,\ T_A = -40\ °C\ to\ +105\ °C)$

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*	I_{CCL}	V_{CC}	$V_{CC} = 5.0\ V$, Internally operating at 8 kHz, subclock operation, $T_A = +25°C$	—	0.3	1.2	mA	MB90F387/S
				—	40	100	μA	MB90387/S
	I_{CCLS}		$V_{CC} = 5.0\ V$, Internally operating at 8 kHz, subclock, sleep mode, $T_A = +25°C$	—	10	30	μA	
	I_{CCT}		$V_{CC} = 5.0\ V$, Internally operating at 8 kHz, watch mode, $T_A = +25°C$	—	8	25	μA	
	I_{CCH}		Stopping, $T_A = +25°C$	—	5	20	μA	
Input capacity	C_{IN}	Other than AV_{CC}, AV_{SS}, AVR, C, V_{CC}, V_{SS}	–	—	5	15	pF	
Pull-up resistor	R_{UP}	RST	–	25	50	100	kΩ	
Pull-down resistor	R_{DOWN}	MD2	–	25	50	100	kΩ	Flash product is not provided with pull-down resistor.

*: Test conditions of power supply current are based on a device using external clock.

• Internal shift clock mode
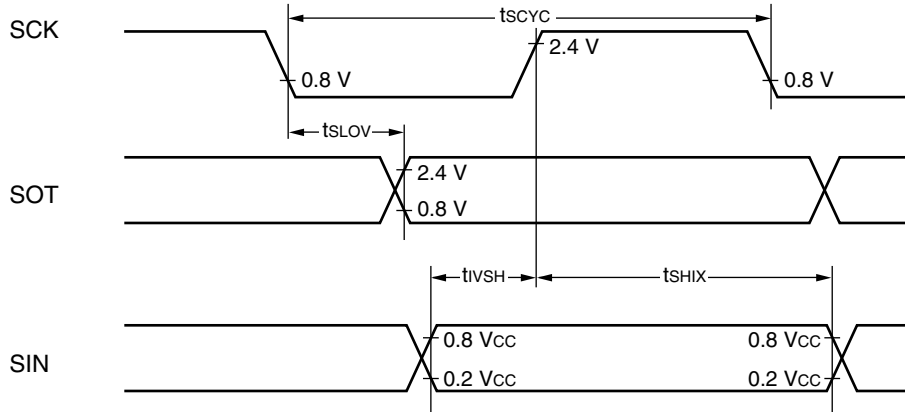
• External shift clock mode
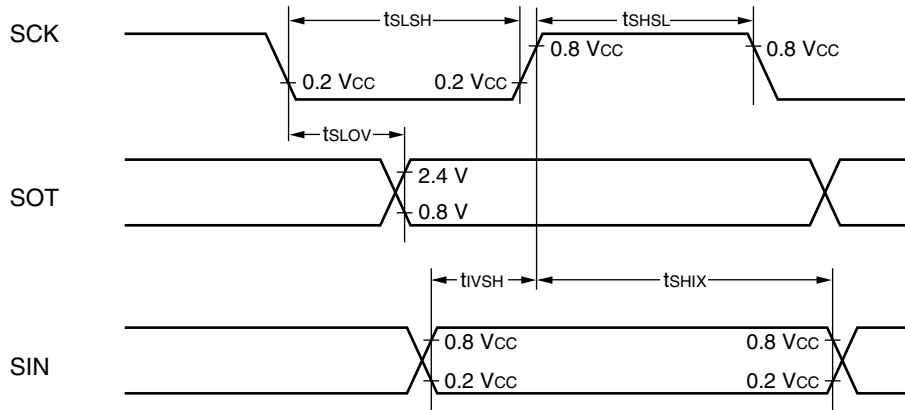
13.4.5 Timer Input Timing

$(V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}, V_{SS} = 0.0 \text{ V}, T_A = -40 °C \text{ to } +105 °C)$

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	**Max**		
Input pulse width	t_{TIWH}	TIN0, TIN1	–	$4 \, t_{CP}$ *	–	ns	
	t_{TIWL}	IN0 to IN3					

*: Refer to Clock Timing ratings for t_{CP} (internal operation clock cycle time).

13.7 Notes on A/D Converter Section

Use the device with external circuits of the following output impedance for analog inputs:

Recommended output impedance of external circuits are: Approx. 3.9 kΩ or lower (4.5 V ≤ AVcc ≤ 5.5 V) (sampling period=2.00 μs at 16 MHz machine clock), Approx. 11 kΩ or lower (4.0 V ≤ AVcc < 4.5 V) (sampling period=8.0 μs at 16 MHz machine clock).

If an external capacitor is used, in consideration of the effect by tap capacitance caused by external capacitors and on-chip capacitors, capacitance of the external one is recommended to be several thousand times as high as internal capacitor.

If output impedance of an external circuit is too high, a sampling period for an analog voltage may be insufficient.

- Analog input circuit model

Analog input — R — • — Comparator

C
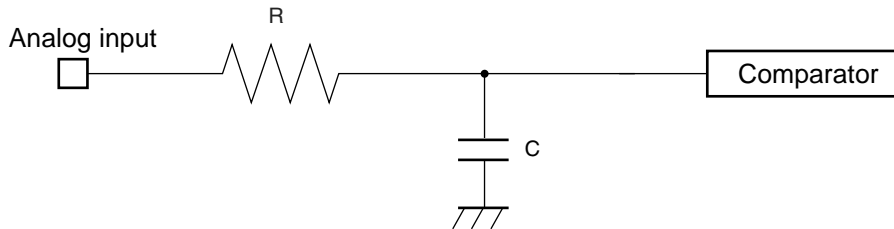
MB90F387/S, MB90387/S
4.5 V ≤ AVcc ≤ 5.5 V   R ≅ 2.35 kΩ, C ≅ 36.4 pF
4.0 V ≤ AVcc < 4.5 V   R ≅ 16.4 kΩ, C ≅ 36.4 pF

Note: Use the values in the figure only as a guideline.

About errors

As [AVR-AVss] become smaller, values of relative errors grow larger.

13.8 Flash Memory Program/Erase Characteristics

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	$T_A = +25$ °C $V_{CC} = 5.0$ V	–	1	15	s	Excludes 00H programming prior to erasure
Chip erase time		–	4	–	s	Excludes 00H programming prior to erasure
Word (16-bit width) programming time		–	16	3,600	μs	Except for the over head time of the system
Program/Erase cycle	–	10,000	–	–	cycle	
Flash Data Retention Time	Average $T_A = +85$ °C	20	–	–	Year	*

*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C).

I_{CCLS} − V_{CC}

T_A = +25 °C, In external clock operation
f = Internal operating frequency

f = 8 kHz

I_{CCT} − V_{CC}

T_A = +25 °C, In external clock operation
f = Internal operating frequency

f = 8 kHz

I_{CCH} − V_{CC}

Stopping, T_A = +25 °C
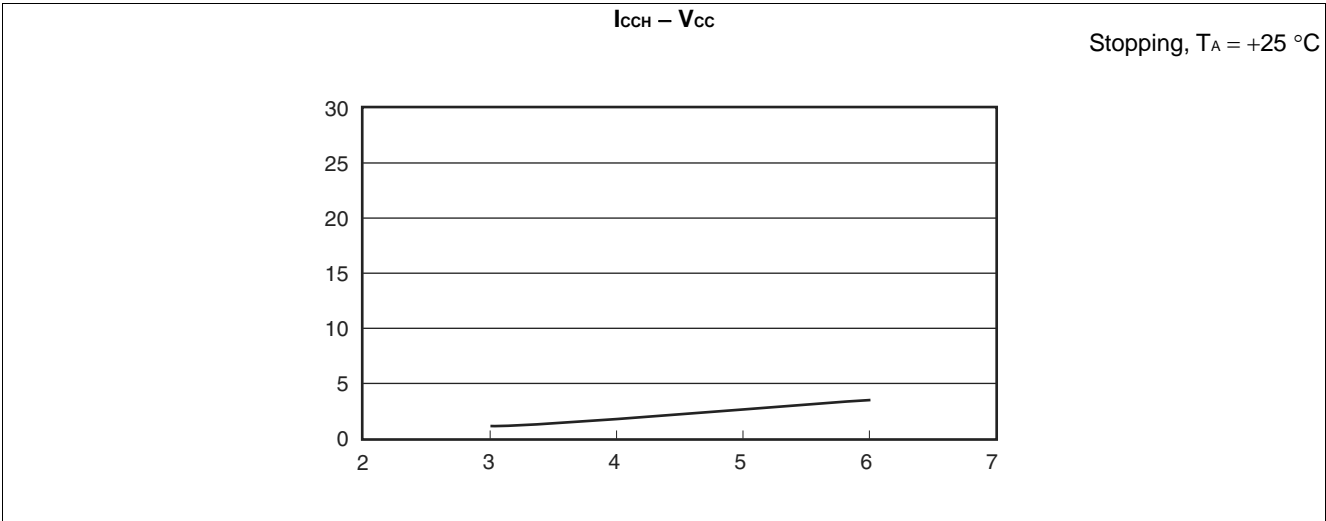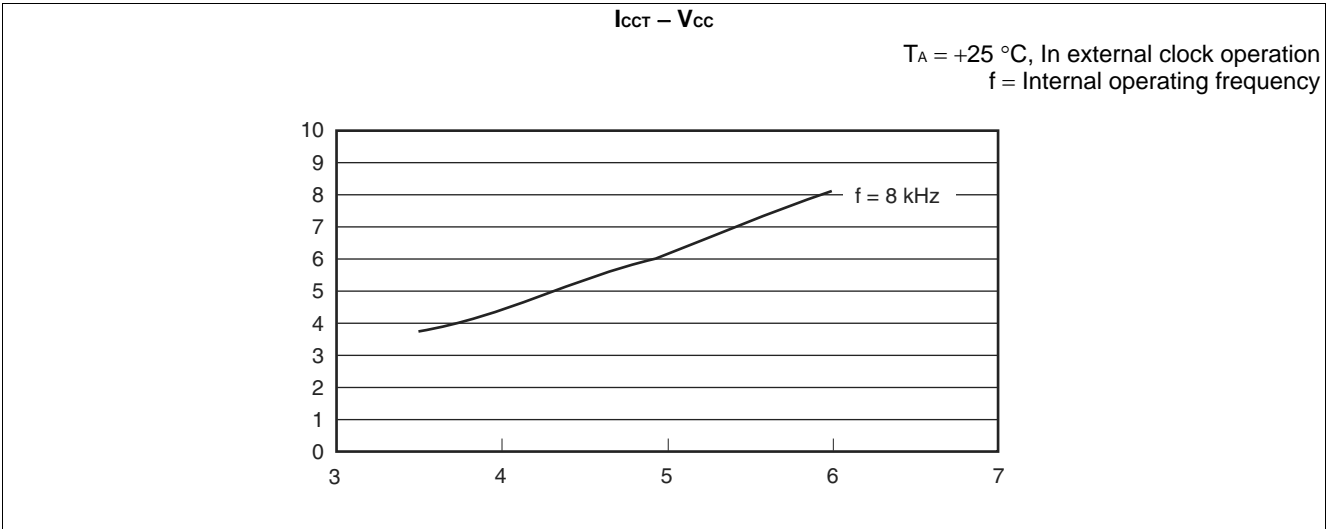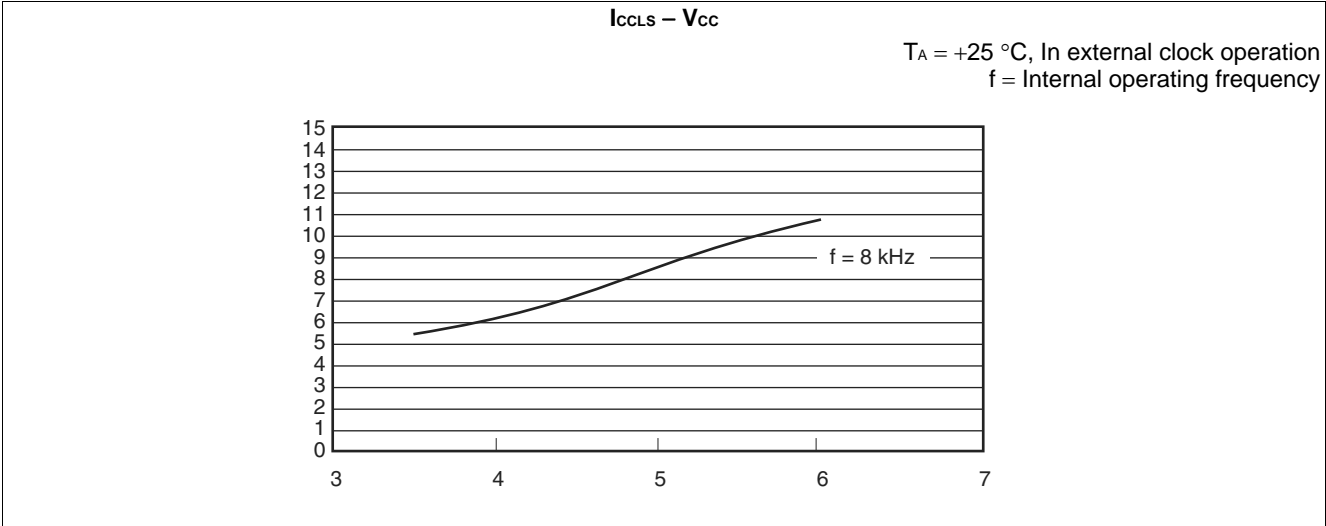
(Continued)

Document History

Document Title: MB90387/387S/F387/F387S, MB90V495G, 16-bit Microcontrollers F²MC-16LX MB90385 Series **Document Number:002-07765**				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	—	AKIH	12/19/2008	Migrated to Cypress and assigned document number 002-07765. No change to document contents or format.
*A	6059071	SSAS	02/05/2018	Updated to Cypress template Package: FPT-48P-M26 --> LQA048

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