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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, SCI, UART/USART
Peripherals	POR, WDT
Number of I/O	34
Program Memory Size	64KB (64K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90387pmt-g-184

Parameter \ Part Number	MB90F387 MB90F387S	MB90387 MB90387S	MB90V495G
8/10-bit A/D converter	Number of channels: 8 Resolution: Selectable 10-bit or 8-bit. Conversion time: 6.125 μs (at 16 MHz machine clock, including sampling time) Sequential conversion of two or more successive channels is allowed. (Setting a maximum of 8 channels is allowed.) Single conversion mode: Selected channel is converted only once. Sequential conversion mode: Selected channel is converted repetitively. Halt conversion mode: Conversion of selected channel is stopped and activated alternately.		
UART(SCI)	Number of channels: 1 Clock-synchronous transfer: 62.5 kbps to 2 Mbps Clock-asynchronous transfer: 9,615 bps to 500 kbps Communication is allowed by bi-directional serial communication function and master/slave type connection.		
CAN	Compliant with Ver 2.0A and Ver 2.0B CAN specifications. 8 built-in message buffers. Transmission rate of 10 kbps to 1 Mbps (by 16 MHz machine clock) CAN wake-up		

*1: Settings of DIP switch S2 for using emulation pod MB2145-507. For details, see MB2145-507 Hardware Manual (2.7 Power Pin solely for Emulator).

*2: MB90387S, MB90F387S

2. Packages And Product Models

Package	MB90F387, MB90F387S	MB90387, MB90387S
LQA048	◯	◯

◯: Yes ×: No

Note: Refer to Package Dimension for details of the package.

3. Product Comparison

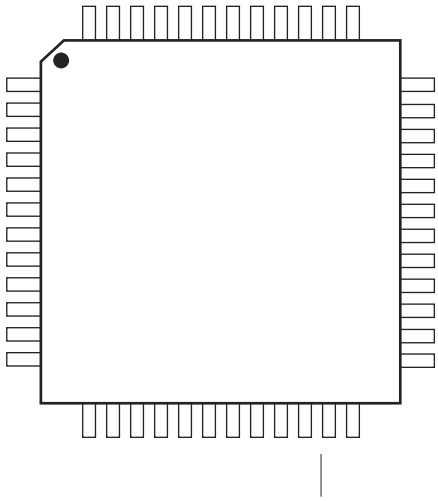
Memory Space

When testing with test product for evaluation, check the differences between the product and a product to be used actually. Pay attention to the following points:

- The MB90V495G has no built-in ROM. However, a special-purpose development tool allows the operations as those of one with built-in ROM. ROM capacity depends on settings on a development tool.
- On MB90V495G, an image from $FF4000_H$ to $FFFFFF_H$ is viewed on 00 bank and an image of $FE0000_H$ to $FF3FFF_H$ is viewed only on FE bank and FF bank. (Modified on settings of a development tool.)
- On MB90F387/F387S/387/387S, an image from $FF4000_H$ to $FFFFFF_H$ is viewed on 00 bank and an image of $FE0000_H$ to $FF3FFF_H$ is viewed only on FF bank.

4. Pin Assignment

(Top View)



(LQA048)

*: MB90387, MB90F387 : X1A, X0A
MB90387S, MB90F387S: P36, P35

Notes When Using No Sub Clock

■ If an oscillator is not connected to X0A and X1A pin, apply pull-down resistor to X0A pin and leave X1A pin open.

About Power Supply Pins

■ If two or more Vcc and Vss pins exist, the pins that should be at the same potential are connected to each other inside the device. For reducing unwanted emissions and preventing malfunction of strobe signals caused by increase of ground level, however, be sure to connect the Vcc and Vss pins to the power source and the ground externally.

■ Pay attention to connect a power supply to Vcc and Vss of MB90385 series device in a lowest-possible impedance.

■ Near pins of MB90385 series device, connecting a bypass capacitor is recommended at 0.1 μF across Vcc pin and Vss pin.

Crystal Oscillator Circuit

■ Noises around X0 and X1 pins cause malfunctions on a MB90385 series device. Design a print circuit so that X0 and X1 pins, an crystal oscillator (or a ceramic oscillator), and bypass capacitor to the ground become as close as possible to each other. Furthermore, avoid wires to X0 and X1 pins crossing each other as much as possible.

■ Print circuit designing that surrounds X0 and X1 pins with grounding wires, which ensures stable operation, is strongly recommended.

Caution on Operations during PLL Clock Mode

■ If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

Sequence of Turning on Power of A/D Converter and Applying Analog Input

■ Be sure to turn on digital power (Vcc) before applying signals to the A/D converter and applying analog input signals (AN0 to AN7 pins).

■ Be sure to turn off the power of A/D converter and analog input before turning off the digital power source.

■ Be sure not to apply AVR exceeding AVcc when turning on and off. (No problems occur if analog and digital power is turned on and off simultaneously.)

Handling Pins When A/D Converter is Not Used

■ If the A/D converter is not used, connect the pins under the following conditions: “AVcc=AVR=Vcc,” and “AVss=Vss”

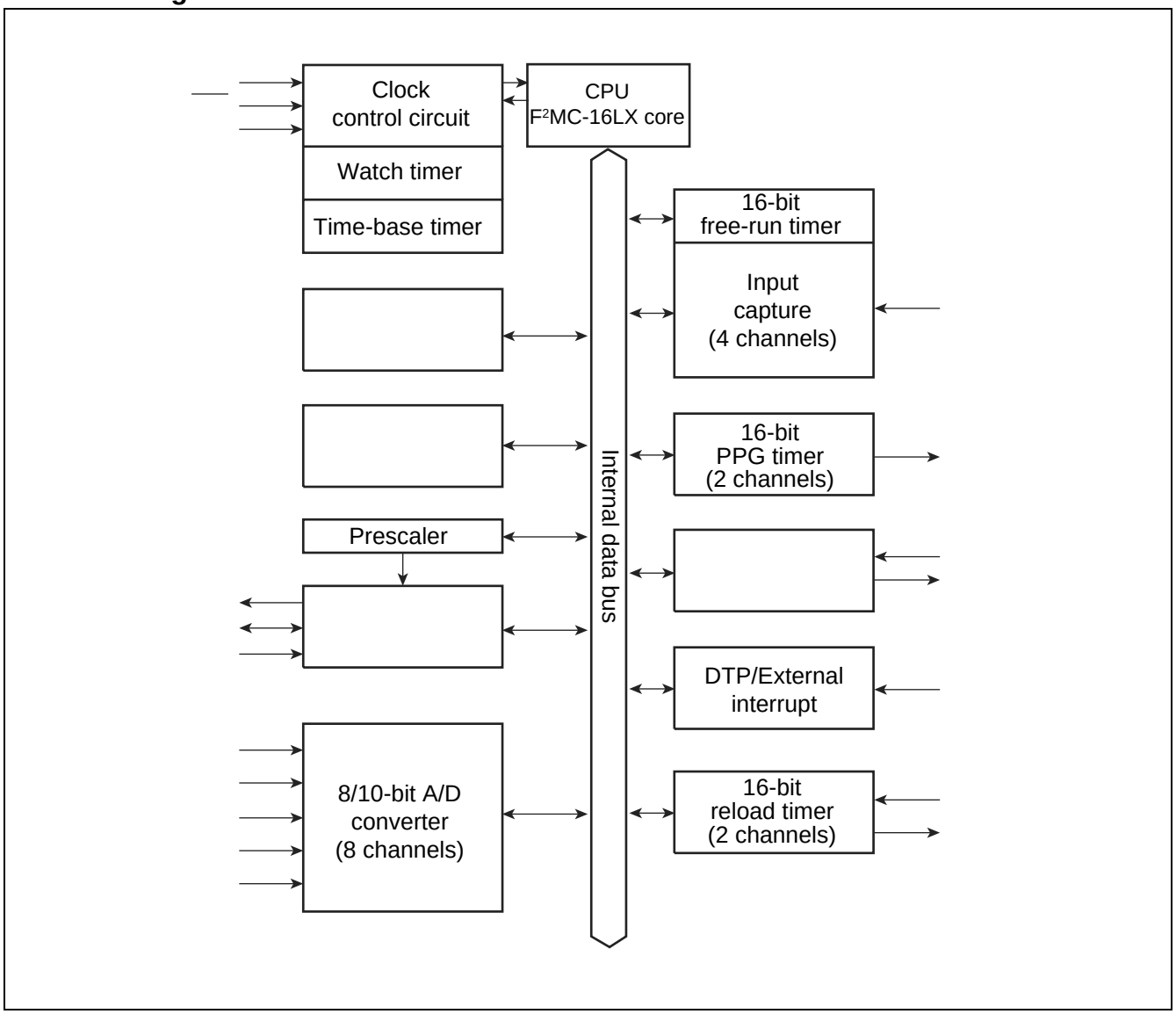
Note on Turning on Power

■ For preventing malfunctions on built-in step-down circuit, maintain a minimum of 50 μs of voltage rising time (between 0.2 V and 2.7V) when turning on the power.

Stabilization of Supply Voltage

■ A sudden change in the supply voltage may cause the device to malfunction even within the specified V_{CC} supply voltage operating range. Therefore, the V_{CC} supply voltage should be stabilized.
For reference, the supply voltage should be controlled so that V_{CC} ripple variations (peak-to-peak values) at commercial frequencies (50 Hz / 60 Hz) fall below 10% of the standard V_{CC} supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

8. Block Diagram



9. Memory Map

MB90385 series allows specifying a memory access mode “single chip mode.”

9.1 Memory Allocation of MB90385

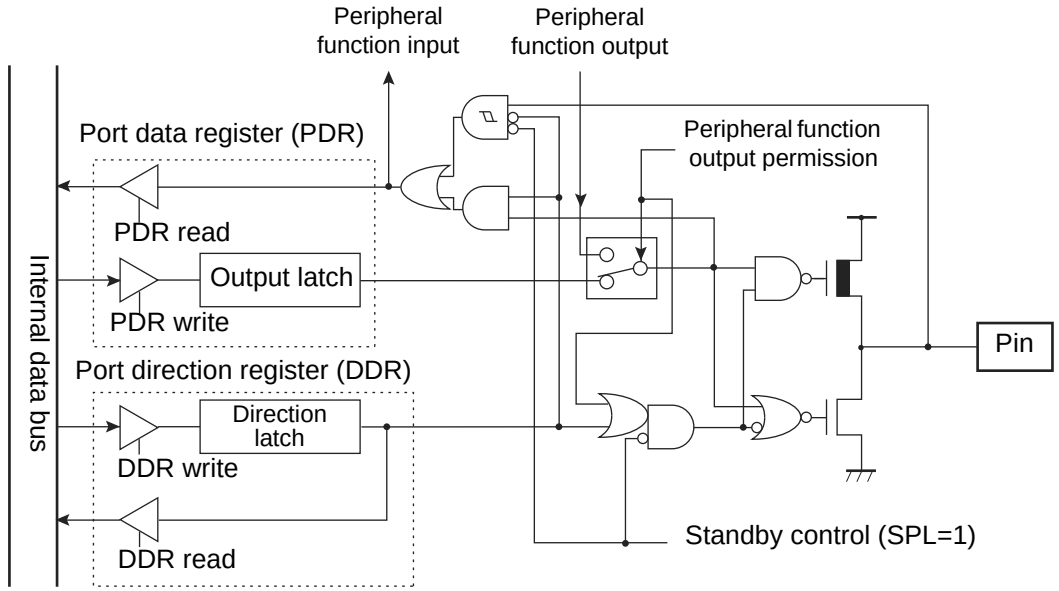
MB90385 series model has 24-bit wide internal address bus and up to 24-bit bus of external address bus.
A maximum of 16-Mbyte memory space of external access memory is accessible.

Address	Register Abbreviation	Register	Read/ Write	Resource	Initial Value
003C38H, 003C39H	DLCR4	DLC register 4	R/W	CAN controller	XXXXXXXXB, XXXXXXXXB
003C3AH, 003C3BH	DLCR5	DLC register 5	R/W		XXXXXXXXB, XXXXXXXXB
003C3CH, 003C3DH	DLCR6	DLC register 6	R/W		XXXXXXXXB, XXXXXXXXB
003C3EH, 003C3FH	DLCR7	DLC register 7	R/W		XXXXXXXXB, XXXXXXXXB
003C40H to 003C47H	DTR0	Data register 0	R/W		XXXXXXXXB to XXXXXXXXB
003C48H to 003C4FH	DTR1	Data register 1	R/W		XXXXXXXXB to XXXXXXXXB
003C50H to 003C57H	DTR2	Data register 2	R/W		XXXXXXXXB to XXXXXXXXB
003C58H to 003C5FH	DTR3	Data register 3	R/W		XXXXXXXXB to XXXXXXXXB
003C60H to 003C67H	DTR4	Data register 4	R/W		XXXXXXXXB to XXXXXXXXB
003C68H to 003C6FH	DTR5	Data register 5	R/W		XXXXXXXXB to XXXXXXXXB
003C70H to 003C77H	DTR6	Data register 6	R/W		XXXXXXXXB to XXXXXXXXB
003C78H to 003C7FH	DTR7	Data register 7	R/W		XXXXXXXXB to XXXXXXXXB
003C80H to 003CFFH	(Reserved area) *				
003D00H, 003D01H	CSR	Control status register	R/W, R	CAN controller	0XXXX001B, 00XXX000B
003D02H	LEIR	Last event display register	R/W		000XX000B
003D03H	(Reserved area) *				
003D04H, 003D05H	RTEC	Send/receive error counter	R	CAN controller	00000000B, 00000000B
003D06H, 003D07H	BTR	Bit timing register	R/W		11111111B, X1111111B
003D08H	IDER	IDE register	R/W		XXXXXXXXB
003D09H	(Reserved area) *				
003D0AH	TRTRR	Send RTR register	R/W	CAN controller	00000000B
003D0BH	(Reserved area) *				
003D0CH	RFWTR	Remote frame receive wait register	R/W	CAN controller	XXXXXXXXB

11. Interrupt Sources, Interrupt Vectors, And Interrupt Control Registers

Interrupt Source	EI²OS Readiness	Interrupt Vector			Interrupt Control Register		Priority*3
		Number		Address	ICR	Address	
Reset	×	#08	08H	FFFFDCH	–	–	High
INT 9 instruction	×	#09	09H	FFFFD8H	–	–	↑
Exceptional treatment	×	#10	0AH	FFFFD4H	–	–	
CAN controller reception completed (RX)	´	#11	0BH	FFFFD0H	ICR00	0000B0H*1	
CAN controller transmission completed (TX) / Node status transition (NS)	´	#12	0CH	FFFFCCH			
Reserved	×	#13	0DH	FFFFC8H	ICR01	0000B1H	
Reserved	×	#14	0EH	FFFFC4H			
CAN wakeup	Δ	#15	0FH	FFFFC0H	ICR02	0000B2H*1	
Time-base timer	×	#16	10H	FFFFBCH			
16-bit reload timer 0	Δ	#17	11H	FFFFB8H	ICR03	0000B3H*1	
8/10-bit A/D converter	Δ	#18	12H	FFFFB4H			
16-bit free-run timer overflow	Δ	#19	13H	FFFFB0H	ICR04	0000B4H*1	
Reserved	×	#20	14H	FFFFACH			
Reserved	×	#21	15H	FFFFA8H	ICR05	0000B5H*1	
PPG timer ch0, ch1 underflow	´	#22	16H	FFFFA4H			
Input capture 0-input	Δ	#23	17H	FFFFA0H	ICR06	0000B6H*1	
External interrupt (INT4/INT5)	Δ	#24	18H	FFFF9CH			
Input capture 1-input	Δ	#25	19H	FFFF98H	ICR07	0000B7H*2	
PPG timer ch2, ch3 underflow	´	#26	1AH	FFFF94H			
External interrupt (INT6/INT7)	Δ	#27	1BH	FFFF90H	ICR08	0000B8H*1	
Watch timer	Δ	#28	1CH	FFFF8CH			
Reserved	×	#29	1DH	FFFF88H	ICR09	0000B9H*1	
Input capture 2-input Input capture 3-input	´	#30	1EH	FFFF84H			
Reserved	×	#31	1FH	FFFF80H	ICR10	0000BAH*1	
Reserved	×	#32	20H	FFFF7CH			
Reserved	×	#33	21H	FFFF78H	ICR11	0000BBH*1	
Reserved	×	#34	22H	FFFF74H			
Reserved	×	#35	23H	FFFF70H	ICR12	0000BCH*1	↓
16-bit reload timer 1	○	#36	24H	FFFF6CH			Low

Port 2 Pins Block Diagram (general-purpose input/output port)



Standby control: Control among Stop mode (SPL=1), Time-base timer mode (SPL=1), and watch mode (SPL=1).

Port 2 Registers

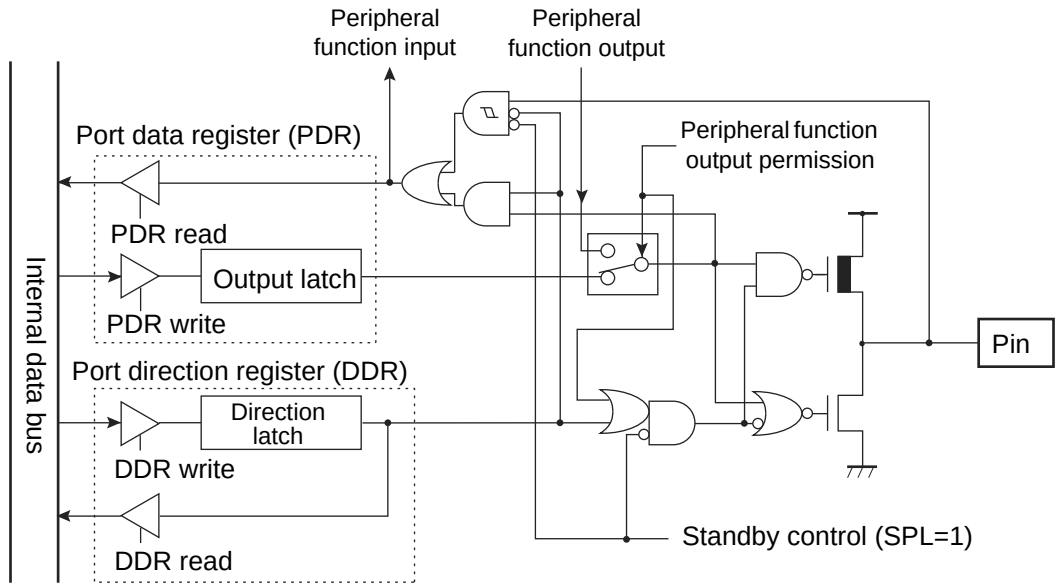
■ Port 2 registers include port 2 data register (PDR2) and port 2 direction register (DDR2).

■ The bits configuring the register correspond to port 2 pins on a one-to-one basis.

Relation between Port 2 Registers and Pins

Port Name	Bits of Register and Corresponding Pins									
Port 2	PDR2,DDR2	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	Corresponding pins	P27	P26	P25	P24	P23	P22	P21	P20

Port 4 Pins Block Diagram



Standby control: Control among Stop mode (SPL=1), Time-base timer mode (SPL=1), and watch mode (SPL=1).

Port 4 Registers

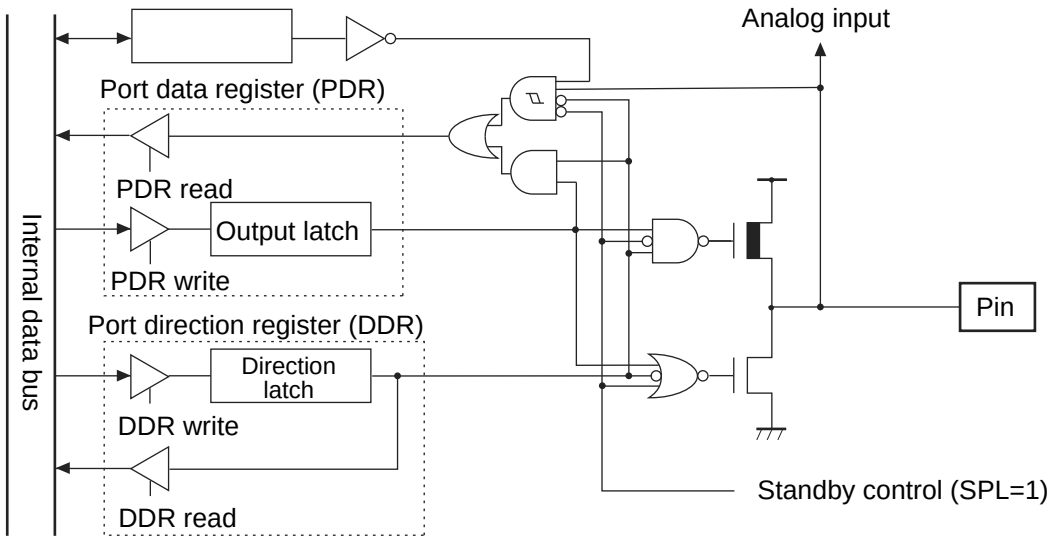
■ Port 4 registers include port 4 data register (PDR4) and port 4 direction register (DDR4).

■ The bits configuring the register correspond to port 4 pins on a one-to-one basis.

Relation between Port 4 Registers and Pins

Port Name	Bits of Register and Corresponding Pins									
Port 4	PDR4, DDR4	–	–	–	bit4	bit3	bit2	bit1	bit0
	Corresponding pins	–	–	–	P44	P43	P42	P41	P40

Port 5 Pins Block Diagram



Standby control: Control among Stop mode (SPL=1), Time-base timer mode (SPL=1), and watch mode (SPL=1).

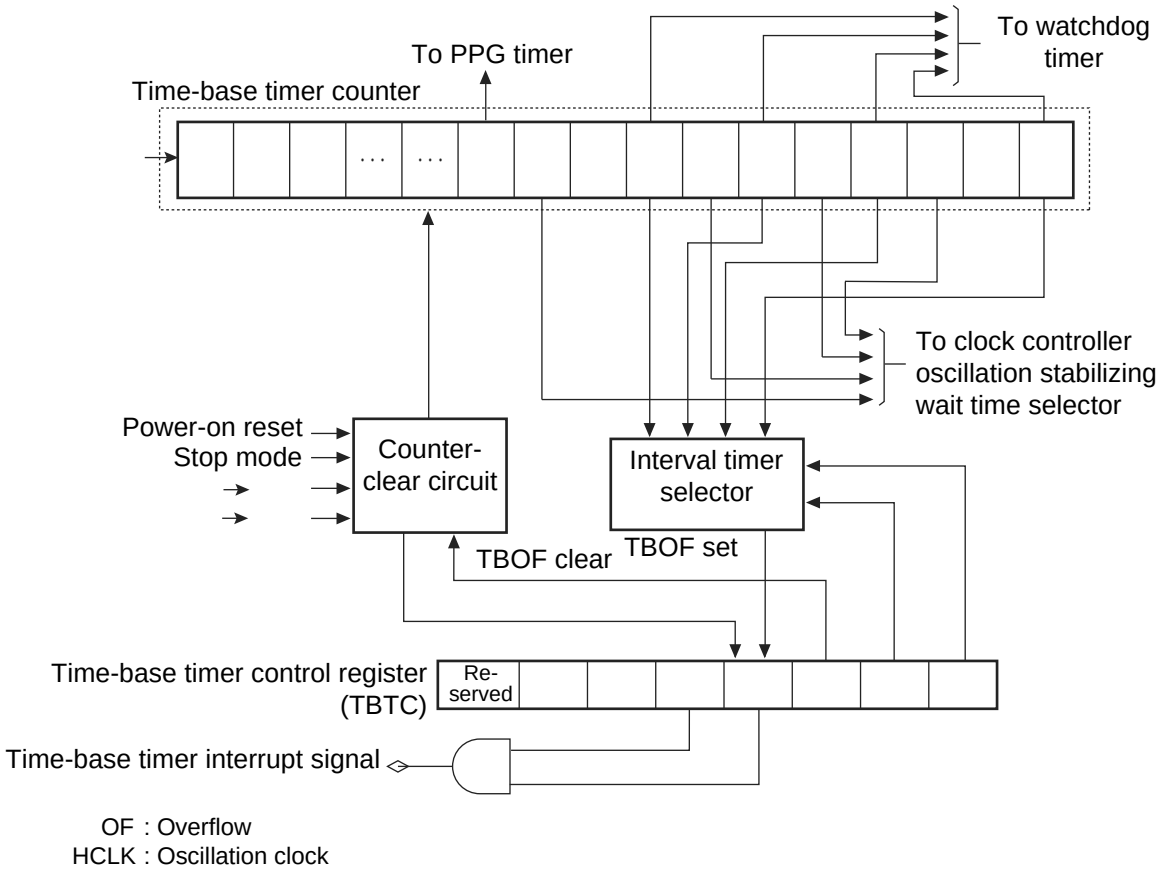
Port 5 Registers

- Port 5 registers include port 5 data register (PDR5), port 5 direction register (DDR5), and analog input permission register (ADER).
- Analog input permission register (ADER) allows or disallows input of analog signal to the analog input pin.
- The bits configuring the register correspond to port 5 pins on a one-to-one basis.

Relation between Port 5 Registers and Pins

Port Name	Bits of Register and Corresponding Pins								
Port 5	PDR5, DDR5	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	ADER	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
	Corresponding pins	P57	P56	P55	P54	P53	P52	P51	P50

Time-base Timer Block Diagram



OF : Overflow
HCLK : Oscillation clock

*1: Switch machine clock from main clock to PLL clock.

*2: Switch machine clock from sub clock to main clock.

Actual interrupt request number of time-base timer is as follows:

Interrupt request number: #16 (10_H)

12.3 Watchdog Timer

The watchdog timer is a 2-bit counter that uses time-base timer or watch timer as count clock. If the counter is not cleared within an interval time, CPU is reset.

Watchdog Timer Functions

- The watchdog timer is a timer counter that prevents runaway of a program. Once a watchdog timer is activated, the counter of watchdog timer must always be cleared within a specified time of interval. If specified interval time elapses without clearing the counter of a watchdog timer, CPU resetting occurs. This is the function of a watchdog timer.
- The interval time of a watchdog timer is determined by a clock cycle, which is input as a count clock. Watchdog resetting occurs between a minimum time and a maximum time specified.
- The output target of a clock source is specified by the watchdog clock selection bit (WTC: WDCS) in the watch timer control register.
- Interval time of a watchdog timer is specified by the time-base timer output selection bit / watch timer output selection bit (WDTC: WT1, WT0) in the watchdog timer control register.

Interval Timer of Watchdog Timer

Min	Max	Clock Cycle	Min	Max	Clock Cycle
Approx. 3.58 ms	Approx. 4.61 ms	$(2^{14}\pm2^{11})$ /HCLK	Approx. 0.457 s	Approx. 0.576 s	$(2^{12}\pm2^{9})$ /SCLK
Approx. 14.33 ms	Approx. 18.3 ms	$(2^{16}\pm2^{13})$ /HCLK	Approx. 3.584 s	Approx. 4.608 s	$(2^{15}\pm2^{12})$ /SCLK
Approx. 57.23 ms	Approx. 73.73 ms	$(2^{18}\pm2^{15})$ /HCLK	Approx. 7.168 s	Approx. 9.216 s	$(2^{16}\pm2^{13})$ /SCLK
Approx. 458.75 ms	Approx. 589.82 ms	$(2^{21}\pm2^{18})$ /HCLK	Approx. 14.336 s	Approx. 18.432 s	$(2^{17}\pm2^{14})$ /SCLK

HCLK: Oscillation clock (4 MHz), CSCLK: Sub clock (8.192 kHz)

Notes:

- If the time-base timer is cleared when watchdog timer count clock is used as time base timer output (carry-over signal), watchdog reset time may become longer.
- When using the sub clock as machine clock, be sure to specify watchdog timer clock source selection bit (WDCS) in watch timer control register (WTC) at “0,” selecting output of watch timer.

12.5 16-bit Reload Timer

The 16-bit reload timer has the following functions:

- Count clock is selectable among 3 internal clocks and external event clock.
- Activation trigger is selectable between software trigger and external trigger.
- Generation of CPU interrupt is allowed upon occurrence of underflow on 16-bit timer register. Available as an interval timer using the interrupt function.
- When underflow of 16-bit timer register (TMR) occurs, one of two reload modes is selectable between one-shot mode that halts counting operation of TMR, and reload mode that reloads 16-bit reload register value to TMR, continuing TMR counting operation.
- The 16-bit reload timer is ready for expanded intelligent I/O service (EI^2OS).
- MB90385 series device has 2 channels of built-in 16-bit reload timer.

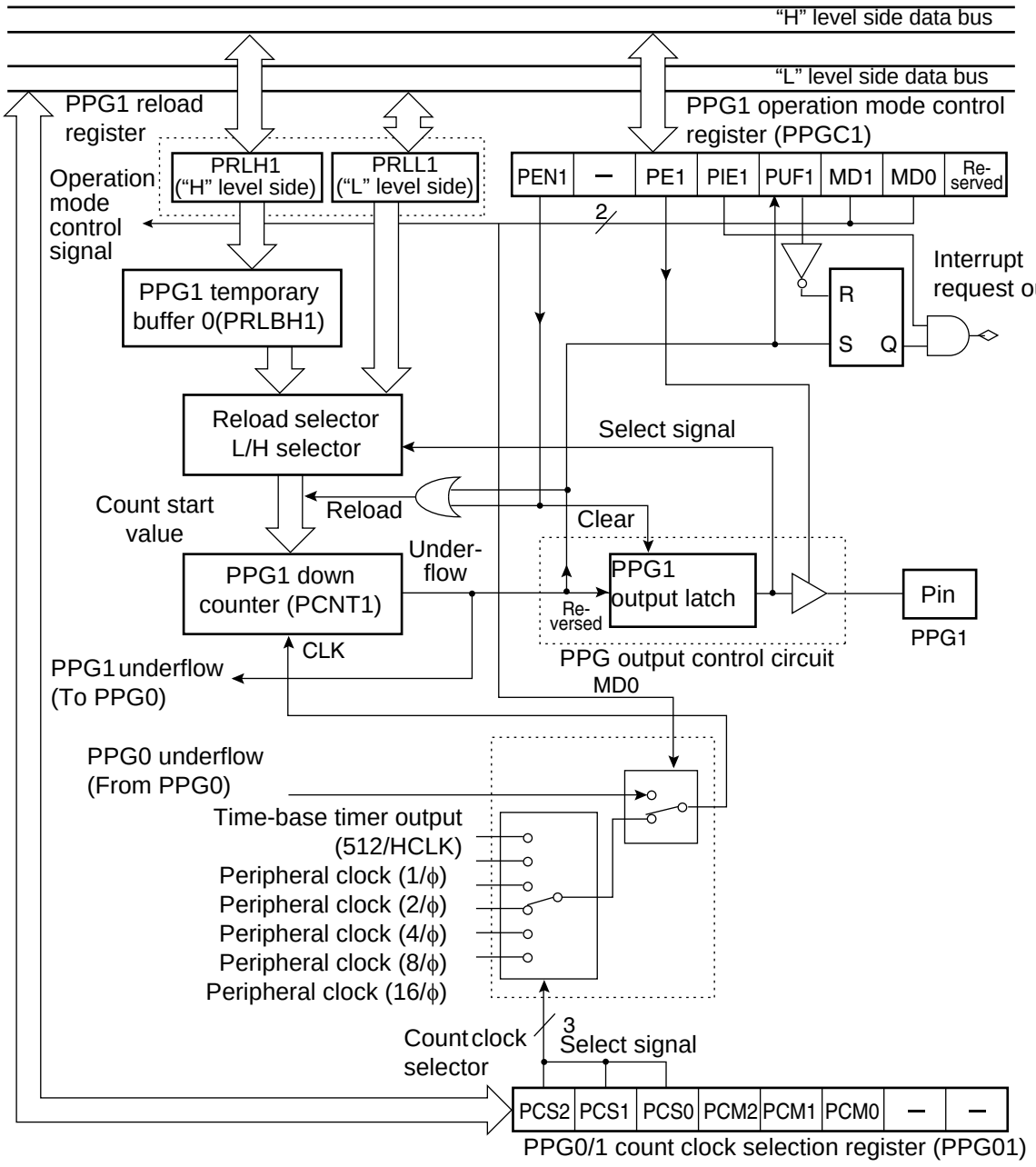
Operation Mode of 16-bit Reload Timer

Count Clock	Activation Trigger	Operation upon Underflow
Internal clock mode	Software trigger, external trigger	One-shot mode, reload mode
Event count mode	Software trigger	One-shot mode, reload mode

Internal Clock Mode

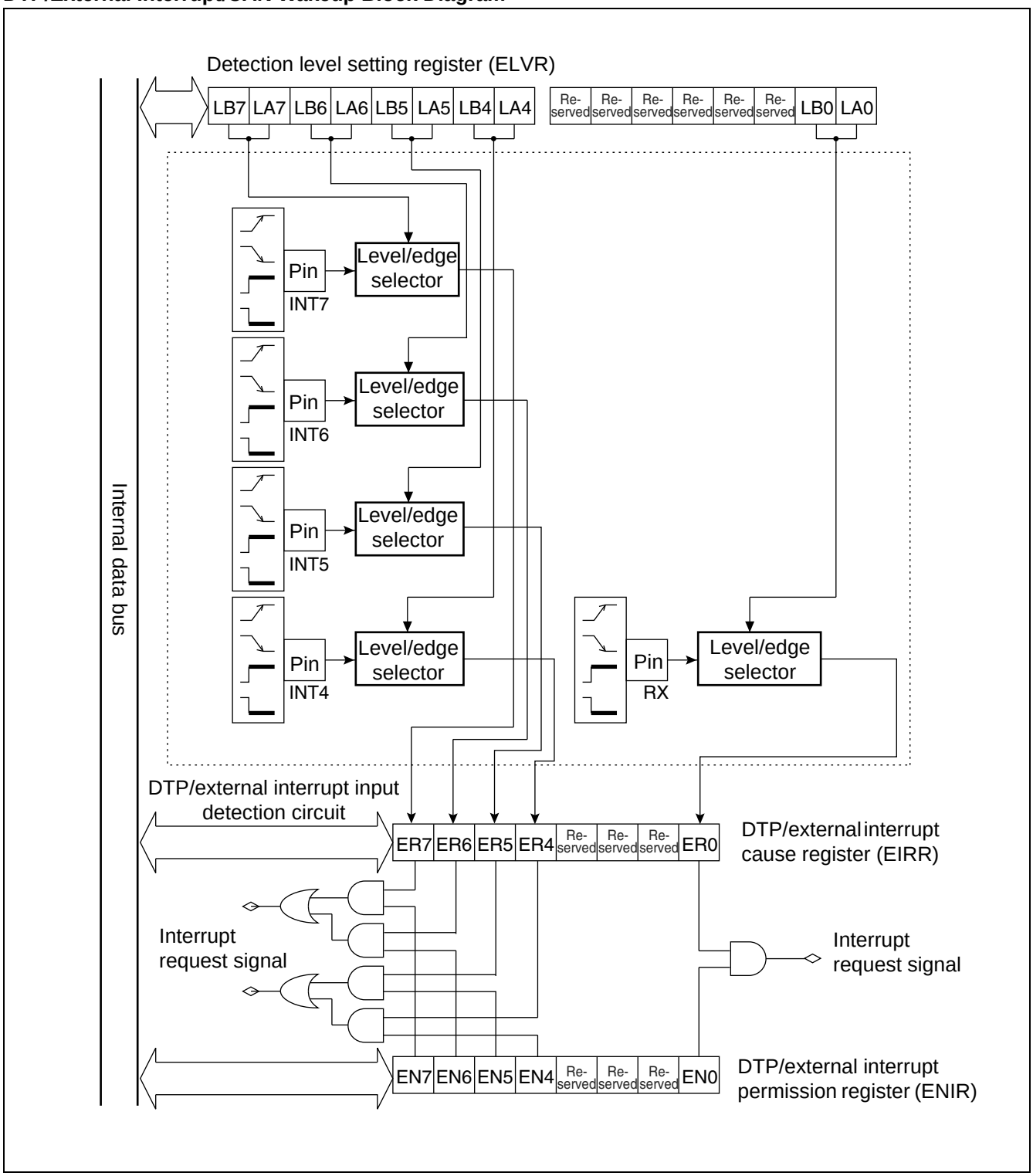
- The 16-bit reload timer is set to internal clock mode, by setting count clock selection bit (TMCSR: CSL1, CSL0) to “00_B”, “01_B”, “10_B”.
- In the internal clock mode, the counter decrements in synchronization with the internal clock.
- Three types of count clock cycles are selectable by count clock selection bit (TMCSR: CSL1, CSL0) in timer control status register.
- Edge detection of software trigger or external trigger is specified as an activation trigger.

8/16-bit PPG Timer 1 Block Diagram

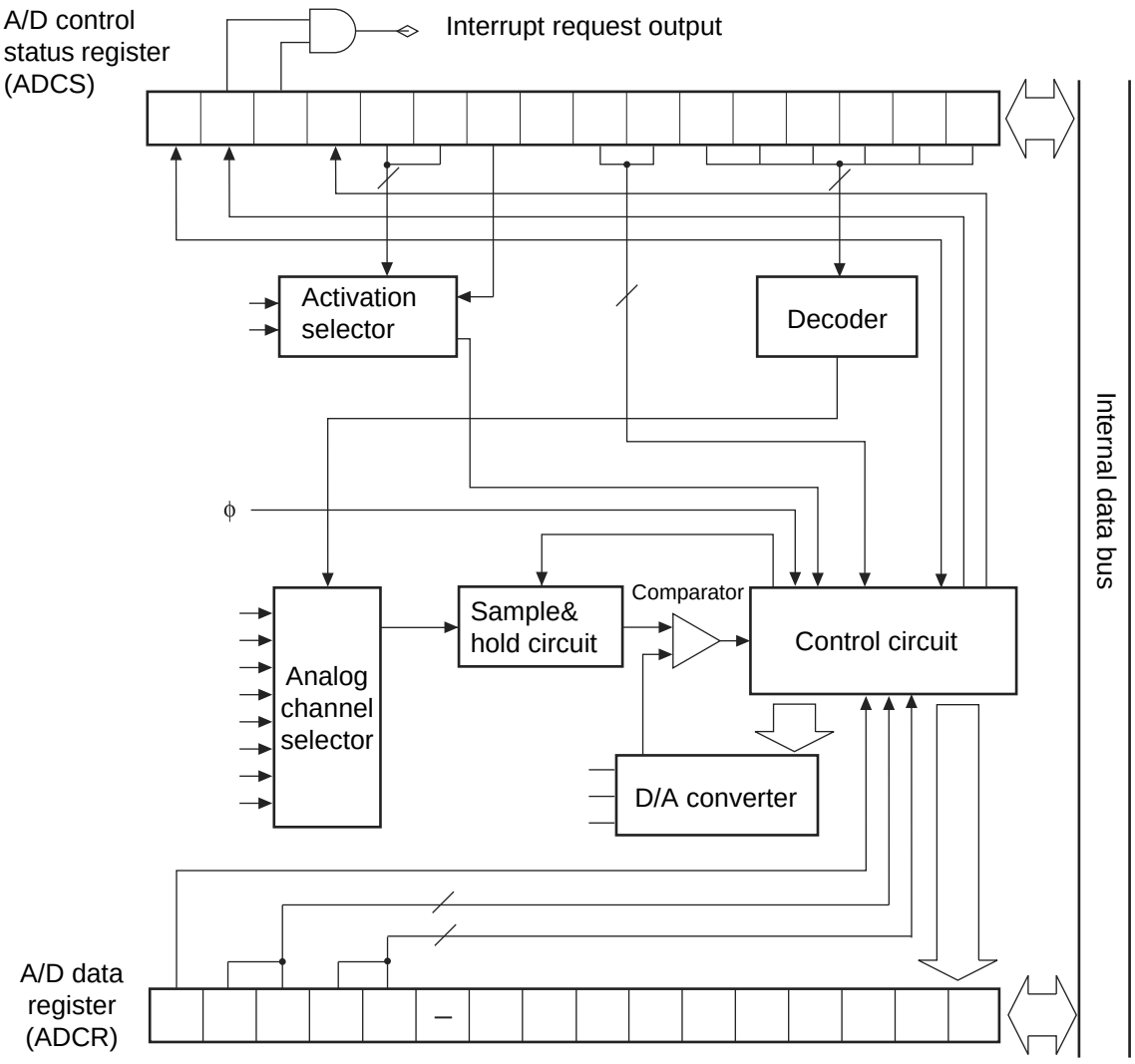


– : Undefined
Reserved: Reserved bit
HCLK : Oscillation clock frequency
ϕ : Machine clock frequency
* : Interrupt output of 8/16-bit PPG timer 1 is incorporated into one by the OR circuit against interrupt output of 8/16-bit PPG timer 0.

DTP/External Interrupt/CAN Wakeup Block Diagram



8/10-bit A/D Converter Block Diagram



TO : Internal timer output
– : Not defined
Reserved: Be sure to set to “0”
ϕ : Machine clock

12.11 UART Outline

UART is a general-purpose serial data communication interface for synchronous and asynchronous communication using external devices.

- Provided with bi-directional communication function for both clock-synchronous and clock-asynchronous modes.
- Provided with master/slave communication function (multi-processor mode). (Only master side is available.)
- Interrupt request is generated upon completion of reception, completion of transmission and detection of reception error.
- Ready for expanded intelligent service, EI^{2}OS.

Table 12-3. UART Functions

	Description
Data buffer	Full-duplex double buffer
Transmission mode	Clock synchronous (No start/stop bit, no parity bit) Clock asynchronous (start-stop synchronous)
Baud rate	Built-in special-purpose baud-rate generator. Setting is selectable among 8 values. Input of external values is allowed. Use of clock from external timer (16-bit reload timer 0) is allowed.
Data length	7 bits (only asynchronous normal mode) 8 bits
Signaling system	Non Return to Zero (NRZ) system
Reception error detection	Framing error Overrun error Parity error (not detectable in operation mode 1 (multi-processor mode))
Interrupt request	Receive interrupt (reception completed, reception error detected) Transmission interrupt (transmission completed) Ready for expanded intelligent I/O service (EI^{2}OS) in both transmission and reception
Master/slave communication function (asynchronous, multi-processor mode)	Communication between 1 (master) and n (slaves) are available (usable as master only).

Note: Start/stop bit is not added upon clock-synchronous transmission. Data only is transmitted.

Table 12-4. UART Operation Modes

Operation Mode		Data Length		Synchronization	Stop Bit Length
		With Parity	Without Parity		
0	Asynchronous mode (normal mode)	7-bit or 8-bit		Asynchronous	1- bit or 2-bit *2
1	Multi processor mode	8+1*1	–	Asynchronous	
2	Synchronous mode	8	–	Synchronous	No

–: Disallowed

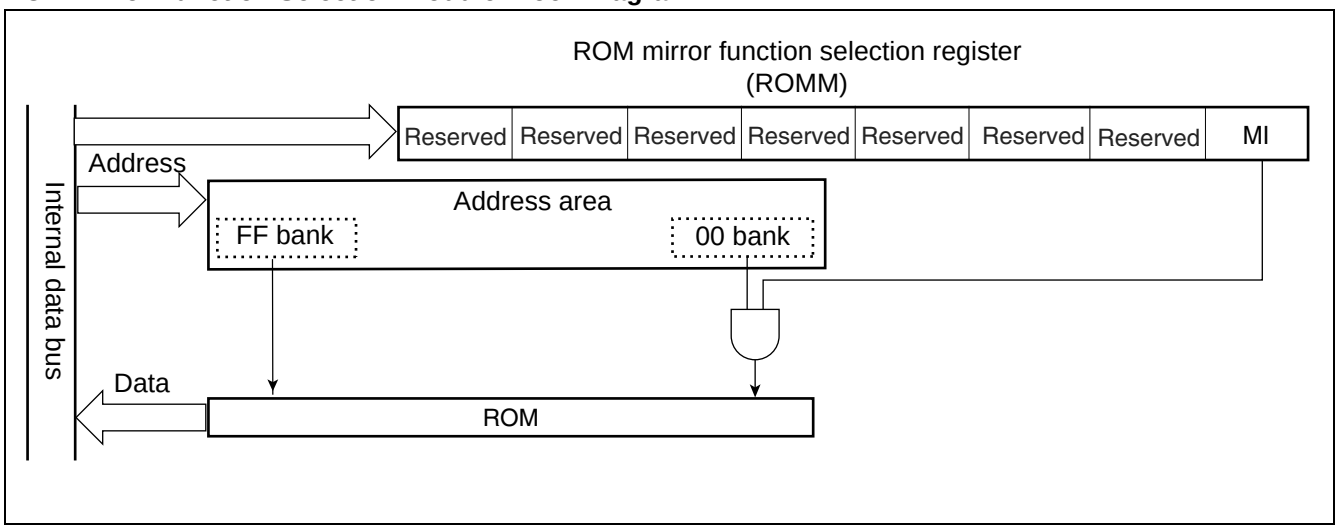
1: “+1” is an address/data selection bit used for communication control (bit 11 of SCR1 register: A/D).

2: Only 1 bit is detected as a stop bit on data reception.

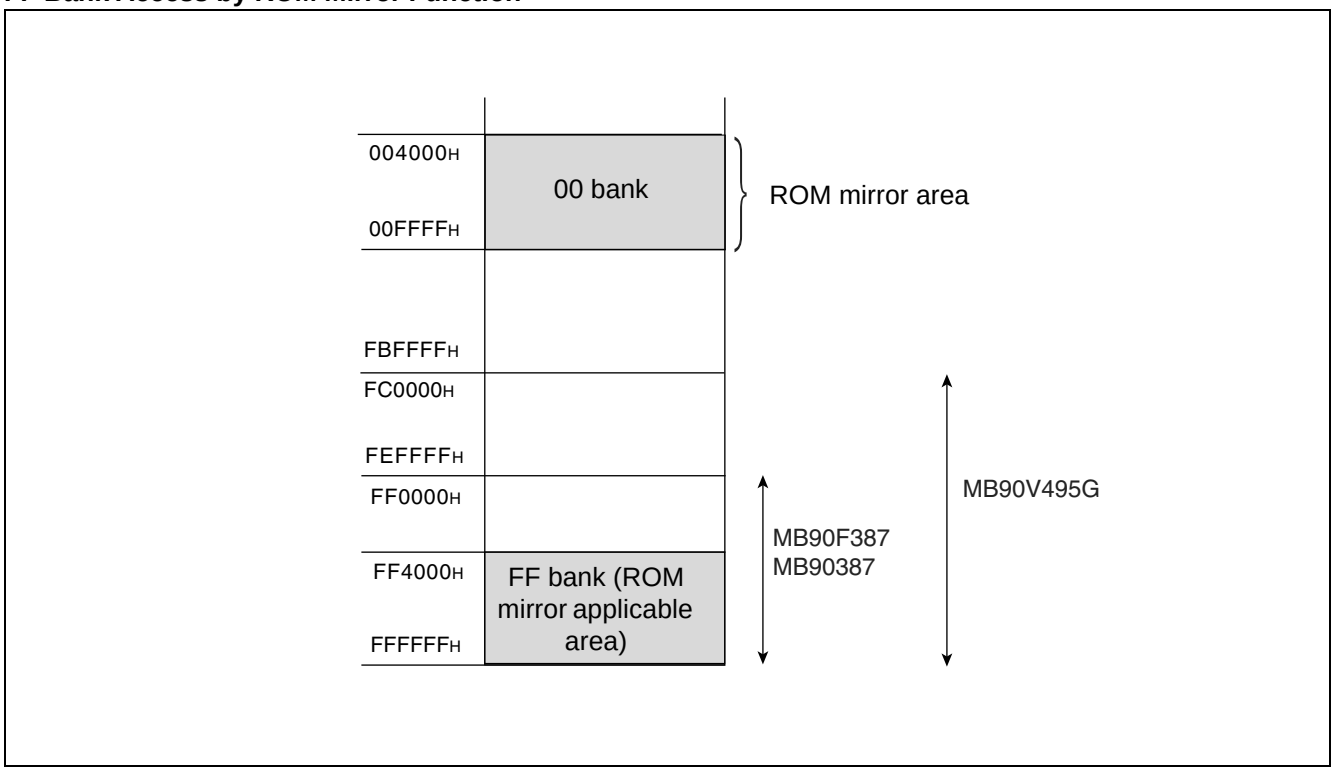
12.14 ROM Mirror Function Selection Module Outline

The ROM mirror function selection module sets the data in ROM assigned to FF bank so that the data is read by access to 00 bank.

ROM Mirror Function Selection Module Block Diagram



FF Bank Access by ROM Mirror Function



13.4.4 UART Timing

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK1	Internal shift clock mode output pin is: CL = 80 pF+1TTL.	4 t_{CP} *	–	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK1, SOT1		−80	+80	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK1, SIN1		100	–	ns	
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK1, SIN1		60	–	ns	
Serial clock “H” pulse width	t_{SHSL}	SCK1	External shift clock mode output pin is: CL = 80 pF+1TTL.	2 t_{CP} *	–	ns	
Serial clock “L” pulse width	t_{SLSH}	SCK1		2 t_{CP} *	–	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK1, SOT1		–	150	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK1, SIN1		60	–	ns	
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK1, SIN1		60	–	ns	

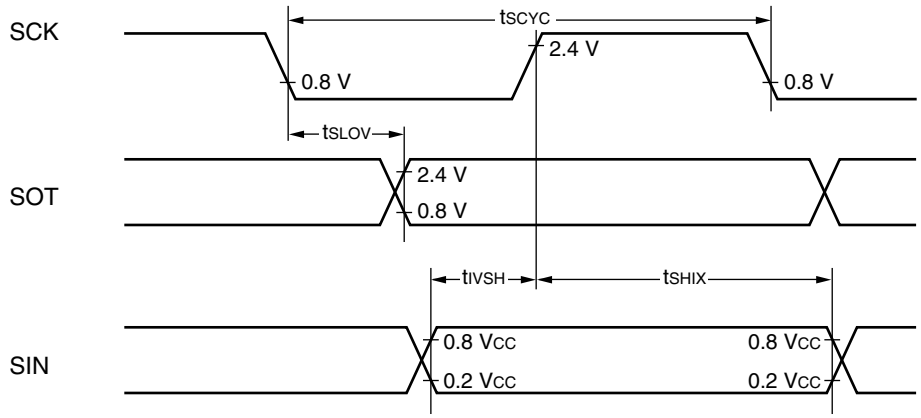
*: Refer to Clock Timing ratings for t_{CP} (internal operation clock cycle time).

Notes:

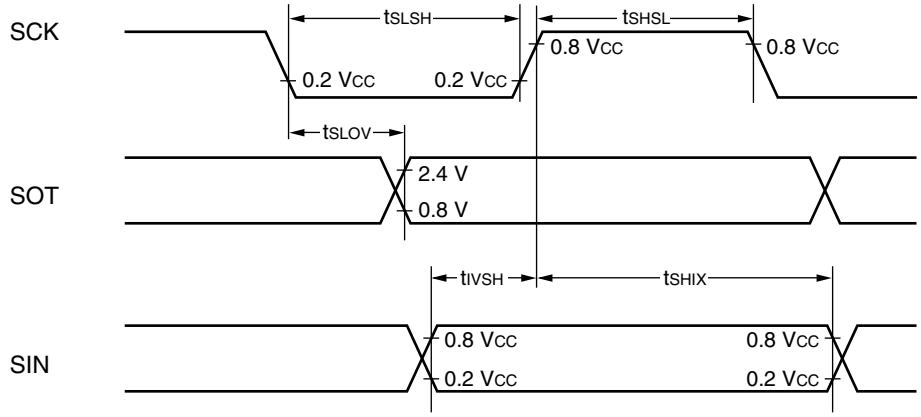
■ AC Characteristics in CLK synchronous mode.

■ C_L is a load capacitance value on pins for testing.

• Internal shift clock mode



• External shift clock mode



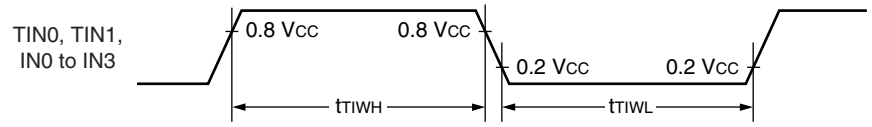
13.4.5 Timer Input Timing

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}	TIN0, TIN1	–	4 t_{CP} *	–	ns	
	t_{TIWL}	IN0 to IN3					

*: Refer to Clock Timing ratings for t_{CP} (internal operation clock cycle time).

• Timer input timing



13.4.6 Trigger Input Timing

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH} t_{TRGL}	INT4 to INT7, ADTG	–	5 t_{CP} *	–	ns	

*: Refer to Clock Timing ratings for t_{CP} (internal operation clock cycle time).

• Trigger input timing