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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, SCI, UART/USART
Peripherals	POR, WDT
Number of I/O	34
Program Memory Size	64KB (64K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90387pmt-g-190

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

DTP/External Interrupt: 4 channels, CAN wakeup: 1channel

Module for activation of expanded intelligent I/O service (EI²OS), and generation of external interrupt.

Delay Interrupt Generator Module

Generates interrupt request for task switching.

8/10-bit A/D Converter: 8 channels

- Resolution is selectable between 8-bit and 10-bit.
- Activation by external trigger input is allowed.
- Conversion time: 6.125 μs (at 16 MHz machine clock, including sampling time)

Program Patch Function

■ Address matching detection for 2 address pointers.

5. Pin Description

Pin No.	Pin Name	Circuit Type	Function	
1	AVcc	-	Vcc power input pin for A/D converter.	
2	AVR	-	Power (Vref+) input pin for A/D converter. Use as input for Vcc or lower.	
3 to 10	P50 to P57	E	General-purpose input/output ports.	
	AN0 to AN7		Functions as analog input pins for A/D converter. Valid when analog input setting is "enabled."	
11	P37	D	General-purpose input/output port.	
	ADTG		Function as an external trigger input pin for A/D converter. Use the pin by setting as input port.	
12	P20	D	General-purpose input/output port.	
	TIN0		Function as an event input pin for reload timer 0. Use the pin by setting as input port.	
13	P21	D	General-purpose input/output port.	
	TOT0		Function as an event output pin for reload timer 0. Valid only when output setting is "enabled."	
14	P22	D	General-purpose input/output port.	
	TIN1		Function as an event input pin for reload timer 1. Use the pin by setting as input port.	
15	P23	D	General-purpose input/output port.	
	TOT1		Function as an event output pin for reload timer 1. Valid only when output setting is "enabled."	
16 to 19	P24 to P27	D	General-purpose input/output ports.	
	INT4 to INT7		Functions as external interrupt input pins. Use the pins by setting as input port.	
20	MD2	F	Input pin for specifying operation mode. Connect directly to Vss.	
21	MD1	С	Input pin for specifying operation mode. Connect directly to Vcc.	
22	MD0	С	Input pin for specifying operation mode. Connect directly to Vcc.	
23	RST	В	External reset input pin.	
24	Vcc	-	Power source (5 V) input pin.	
25	Vss	-	Power source (0 V) input pin.	
26	С	_	Capacitor pin for stabilizing power source. Connect a ceramic capacitor of approximately 0.1 $\mu\text{F}.$	
27	X0	A	Pin for high-rate oscillation.	
28	X1	A	Pin for high-rate oscillation.	
29 to 32	P10 to P13	D	General-purpose input/output ports.	
	IN0 to IN3		Functions as trigger input pins of input capture ch.0 to ch.3. Use the pins by setting as input ports.	
33 to 36	P14 to P17	G	General-purpose input/output ports. High-current output ports.	
	PPG0 to PPG3		Functions as output pins of PPG timers 01 and 23. Valid when output setting is "enabled."	
37	P40	D	General-purpose input/output port.	
	SIN1		Serial data input pin for UART. Use the pin by setting as input port.	
38	P41	D	General-purpose input/output port.	
	SCK1		Serial clock input pin for UART. Valid only when serial clock input/output setting on UART is "enabled."	

Notes When Using No Sub Clock

■ If an oscillator is not connected to X0A and X1A pin, apply pull-down resistor to X0A pin and leave X1A pin open.

About Power Supply Pins

- If two or more Vcc and Vss pins exist, the pins that should be at the same potential are connected to each other inside the device. For reducing unwanted emissions and preventing malfunction of strobe signals caused by increase of ground level, however, be sure to connect the Vcc and Vss pins to the power source and the ground externally.
- Pay attention to connect a power supply to Vcc and Vss of MB90385 series device in a lowest-possible impedance.
- Near pins of MB90385 series device, connecting a bypass capacitor is recommended at 0.1 µF across Vcc pin and Vss pin.

Crystal Oscillator Circuit

- Noises around X0 and X1 pins cause malfunctions on a MB90385 series device. Design a print circuit so that X0 and X1 pins, an crystal oscillator (or a ceramic oscillator), and bypass capacitor to the ground become as close as possible to each other. Furthermore, avoid wires to X0 and X1 pins crossing each other as much as possible.
- Print circuit designing that surrounds X0 and X1 pins with grounding wires, which ensures stable operation, is strongly recommended.

Caution on Operations during PLL Clock Mode

If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

Sequence of Turning on Power of A/D Converter and Applying Analog Input

- Be sure to turn on digital power (Vcc) before applying signals to the A/D converter and applying analog input signals (AN0 to AN7 pins).
- Be sure to turn off the power of A/D converter and analog input before turning off the digital power source.
- Be sure not to apply AVR exceeding AVcc when turning on and off. (No problems occur if analog and digital power is turned on and off simultaneously.)

Handling Pins When A/D Converter is Not Used

■ If the A/D converter is not used, connect the pins under the following conditions: "AVcc=AVR=Vcc," and "AVss=Vss"

Note on Turning on Power

For preventing malfunctions on built-in step-down circuit, maintain a minimum of 50 μs of voltage rising time (between 0.2 V and 2.7V) when turning on the power.

Stabilization of Supply Voltage

■ A sudden change in the supply voltage may cause the device to malfunction even within the specified Vcc supply voltage operating range. Therefore, the Vcc supply voltage should be stabilized.

For reference, the supply voltage should be controlled so that Vcc ripple variations (peak-to-peak values) at commercial frequencies (50 Hz / 60 Hz) fall below 10% of the standard Vcc supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

10. I/O Map

Address	Register Abbreviation	Register	Read/ Write	Resource	Initial Value
00000н		(Reserve	ed area) *		I
000001н	PDR1	Port 1 data register	R/W	Port 1	XXXXXXXXB
000002н	PDR2	Port 2 data register	R/W	Port 2	XXXXXXXXB
00003н	PDR3	Port 3 data register	R/W	Port 3	XXXXXXXXB
000004н	PDR4	Port 4 data register	R/W	Port 4	XXXXXXXXB
000005н	PDR5	Port 5 data register	R/W	Port 5	XXXXXXXXB
000006н to 000010н		(Reserve	ed area) *		
000011н	DDR1	Port 1 direction data register	R/W	Port 1	0000000в
000012н	DDR2	Port 2 direction data register	R/W	Port 2	0000000в
000013н	DDR3	Port 3 direction data register	R/W	Port 3	000Х000в
000014н	DDR4	Port 4 direction data register	R/W	Port 4	ХХХ00000в
000015н	DDR5	Port 5 direction data register	R/W	Port 5	0000000в
000016н to 00001Ан		(Reserve	ed area) *		I
00001Bн	ADER	Analog input permission register	R/W	8/10-bit A/D converter	11111111в
00001Cнto 000025н		(Reserve	ed area) *		
000026н	SMR1	Serial mode register 1	R/W	UART1	0000000в
000027н	SCR1	Serial control register 1	R/W, W		00000100в
000028н	SIDR1/ SODR1	Serial input data register 1/ Serial output data register 1	R, W		XXXXXXXXB
000029н	SSR1	Serial status data register 1	R, R/W		00001000в
00002Ан		(Reserve	ed area) *		
00002Вн	CDCR1	Communication prescaler control register 1	R/W	UART1	0ХХХ0000в
00002Cнto 00002Fн		(Reserve	ed area) *		
000030н	ENIR	DTP/External interrupt permission register	R/W	DTP/External interrupt	0000000в
000031н	EIRR	DTP/External interrupt permission register	R/W		XXXXXXXXB
000032н	ELVR	Detection level setting register	R/W		0000000в
000033н			R/W		0000000в
000034н	ADCS	A/D control status register	R/W	8/10-bit A/D	0000000в
000035н	1		R/W, W	converter	0000000в
000036н	ADCR	A/D data register	W, R	1	XXXXXXXXB
000037н]		R]	00101XXXв

Interrupt Source	El ² OS	l	nterrup	t Vector	Interrupt C	Priority*3	
interrupt Source	Readiness	Number		Address	ICR	Address	FIOLITY
UART1 reception completed	0	#37	25н	FFFF68 _H	ICR13	0000BDH*1	High
UART1 transmission completed	Δ	#38	26н	FFFF64H			\uparrow
Reserved	×	#39	27н	FFFF60H	ICR14	0000BEн*1	
Reserved	×	#40	28н	FFFF5CH			
Flash memory	×	#41	29н	FFFF58н	ICR15	0000BFн*1	\downarrow
Delay interrupt generation module	×	#42	2Ан	FFFF54н			Low

○ : Available

× : Unavailable

© : Available El²OS function is provided.

 Δ : Available when a cause of interrupt sharing a same ICR is not used.

*1:

□ Peripheral functions sharing an ICR register have the same interrupt level.

□ If peripheral functions share an ICR register, only one function is available when using expanded intelligent I/O service.

If peripheral functions share an ICR register, a function using expanded intelligent I/O service does not allow interrupt by another function.

*2: Input capture 1 corresponds to EI2OS, however, PPG does not. When using EI2OS by input capture 1, interrupt should be disabled for PPG.

*3:Priority when two or more interrupts of a same level occur simultaneously.

12. Peripheral Resources

12.1 I/O Ports

The I/O ports are used as general-purpose input/output ports (parallel I/O ports). The MB60385 series model is provided with 5 ports (34 inputs). The ports function as input/output pins for peripheral functions also.

I/O Port Functions

An I/O port, using port data resister (PDR), outputs the output data to I/O pin and input a signal input to I/O port. The port direction register (DDR) specifies direction of input/output of I/O pins on a bit-by-bit basis.

The following summarizes functions of the ports and sharing peripheral functions:

- Port 1: General-purpose input/output port, used also for PPG timer output and input capture inputs.
- Port 2: General-purpose input/output port, used also for reload timer input/output and external interrupt input.
- Port 3: General-purpose input/output port, used also for A/D converter activation trigger pin.
- Port 4: General-purpose input/output port, used also for UART input/output and CAN controller send/receive pin.
- Port 5: General-purpose input/output port, used also analog input pin.





Port 3 Registers

- Port 3 registers include port 3 data register (PDR3) and port 3 direction register (DDR3).
- The bits configuring the register correspond to port 3 pins on a one-to-one basis.

Relation between Port 3 Registers and Pins

Port Name	Bits of Register and Corresponding Pins								
Port 3	PDR3, DDR3	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	Corresponding pins	P37	P36*	P35*	_	P33	P32	P31	P30

*: P35 and P36 do not exist on MB90387and MB90F387.

Time-base Timer Block Diagram



Actual interrupt request number of time-base timer is as follows: Interrupt request number: #16 (10_H)

12.3 Watchdog Timer

The watchdog timer is a 2-bit counter that uses time-base timer or watch timer as count clock. If the counter is not cleared within an interval time, CPU is reset.

Watchdog Timer Functions

- The watchdog timer is a timer counter that prevents runaway of a program. Once a watchdog timer is activated, the counter of watchdog timer must always be cleared within a specified time of interval. If specified interval time elapses without clearing the counter of a watchdog timer, CPU resetting occurs. This is the function of a watchdog timer.
- The interval time of a watchdog timer is determined by a clock cycle, which is input as a count clock. Watchdog resetting occurs between a minimum time and a maximum time specified.
- The output target of a clock source is specified by the watchdog clock selection bit (WTC: WDCS) in the watch timer control register.
- Interval time of a watchdog timer is specified by the time-base timer output selection bit / watch timer output selection bit (WDTC: WT1, WT0) in the watchdog timer control register.

Min	Мах	Clock Cycle	Min	Max	Clock Cycle
Approx. 3.58 ms	Approx. 4.61 ms	(2 ¹⁴ ±2 ¹¹) /HCLK	Approx. 0.457 s	Approx. 0.576 s	(2 ¹² ±2 ⁹) /SCLK
Approx. 14.33 ms	Approx. 18.3 ms	(2 ¹⁶ ±2 ¹³) /HCLK	Approx. 3.584 s	Approx. 4.608 s	(2 ¹⁵ ±2 ¹²) /SCLK
Approx. 57.23 ms	Approx. 73.73 ms	(2 ¹⁸ ±2 ¹⁵) /HCLK	Approx. 7.168 s	Approx. 9.216 s	(2 ¹⁶ ±2 ¹³) /SCLK
Approx. 458.75 ms	Approx. 589.82 ms	(2 ²¹ ±2 ¹⁸) /HCLK	Approx. 14.336 s	Approx. 18.432 s	(2 ¹⁷ ±2 ¹⁴) /SCLK

Interval Timer of Watchdog Timer

HCLK: Oscillation clock (4 MHz), CSCLK: Sub clock (8.192 kHz)

Notes:

- If the time-base timer is cleared when watchdog timer count clock is used as time base timer output (carry-over signal), watchdog reset time may become longer.
- When using the sub clock as machine clock, be sure to specify watchdog timer clock source selection bit (WDCS) in watch timer control register (WTC) at "0," selecting output of watch timer.

12.5 16-bit Reload Timer

The 16-bit reload timer has the following functions:

- Count clock is selectable among 3 internal clocks and external event clock.
- Activation trigger is selectable between software trigger and external trigger.
- Generation of CPU interrupt is allowed upon occurrence of underflow on 16-bit timer register. Available as an interval timer using the interrupt function.
- When underflow of 16-bit timer register (TMR) occurs, one of two reload modes is selectable between one-shot mode that halts counting operation of TMR, and reload mode that reloads 16-bit reload register value to TMR, continuing TMR counting operation.
- The 16-bit reload timer is ready for expanded intelligent I/O service (El²OS).
- MB90385 series device has 2 channels of built-in 16-bit reload timer.

Operation Mode of 16-bit Reload Timer

Count Clock	Activation Trigger	Operation upon Underflow
Internal clock mode	Software trigger, external trigger	One-shot mode, reload mode
Event count mode	Software trigger	One-shot mode, reload mode

Internal Clock Mode

- The 16-bit reload timer is set to internal clock mode, by setting count clock selection bit (TMCSR: CSL1, CSL0) to "00_B", "01_B", "10_B".
- In the internal clock mode, the counter decrements in synchronization with the internal clock.
- Three types of count clock cycles are selectable by count clock selection bit (TMCSR: CSL1, CSL0) in timer control status register.
- Edge detection of software trigger or external trigger is specified as an activation trigger.

Watch Timer Block Diagram



Actual interrupt request number of watch timer is as follows: Interrupt request number: #28 (1C_H)

Watch Timer Counter

A 15-bit up counter that uses sub clock (SCLK) as a count clock.

Counter Clear Circuit

A circuit that clears the watch timer counter.

8/16-bit PPG Timer 1 Block Diagram



CAN Controller Block Diagram



13. Electrical Characteristics

13.1 Absolute Maximum Rating

Baramatar	Symbol	Rat	ing	Unit	Bomarka	
Falameter	Symbol	Min	Max	Unit	Remarks	
Power supply voltage*1	Vcc	Vss - 0.3	Vss + 6.0	V		
	AVcc	Vss - 0.3	Vss + 6.0	V	Vcc = AVcc*2	
	AVR	Vss - 0.3	Vss + 6.0	V	$AVcc \ge AVR^{*2}$	
Input voltage*1	Vı	Vss - 0.3	Vss + 6.0	V	*3	
Output voltage*1	Vo	Vss - 0.3	Vss + 6.0	V	*3	
Maximum clamp current		- 2.0	+ 2.0	mA	*7	
Total maximum clamp current	Σ Iclamp	-	20	mA	*7	
"L" level maximum output current	IOL1	-	15	mA	Normal output*4	
	lol2	-	40	mA	High-current output*4	
"L" level average output current	IOLAV1	-	4	mA	Normal output*5	
	IOLAV2	-	30	mA	High-current output*5	
"L" level maximum total output current	Σlol1	-	125	mA	Normal output	
	Σ Ι OL2	-	160	mA	High-current output	
"L" level average total output current	Σ IOLAV1	-	40	mA	Normal output*6	
	Σ Iolav2	-	40	mA	High-current output*6	
"H" level maximum output current	Іон1	-	-15	mA	Normal output*4	
	Іон2	-	-40	mA	High-current output*4	
"H" level average output current	IOHAV1	-	-4	mA	Normal output*5	
	IOHAV2	-	-30	mA	High-current output*5	
"H" level maximum total output current	Σloh1	-	-125	mA	Normal output	
	ΣІон2	-	-160	mA	High-current output	
"H" level average total output current	ΣΙομαν1	-	-40	mA	Normal output*6	
	ΣΙοήαν2	-	-40	mA	High-current output*6	
Power consumption	PD	-	245	mW		
Operating temperature	TA	-40	+105	°C		
Storage temperature	Tstg	-55	+150	°C		

*1: The parameter is based on $V_{SS} = AV_{SS} = 0.0 V.$

*2: AVcc and AVR should not exceed Vcc.

*3: VI and Vo should not exceed Vcc + 0.3 V. However if the maximum current to/from an input is limited by some means with external components, the IcLAMP rating supersedes the VI rating.

*4: A peak value of an applicable one pin is specified as a maximum output current.

- *5: An average current value of an applicable one pin within 100 ms is specified as an average output current. (Average value is found by multiplying operating current by operating rate.)
- *6: An average current value of all pins within 100 ms is specified as an average total output current. (Average value is found by multiplying operating current by operating rate.)

*7:

Applicable to pins: P10 to P17, P20 to P27, P30 to P33, P35*, P36*, P37, P40 to P44, P50 to P57
 *: P35 and P36 are MB90387S and MB90F387S only.

13.7 Notes on A/D Converter Section

Use the device with external circuits of the following output impedance for analog inputs:

Recommended output impedance of external circuits are: Approx. 3.9 k Ω or lower (4.5 V \leq AVcc \leq 5.5 V) (sampling period=2.00 μ s at 16 MHz machine clock), Approx. 11 k Ω or lower (4.0 V \leq AVcc < 4.5 V) (sampling period=8.0 μ s at 16 MHz machine clock).

If an external capacitor is used, in consideration of the effect by tap capacitance caused by external capacitors and on-chip capacitors, capacitance of the external one is recommended to be several thousand times as high as internal capacitor.

If output impedance of an external circuit is too high, a sampling period for an analog voltage may be insufficient.



About errors

As [AVR-AVss] become smaller, values of relative errors grow larger.

13.8 Flash Memory Program/Erase Characteristics

Paramotor	Conditions		Value		Unit	Pomarke
Falameter	Conditions	Min	Тур	Max	Onit	Rellidiks
Sector erase time	$\begin{array}{l} T_{\text{A}}=+~25~^{\circ}C\\ V_{\text{CC}}=5.0~V \end{array}$	-	1	15	S	Excludes 00H programming prior to erasure
Chip erase time		-	4	-	S	Excludes 00H programming prior to erasure
Word (16-bit width) programming time		-	16	3,600	μS	Except for the over head time of the system
Program/Erase cycle	_	10,000	-	-	cycle	
Flash Data Retention Time	Average T _A = + 85 °C	20	-	-	Year	*

*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C).

14. Example Characteristics

MB90F387



(Continued)



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17. Major Changes

Spansion Publication Number: DS07-13717-5E

Page	Section	Change Results
4	■ PRODUCT LINEUP	Changed the number of channel of 8/16 bit PPG timer. or one 16-bit channel \rightarrow or two 16-bit channels
13	■ BLOCK DIAGRAM	Changed the direction of arrow of TIN0, TIN1 signals of 16-bit reload timer. right arrow (output) \rightarrow left arrow (input)
67	 ELECTRIC CHARACTERISTICS 4. AC Characteristics (4) UART timing 	Changed the value of Serial clock. Serial clock "H" pulse width: 4tcp→2tcp Serial clock "L" pulse width: 4tcp→2tcp

NOTE: Please see "Document History" about later revised information.