## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

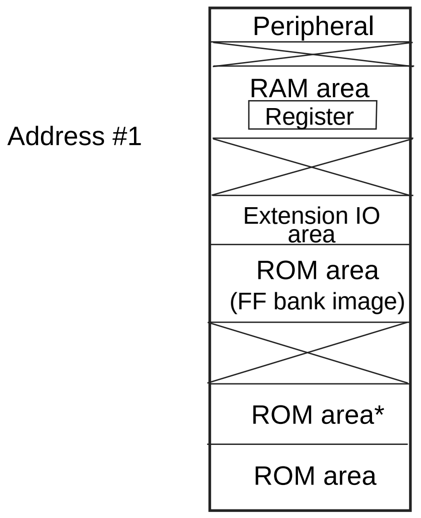
## Applications of "Embedded - Microcontrollers"

| **Details** | |
|---|---|
| Product Status | Active |
| Core Processor | F²MC-16LX |
| Core Size | 16-Bit |
| Speed | 16MHz |
| Connectivity | CANbus, SCI, UART/USART |
| Peripherals | POR, WDT |
| Number of I/O | 34 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | Mask ROM |
| EEPROM Size | - |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3.5V ~ 5.5V |
| Data Converters | A/D 8x8/10b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-LQFP |
| Supplier Device Package | 48-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/mb90387pmt-gs-157 |

## Contents

### 9.2 Memory Map

(with ROM mirroring function enabled)



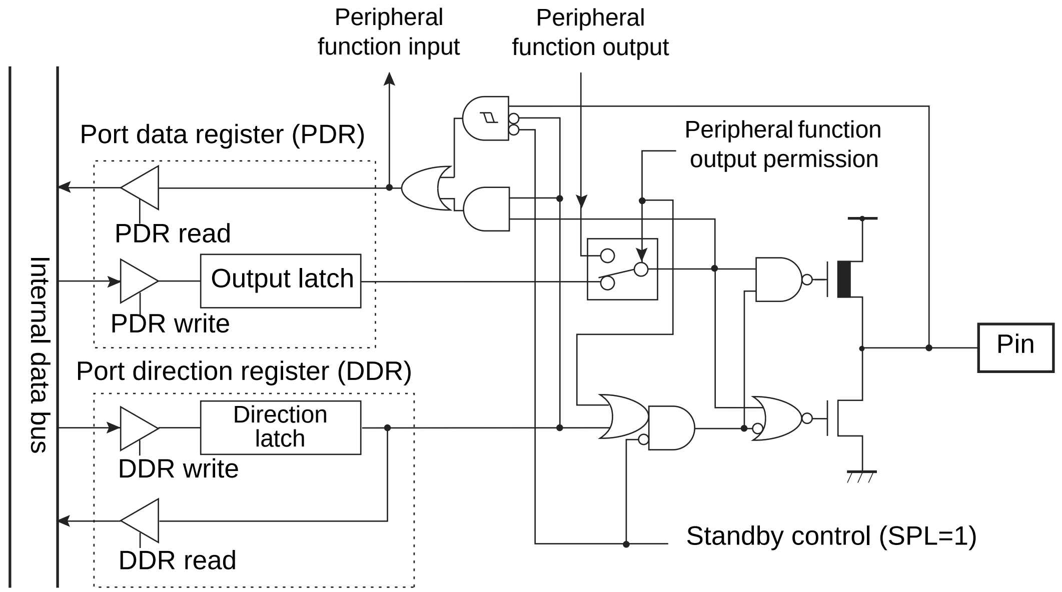
| Model | Address #1 |
|---|---|
| | 001900$_H$ |
| | 000900$_H$ |
| | 000900$_H$ |

☐ : Internal access memory
☒ : Access disallowed

*: On MB90387/S or MB90F387/S, to read “FE0000$_H$” to “FEFFFF$_H$” is to read out “FF0000$_H$” to “FFFFFF$_H$”.

Note: When internal ROM is operating, $F^2$MC-16LX allows viewing ROM data image on FF bank at upper-level of 00 bank. This function is called “mirroring ROM,” which allows effective use of C compiler small model.
$F^2$MC-16LX assigns the same low order 16-bit address to FF bank and 00 bank, which allows referencing table in ROM without specifying “far” using pointer.
For example, when accessing to “00C000$_H$”, ROM data at “FFC000$_H$” is accessed actually. However, because ROM area of FF bank exceeds 48 Kbytes, viewing all areas is not possible on 00 bank image. Because ROM data of “FF4000$_H$” to “FFFFFF$_H$” is viewed on “004000$_H$” to “00FFFF$_H$” image, store a ROM data table in area “FF4000$_H$” to “FFFFFF$_H$.”

### Port 2 Pins Block Diagram (general-purpose input/output port)



Standby control: Control among Stop mode (SPL=1), Time-base timer mode (SPL=1), and watch mode (SPL=1).

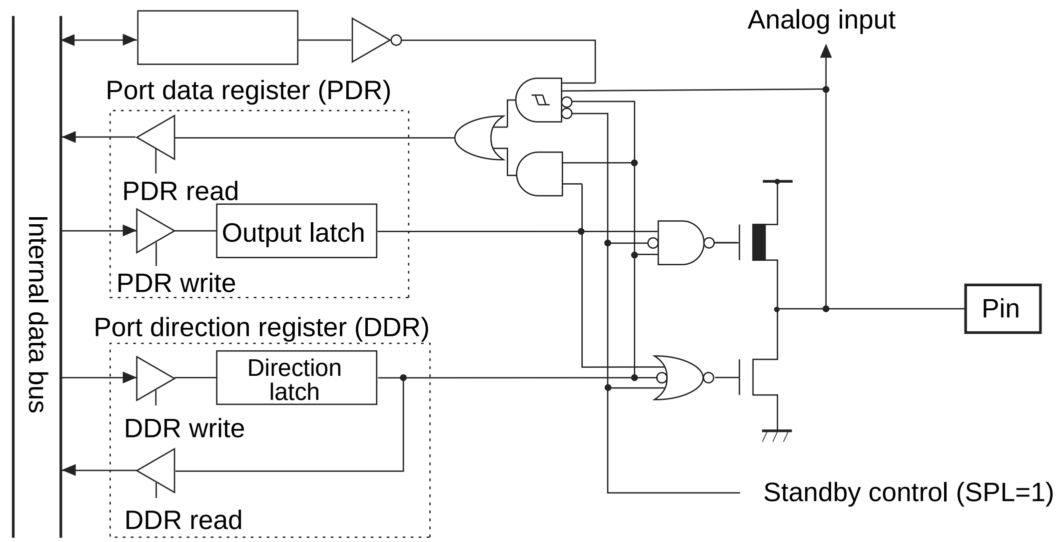
### Port 2 Registers

- Port 2 registers include port 2 data register (PDR2) and port 2 direction register (DDR2).
- The bits configuring the register correspond to port 2 pins on a one-to-one basis.

### Relation between Port 2 Registers and Pins

| Port Name | Bits of Register and Corresponding Pins | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Port 2 | PDR2,DDR2 | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| | Corresponding pins | P27 | P26 | P25 | P24 | P23 | P22 | P21 | P20 |

### Port 5 Pins Block Diagram



Standby control: Control among Stop mode (SPL=1), Time-base timer mode (SPL=1), and watch mode (SPL=1).

### Port 5 Registers

- ■ Port 5 registers include port 5 data register (PDR5), port 5 direction register (DDR5), and analog input permission register (ADER).
- ■ Analog input permission register (ADER) allows or disallows input of analog signal to the analog input pin.
- ■ The bits configuring the register correspond to port 5 pins on a one-to-one basis.

### Relation between Port 5 Registers and Pins

| Port Name | Bits of Register and Corresponding Pins | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Port 5 | PDR5, DDR5 | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| | ADER | ADE7 | ADE6 | ADE5 | ADE4 | ADE3 | ADE2 | ADE1 | ADE0 |
| | Corresponding pins | P57 | P56 | P55 | P54 | P53 | P52 | P51 | P50 |

## 12.5 16-bit Reload Timer

The 16-bit reload timer has the following functions:

- Count clock is selectable among 3 internal clocks and external event clock.
- Activation trigger is selectable between software trigger and external trigger.
- Generation of CPU interrupt is allowed upon occurrence of underflow on 16-bit timer register. Available as an interval timer using the interrupt function.
- When underflow of 16-bit timer register (TMR) occurs, one of two reload modes is selectable between one-shot mode that halts counting operation of TMR, and reload mode that reloads 16-bit reload register value to TMR, continuing TMR counting operation.
- The 16-bit reload timer is ready for expanded intelligent I/O service (EI$^2$OS).
- MB90385 series device has 2 channels of built-in 16-bit reload timer.

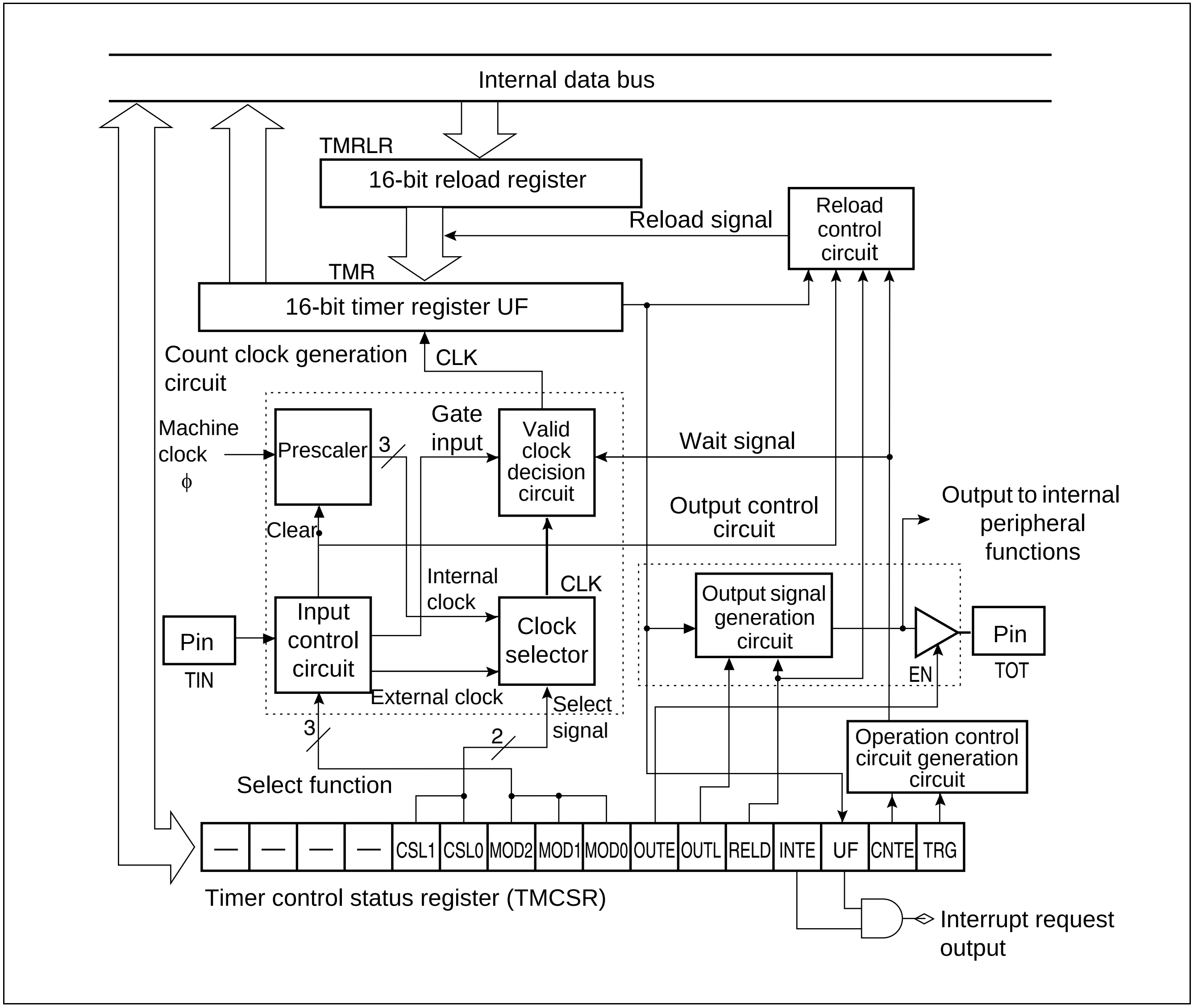
### Operation Mode of 16-bit Reload Timer

| Count Clock | Activation Trigger | Operation upon Underflow |
|---|---|---|
| Internal clock mode | Software trigger, external trigger | One-shot mode, reload mode |
| Event count mode | Software trigger | One-shot mode, reload mode |

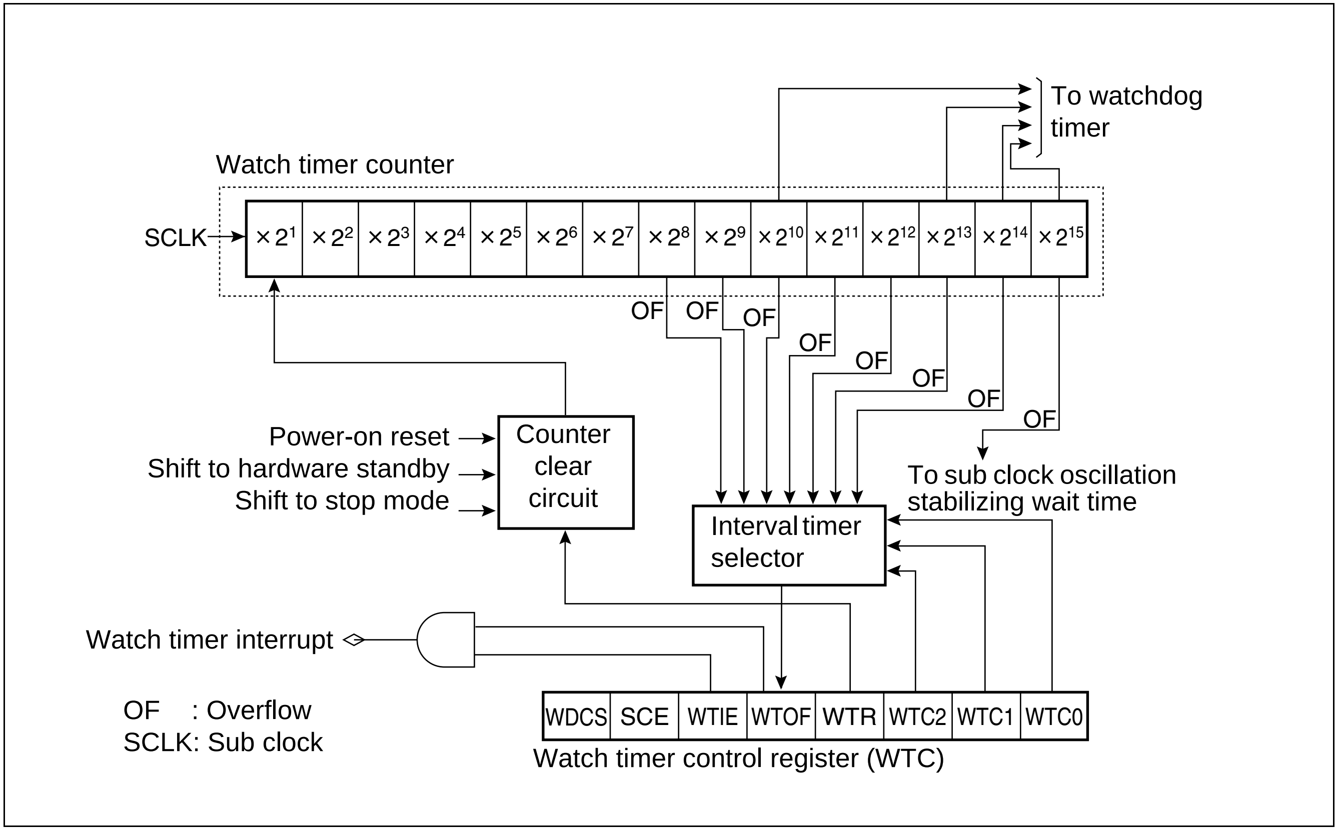
### Internal Clock Mode

- The 16-bit reload timer is set to internal clock mode, by setting count clock selection bit (TMCSR: CSL1, CSL0) to “$00_B$”, “$01_B$”, “$10_B$”.
- In the internal clock mode, the counter decrements in synchronization with the internal clock.
- Three types of count clock cycles are selectable by count clock selection bit (TMCSR: CSL1, CSL0) in timer control status register.
- Edge detection of software trigger or external trigger is specified as an activation trigger.

### 16-bit Reload Timer Block Diagram



### Watch Timer Block Diagram



Actual interrupt request number of watch timer is as follows:

Interrupt request number: #28 ($1C_H$)

### Watch Timer Counter

A 15-bit up counter that uses sub clock (SCLK) as a count clock.

### Counter Clear Circuit

A circuit that clears the watch timer counter.

## 12.11 UART Outline

UART is a general-purpose serial data communication interface for synchronous and asynchronous communication using external devices.

- ■ Provided with bi-directional communication function for both clock-synchronous and clock-asynchronous modes.
- ■ Provided with master/slave communication function (multi-processor mode). (Only master side is available.)
- ■ Interrupt request is generated upon completion of reception, completion of transmission and detection of reception error.
- ■ Ready for expanded intelligent service, EI$^2$OS.

**Table 12-3. UART Functions**

| | Description |
|---|---|
| Data buffer | Full-duplex double buffer |
| Transmission mode | Clock synchronous (No start/stop bit, no parity bit)<br>Clock asynchronous (start-stop synchronous) |
| Baud rate | Built-in special-purpose baud-rate generator. Setting is selectable among 8 values.<br>Input of external values is allowed.<br>Use of clock from external timer (16-bit reload timer 0) is allowed. |
| Data length | 7 bits (only asynchronous normal mode)<br>8 bits |
| Signaling system | Non Return to Zero (NRZ) system |
| Reception error detection | Framing error<br>Overrun error<br>Parity error (not detectable in operation mode 1 (multi-processor mode)) |
| Interrupt request | Receive interrupt (reception completed, reception error detected)<br>Transmission interrupt (transmission completed)<br>Ready for expanded intelligent I/O service (EI$^2$OS) in both transmission and reception |
| Master/slave communication function (asynchronous, multi-processor mode) | Communication between 1 (master) and n (slaves) are available (usable as master only). |

Note: Start/stop bit is not added upon clock-synchronous transmission. Data only is transmitted.

**Table 12-4. UART Operation Modes**

| Operation Mode | | Data Length | | Synchronization | Stop Bit Length |
|---|---|---|---|---|---|
| | | With Parity | Without Parity | | |
| 0 | Asynchronous mode (normal mode) | 7-bit or 8-bit | | Asynchronous | 1- bit or 2-bit *[2] |
| 1 | Multi processor mode | 8+1*[1] | – | Asynchronous | |
| 2 | Synchronous mode | 8 | – | Synchronous | No |

–: Disallowed

1: “+1” is an address/data selection bit used for communication control (bit 11 of SCR1 register: A/D).

2: Only 1 bit is detected as a stop bit on data reception.

## 12.12 CAN Controller

The Controller Area Network (CAN) is a serial communication protocol compliant with CANVer2.0A and Ver2.0B. The protocol allows data transmission and reception in both standard frame format and expanded frame format.

### Features of CAN Controller

- CAN controller format is compliant with CANVer2.0A and Ver2.0B.
- The protocol allows data transmission and reception in standard frame format and expanded frame format.
- Automatic transmission of data frame by remote frame reception is allowed.
- Baud rate ranges from 10 kbps to 1 Mbps (with 16-MHz machine clock).

**Table 12-5. Data Transmission Baud Rate**

| Machine Clock | Baud Rate (Max) |
|---|---|
| 16 MHz | 1 Mbps |
| 12 MHz | 1 Mbps |
| 8 MHz | 1 Mbps |
| 4 MHz | 500 kbps |
| 2 MHz | 250 kbps |

- Provided with 8 transmission/reception message buffers.
- Transmission/reception is allowed at ID 11 bit in standard format, and at ID 29 bit in expanded frame format.
- Specifying 0 byte to 8 bytes is allowed in message data.
- Multi-level message buffer configuration is allowed.
- CAN controller has two built-in acceptance masks. Mask settings are independently allowed for the two acceptance masks on reception IDs.
- The two acceptance masks allow reception in standard frame format and expanded frame format.
- For types of masking, all-bit comparison, all-bit masking, and partial masking with acceptance mask register 0/1, are specifiable.

## 12.15 512 Kbit Flash Memory Outline

The following three methods are provided for data writing and deleting on Flash memory:

1. Parallel writer
2. Serial special-purpose writer
3. Writing/deleting by program execution

This section describes “3. Writing/deleting by program execution.”

### 512 Kbit Flash Memory Outline

The 512 Kbit Flash memory is allocated on $FF_H$ bank of CPU memory map. Using the function of Flash memory interface circuit, the memory allows read access and program access from CPU.

Writing/deleting on Flash memory is performed by instruction from CPU via Flash memory interface. Because rewriting is allowed on mounted memory, modifying program and data is performed efficiently.

### Features of 512 Kbit Flash Memory

- ■ 128 K words x 8 bits/64 K words x 16 bits (16 K + 8 K + 8 K + 32 K) sector configuration
- ■ Automatic program algorithm (Embedded Algorithm: Similar to MBM29LV200.)
- ■ Built-in deletion pause/deletion resume function
- ■ Detection of completed writing/deleting by data polling and toggle bits.
- ■ Detection of completed writing/deleting by CPU interrupt.
- ■ Deletion is allowed on a sector-by-sector basis (sectors are combined freely).
- ■ Number of writing/deleting operations (minimum): 10,000 times
- ■ Sector protection
- ■ Expanded sector protection
- ■ Temporaly sector unprotection

Note: A function of reading manufacture code and device code is not provided. These codes are not accessible by command either.

### Flash Memory Writing/Deleting

- ■ Writing and reading data is not allowed simultaneously on the Flash memory.
- ■ Data writing and deleting on the Flash memory is performed by the processes as follows: Make a copy of program on Flash memory onto RAM. Then, execute the program copied on the RAM.

### List of Registers and Reset Values in Flash Memory

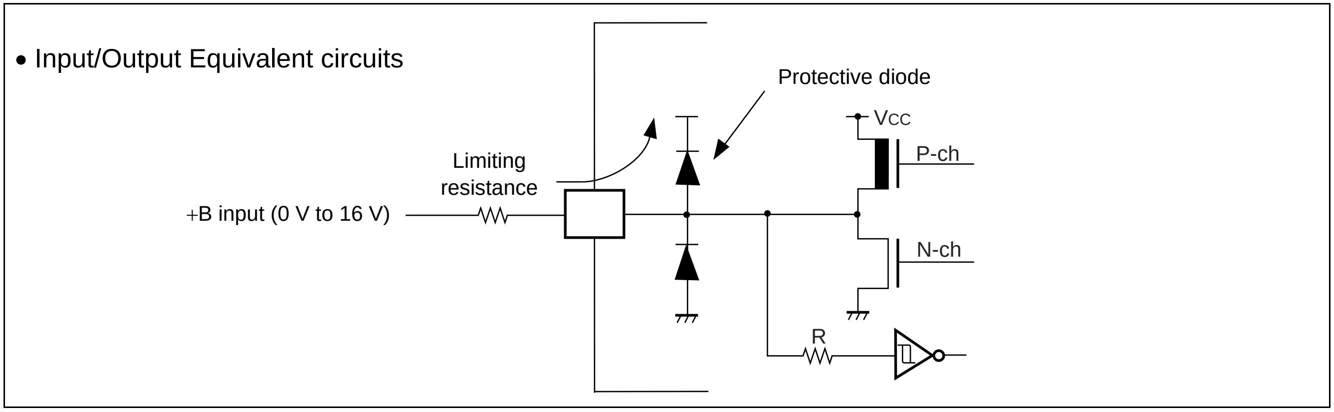
| | bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| Flash memory control status register (FMCS) | | 0 | 0 | 0 | X | 0 | 0 | 0 | 0 |

× : Undefined

### Sector Configuration

For access from CPU, SA0 to SA3 are allocated in FF bank register.

- Use within recommended operating conditions.
- Use at DC voltage (current).
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the $V_{CC}$ pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.
- Sample recommended circuits:


• Input/Output Equivalent circuits

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

### 13.2 Recommended Operating Conditions

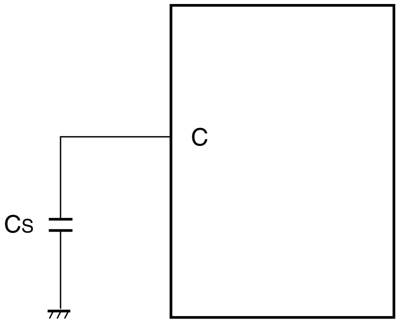
($V_{SS} = AV_{SS} = 0.0V$)

| Parameter | Symbol | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Power supply voltage | $V_{CC}$ | 3.5 | 5.0 | 5.5 | V | Under normal operation |
| | | 3.0 | – | 5.5 | V | Retain status of stop operation |
| | $AV_{CC}$ | 4.0 | – | 5.5 | V | *2 |
| Smoothing capacitor | $C_S$ | 0.1 | – | 1.0 | µF | *1 |
| Operating temperature | $T_A$ | –40 | – | +105 | °C | |

*1: Use a ceramic capacitor, or a capacitor of similar frequency characteristics. On the Vcc pin, use a bypass capacitor that has a larger capacity than that of Cs.
Refer to the following figure for connection of smoothing capacitor Cs.

*2: AVcc is a voltage at which accuracy is guaranteed. AVcc should not exceed Vcc.

- C pin connection diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

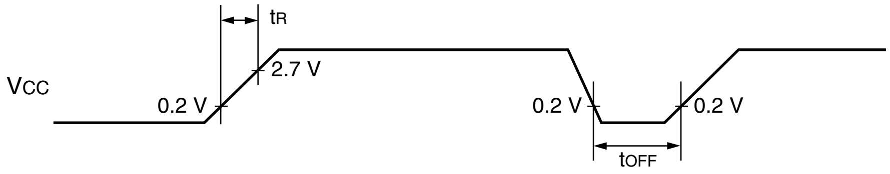
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

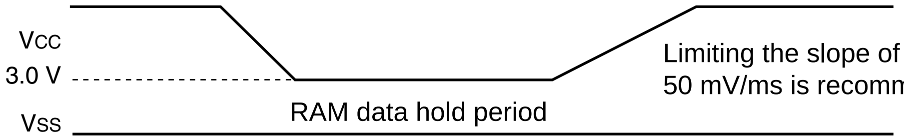
### *13.4.3 Power-on Reset*

($V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = −40 °C to +105 °C)

| **Parameter** | **Symbol** | **Pin Name** | **Conditions** | **Value** | | **Unit** | **Remarks** |
|---|---|---|---|---|---|---|---|
| | | | | **Min** | **Max** | | |
| Power supply rise time | $t_R$ | $V_{CC}$ | – | 0.05 | 30 | ms | |
| Power supply shutdown time | $t_{OFF}$ | $V_{CC}$ | | 1 | – | ms | Waiting time until power-on |



Sudden change of power supply voltage may activate the power-on reset function. When changing power supply voltages during operation, raise the power smoothly by suppressing variation of voltages as shown below. When raising the power, do not use PLL clock. However, if voltage drop is 1V/s or less, use of PLL clock is allowed during operation.

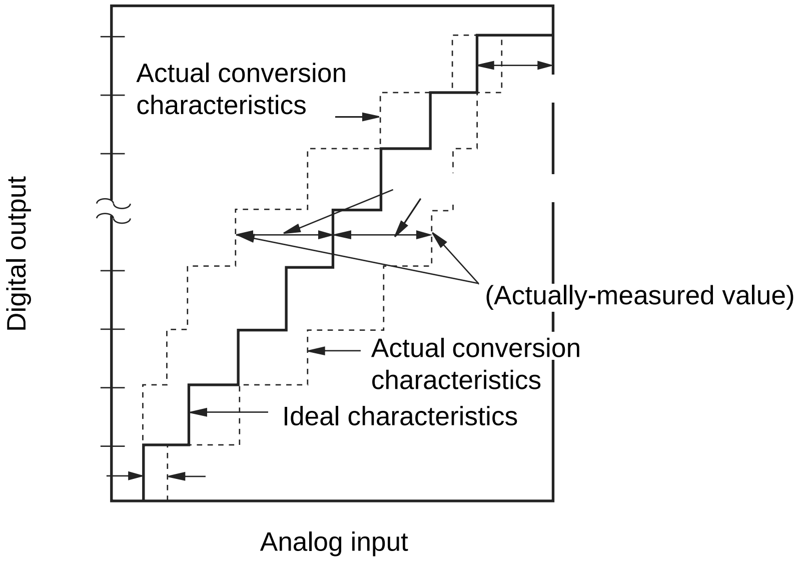


Limiting the slope of rising within 50 mV/ms is recommended.

### 13.6 Definition of A/D Converter Terms

| | |
|---|---|
| Resolution: | Analog variation that is recognized by an A/D converter. |
| Linear error: | Deviation between a line across zero-transition line (“00 0000 00 0 0” ←→“00 0000 0001”) and full-scale transition line (“11 1111 11 1 0” ←→ “11 1111 1111”) and actual conversion characteristics. |
| Differential linear error: | Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value. |
| Total error: | Difference between an actual value and an ideal value. A total error includes zero transition error, full-scale transition error, and linear error. |

Total error



$$\text{Total error of digital output “N”} = \frac{V_{NT} - \{1\text{ LSB} \times (N - 1) + 0.5\text{ LSB}\}}{1\text{ LSB}} \quad [\text{LSB}]$$

$$1\text{ LSB} = (\text{Ideal value})\ \frac{AVR - AV_{SS}}{1024}\ [\text{V}]$$

$V_{OT}$ (Ideal value) = $AV_{SS}$ + 0.5 LSB [V]

$V_{FST}$ (Ideal value) = AVR − 1.5 LSB [V]

$V_{NT}$: A voltage at which digital output transits from $(N\text{-}1)_H$ to $N_H$.

*(Continued)*

## 13.7 Notes on A/D Converter Section

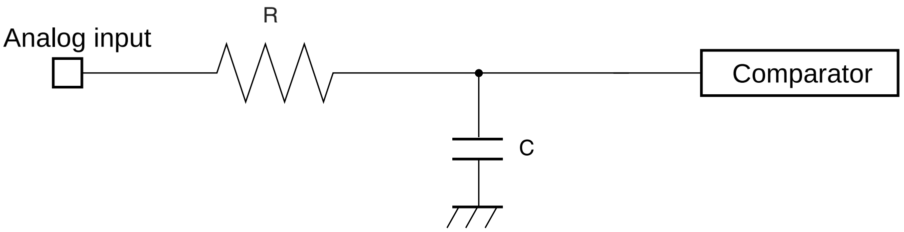
Use the device with external circuits of the following output impedance for analog inputs:

Recommended output impedance of external circuits are: Approx. 3.9 kΩ or lower (4.5 V ≤ AVcc ≤ 5.5 V) (sampling period=2.00 µs at 16 MHz machine clock), Approx. 11 kΩ or lower (4.0 V ≤ AVcc < 4.5 V) (sampling period=8.0 µs at 16 MHz machine clock).

If an external capacitor is used, in consideration of the effect by tap capacitance caused by external capacitors and on-chip capacitors, capacitance of the external one is recommended to be several thousand times as high as internal capacitor.

If output impedance of an external circuit is too high, a sampling period for an analog voltage may be insufficient.

- Analog input circuit model



MB90F387/S, MB90387/S
4.5 V ≤ AVcc ≤ 5.5 V    R ≅ 2.35 kΩ, C ≅ 36.4 pF
4.0 V ≤ AVcc < 4.5 V    R ≅ 16.4 kΩ, C ≅ 36.4 pF

Note: Use the values in the figure only as a guideline.

### About errors

As [AVR-AVss] become smaller, values of relative errors grow larger.

## 13.8 Flash Memory Program/Erase Characteristics

| Parameter | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Sector erase time | $T_A$ = + 25 °C<br>$V_{CC}$ = 5.0 V | – | 1 | 15 | s | Excludes 00H programming prior to erasure |
| Chip erase time | | – | 4 | – | s | Excludes 00H programming prior to erasure |
| Word (16-bit width) programming time | | – | 16 | 3,600 | µs | Except for the over head time of the system |
| Program/Erase cycle | – | 10,000 | – | – | cycle | |
| Flash Data Retention Time | Average<br>$T_A$ = + 85 °C | 20 | – | – | Year | * |

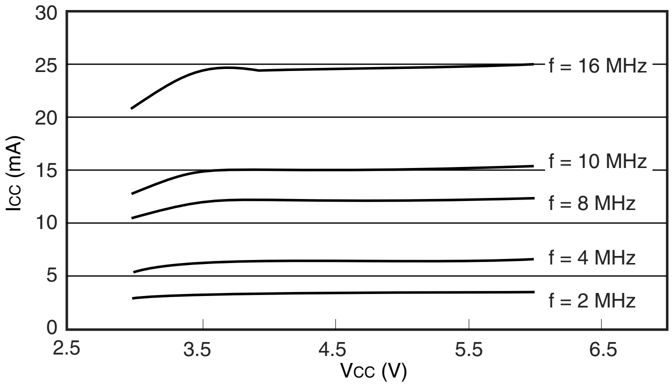
*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C).

## 14. Example Characteristics

**MB90F387**

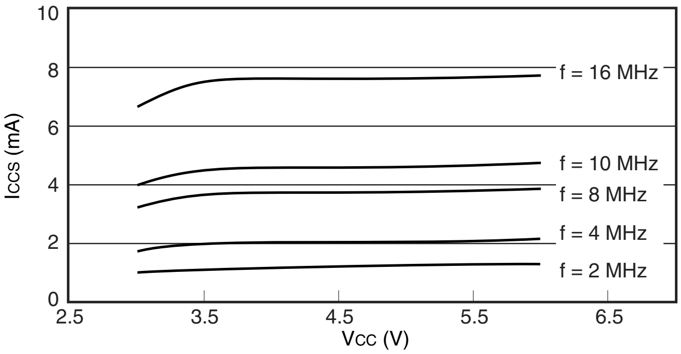
**$I_{CC} - V_{CC}$**

$T_A$ = +25 °C, In external clock operation
f = Internal operating frequency



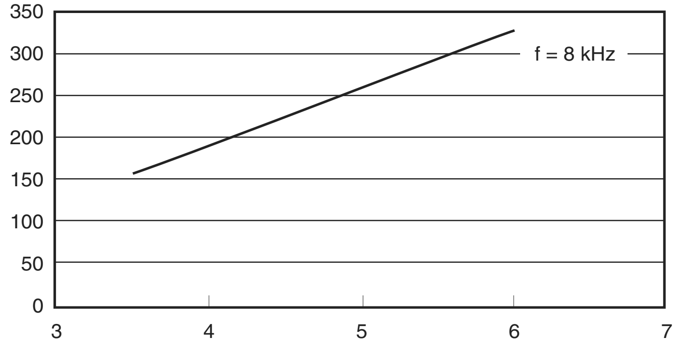
**$I_{CCS} - V_{CC}$**

$T_A$ = +25 °C, In external clock operation
f = Internal operating frequency



**$I_{CCL} - V_{CC}$**

$T_A$ = +25 °C, In external clock operation
f = Internal operating frequency



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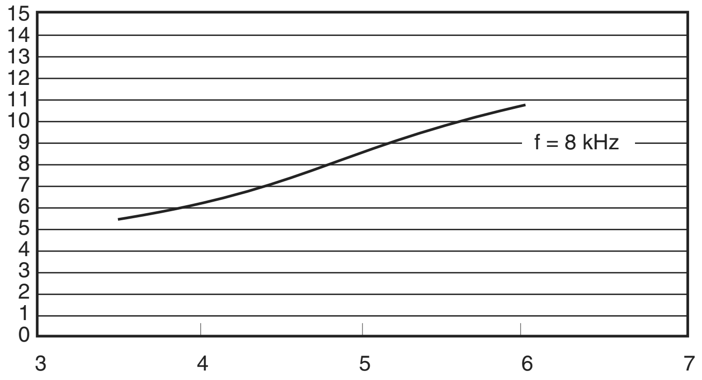
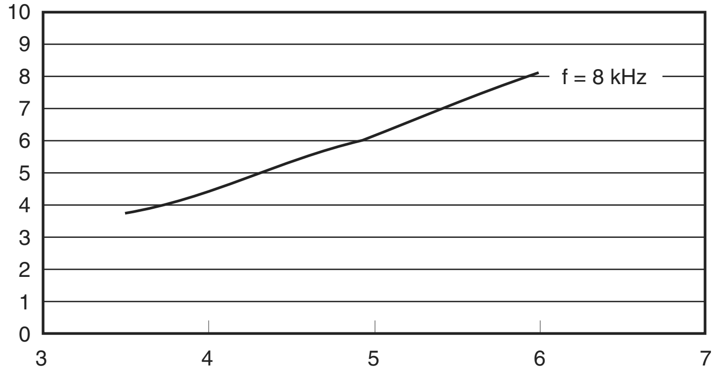
**$I_{CCLS}$ – $V_{CC}$**

$T_A$ = +25 °C, In external clock operation
f = Internal operating frequency



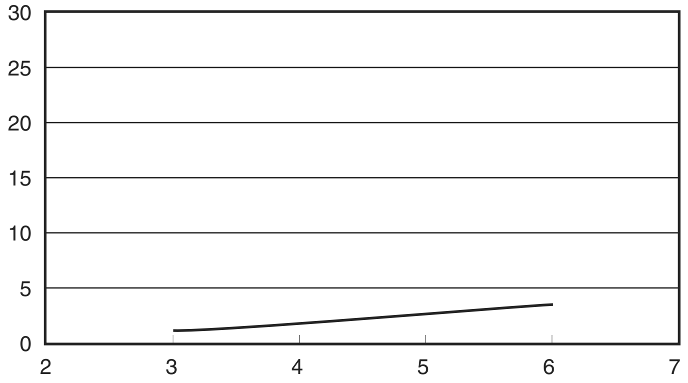
**$I_{CCT}$ – $V_{CC}$**

$T_A$ = +25 °C, In external clock operation
f = Internal operating frequency



**$I_{CCH}$ – $V_{CC}$**

Stopping, $T_A$ = +25 °C

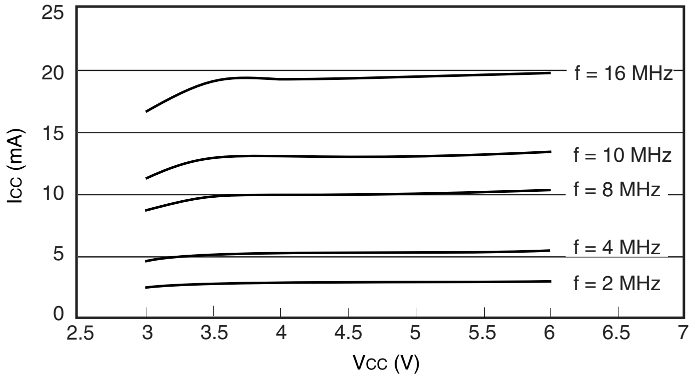


*(Continued)*

**MB90387**

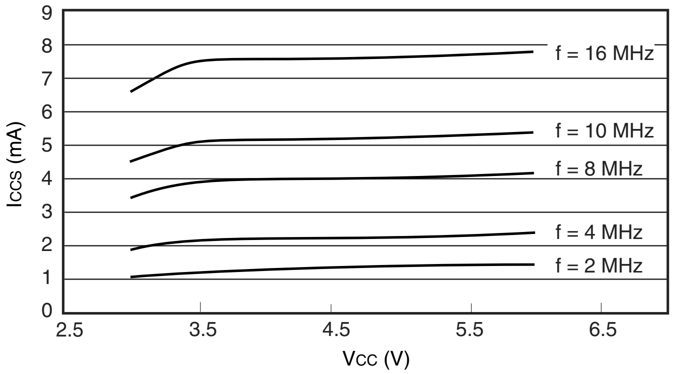
**$I_{CC}$ – $V_{CC}$**

$T_A$ = +25 °C, In external clock operation
f = Internal operating frequency



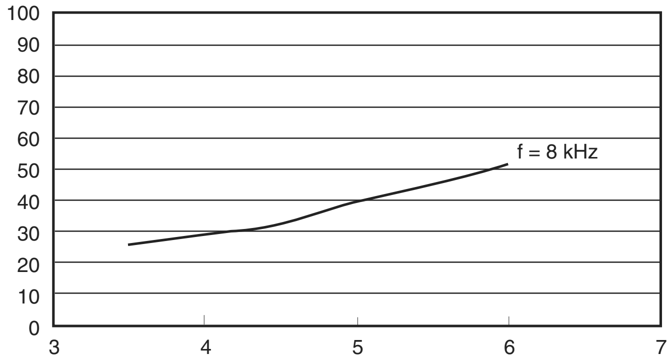
**$I_{CCS}$ – $V_{CC}$**

$T_A$ = +25 °C, In external clock operation
f = Internal operating frequency



**$I_{CCL}$ – $V_{CC}$**

$T_A$ = +25 °C, In external clock operation
f = Internal operating frequency



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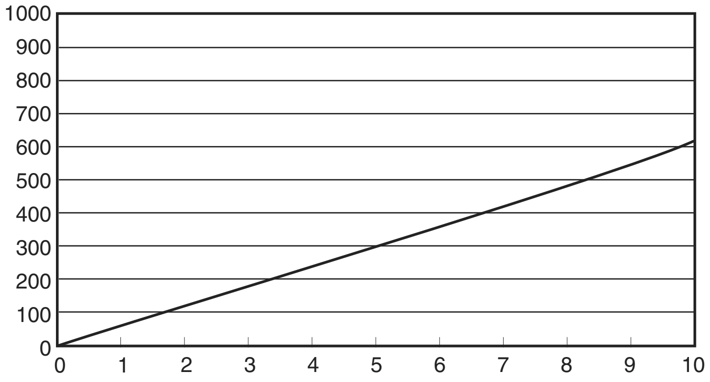
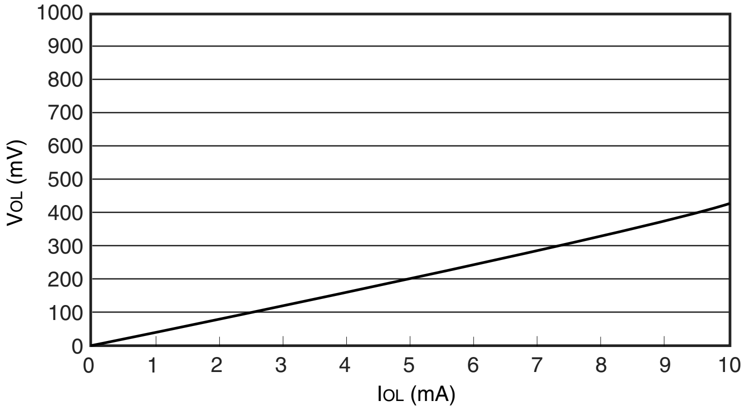
**$(V_{CC} - V_{OH}) – I_{OH}$**

$T_A = +25$ °C, $V_{CC} = 4.5$ V



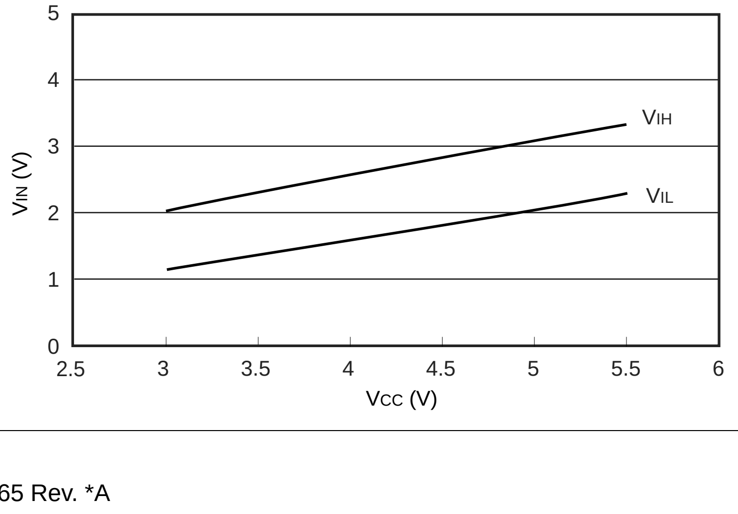
**$V_{OL} – I_{OL}$**

$T_A = +25$ °C, $V_{CC} = 4.5$ V



**H level input voltage/ L level input voltage**
**$V_{IN} – V_{CC}$**

$T_A = +25$ °C



## Document History

| Document Title: MB90387/387S/F387/F387S, MB90V495G, 16-bit Microcontrollers F²MC-16LX MB90385 Series<br>Document Number:002-07765 | | | | |
|---|---|---|---|---|
| **Revision** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** | — | AKIH | 12/19/2008 | Migrated to Cypress and assigned document number 002-07765.<br>No change to document contents or format. |
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