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What is "**Embedded - Microcontrollers**"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "**Embedded - Microcontrollers**"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, SCI, UART/USART
Peripherals	POR, WDT
Number of I/O	34
Program Memory Size	64KB (64K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90387pmt-gs-185e1

DTP/External Interrupt: 4 channels, CAN wakeup: 1channel

■ Module for activation of expanded intelligent I/O service (EI²OS), and generation of external interrupt.

Delay Interrupt Generator Module

■ Generates interrupt request for task switching.

8/10-bit A/D Converter: 8 channels

■ Resolution is selectable between 8-bit and 10-bit.

■ Activation by external trigger input is allowed.

■ Conversion time: 6.125 μs (at 16 MHz machine clock, including sampling time)

Program Patch Function

■ Address matching detection for 2 address pointers.

Contents

Part Number / Parameter	MB90F387 MB90F387S	MB90387 MB90387S	MB90V495G
8/10-bit A/D converter	Number of channels: 8 Resolution: Selectable 10-bit or 8-bit. Conversion time: 6.125 μs (at 16 MHz machine clock, including sampling time) Sequential conversion of two or more successive channels is allowed. (Setting a maximum of 8 channels is allowed.) Single conversion mode: Selected channel is converted only once. Sequential conversion mode: Selected channel is converted repetitively. Halt conversion mode: Conversion of selected channel is stopped and activated alternately.		
UART(SCI)	Number of channels: 1 Clock-synchronous transfer: 62.5 kbps to 2 Mbps Clock-asynchronous transfer: 9,615 bps to 500 kbps Communication is allowed by bi-directional serial communication function and master/slave type connection.		
CAN	Compliant with Ver 2.0A and Ver 2.0B CAN specifications. 8 built-in message buffers. Transmission rate of 10 kbps to 1 Mbps (by 16 MHz machine clock) CAN wake-up		

*1: Settings of DIP switch S2 for using emulation pod MB2145-507. For details, see MB2145-507 Hardware Manual
 (2.7 Power Pin solely for Emulator).

*2: MB90387S, MB90F387S

2. Packages And Product Models

Package	MB90F387, MB90F387S	MB90387, MB90387S
LQA048	◯	◯

◯ : Yes ×: No
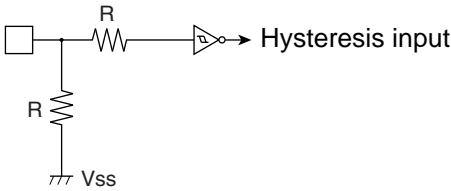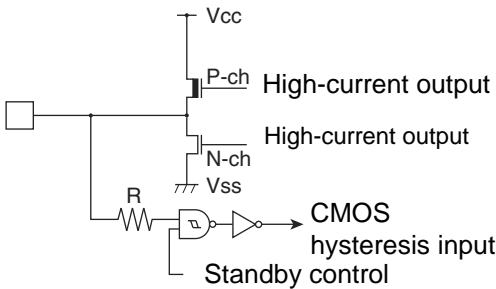
Note: Refer to Package Dimension for details of the package.

3. Product Comparison

Memory Space

When testing with test product for evaluation, check the differences between the product and a product to be used actually. Pay attention to the following points:

■ The MB90V495G has no built-in ROM. However, a special-purpose development tool allows the operations as those of one with built-in ROM. ROM capacity depends on settings on a development tool.

■ On MB90V495G, an image from FF4000$_H$ to FFFFFF$_H$ is viewed on 00 bank and an image of FE0000$_H$ to FF3FFF$_H$ is viewed only on FE bank and FF bank. (Modified on settings of a development tool.)

■ On MB90F387/F387S/387/387S, an image from FF4000$_H$ to FFFFFF$_H$ is viewed on 00 bank and an image of FE0000$_H$ to FF3FFF$_H$ is viewed only on FF bank.

Type	Circuit	Remarks
F		■ Hysteresis input with pull-down resistor ■ Pull-down resistor, approx. 50 kΩ ■ Flash product is not provided with pull-down resistor.
G		■ CMOS hysteresis input ■ CMOS level output (high-current output) ■ Standby control provided

7. Handling Devices

Do Not Exceed Maximum Rating (preventing "latch up")

■ On a CMOS IC, latch-up may occur when applying a voltage higher than Vcc or a voltage lower than Vss to input or output pin, which has no middle or high withstand voltage. Latch-up may also occur when a voltage exceeding maximum rating is applied across Vcc pin and Vss pin.

■ Latch-up causes drastic increase of power current, which may lead to destruction of elements by heat. Extreme caution must be taken not to exceed maximum rating.

■ When turning on and off analog power source, take extra care not to apply an analog power voltages (AVcc and AVR) and analog input voltage that are higher than digital power voltage (Vcc).

Handling Unused Pins

■ Leaving unused input pins open may cause permanent destruction by malfunction or latch-up. Apply pull-up or pull-down process to the unused pins using resistors of 2 kΩ or higher. Leave unused input/output pins open under output status, or process as input pins if they are under input status.

Using External Clock

■ When using an external clock, drive only X0 pin and leave X1 pin open. An example of using an external clock is shown below.

- Using external clock

Open — X1
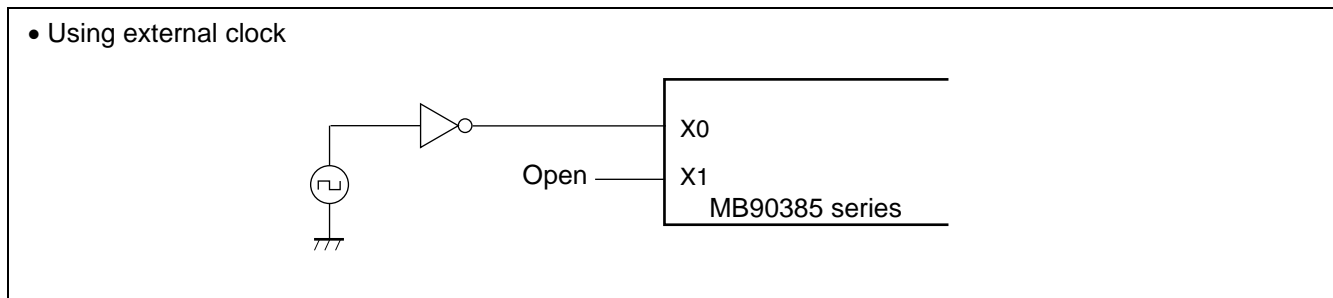
MB90385 series

8. Block Diagram
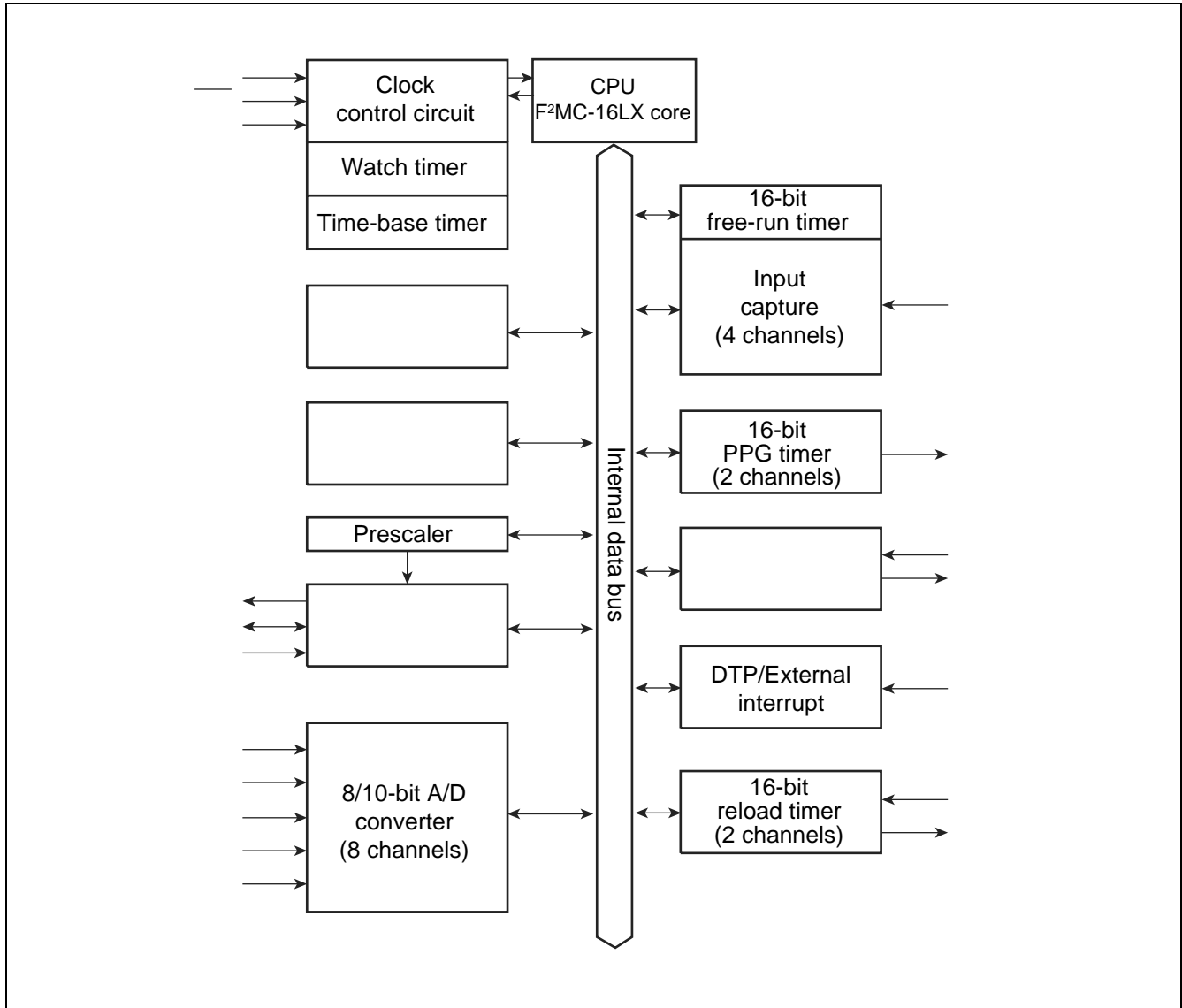
9. Memory Map

MB90385 series allows specifying a memory access mode "single chip mode."

9.1 Memory Allocation of MB90385

MB90385 series model has 24-bit wide internal address bus and up to 24-bit bus of external address bus.
A maximum of 16-Mbyte memory space of external access memory is accessible.

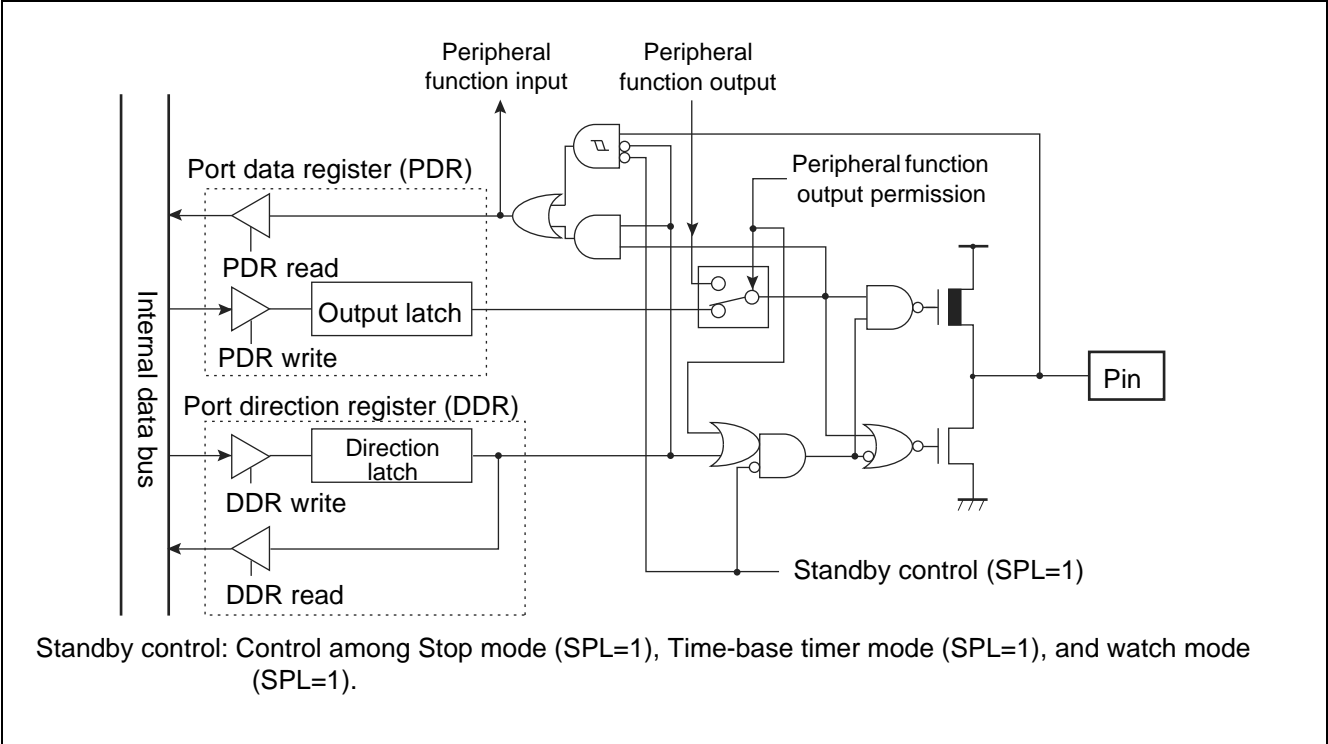| Address	Register Abbreviation	Register	Read/Write	Resource	Initial Value
003910H	PRLL0	PPG0 reload register L	R/W	8/16-bit PPG timer	XXXXXXXXB
003911H	PRLH0	PPG0 reload register H	R/W		XXXXXXXXB
003912H	PRLL1	PPG1 reload register L	R/W		XXXXXXXXB
003913H	PRLH1	PPG1 reload register H	R/W		XXXXXXXXB
003914H	PRLL2	PPG2 reload register L	R/W		XXXXXXXXB
003915H	PRLH2	PPG2 reload register H	R/W		XXXXXXXXB
003916H	PRLL3	PPG3 reload register L	R/W		XXXXXXXXB
003917H	PRLH3	PPG3 reload register H	R/W		XXXXXXXXB
003918H to 00392FH		(Reserved area) *			
003930H to 003BFFH		(Reserved area) *			
003C00H to 003C0FH		RAM (General-purpose RAM)			
003C10H to 003C13H	IDR0	ID register 0	R/W	CAN controller	XXXXXXXXB to XXXXXXXXB
003C14H to 003C17H	IDR1	ID register 1	R/W		XXXXXXXXB to XXXXXXXXB
003C18H to 003C1BH	IDR2	ID register 2	R/W		XXXXXXXXB to XXXXXXXXB
003C1CH to 003C1FH	IDR3	ID register 3	R/W		XXXXXXXXB to XXXXXXXXB
003C20H to 003C23H	IDR4	ID register 4	R/W		XXXXXXXXB to XXXXXXXXB
003C24H to 003C27H	IDR5	ID register 5	R/W		XXXXXXXXB to XXXXXXXXB
003C28H to 003C2BH	IDR6	ID register 6	R/W		XXXXXXXXB to XXXXXXXXB
003C2CH to 003C2FH	IDR7	ID register 7	R/W		XXXXXXXXB to XXXXXXXXB
003C30H, 003C31H	DLCR0	DLC register 0	R/W		XXXXXXXXB, XXXXXXXXB
003C32H, 003C33H	DLCR1	DLC register 1	R/W		XXXXXXXXB, XXXXXXXXB
003C34H, 003C35H	DLCR2	DLC register 2	R/W		XXXXXXXXB, XXXXXXXXB
003C36H, 003C37H	DLCR3	DLC register 3	R/W		XXXXXXXXB, XXXXXXXXB

Port 3 Pins Block Diagram (general-purpose input/output port)

Standby control: Control among Stop mode (SPL=1), Time-base timer mode (SPL=1), and watch mode (SPL=1).

Port 3 Registers

■ Port 3 registers include port 3 data register (PDR3) and port 3 direction register (DDR3).

■ The bits configuring the register correspond to port 3 pins on a one-to-one basis.

Relation between Port 3 Registers and Pins

Port Name	Bits of Register and Corresponding Pins								
Port 3	PDR3, DDR3	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	Corresponding pins	P37	P36*	P35*	–	P33	P32	P31	P30

*: P35 and P36 do not exist on MB90387and MB90F387.

12.4 16-bit Input/Output Timer

The 16-bit input/output timer is a compound module composed of 16-bit free-run timer, (1 unit) and input capture (2 units, 4 input pins). The timer, using the 16-bit free-run timer as a basis, enables measurement of clock cycle of an input signal and its pulse width.

Configuration of 16-bit Input/Output Timer

The 16-bit input/output timer is composed of the following modules:

■ 16-bit free-run timer (1 unit)

■ Input capture (2 units, 2 input pins per unit)

Functions of 16-bit Input/Output Timer

Functions of 16-bit Free-run Timer

The 16-bit free-run timer is composed of 16-bit up counter, timer counter control status register, and prescaler. The 16-bit up counter increments in synchronization with dividing ratio of machine clock.

■ Count clock is set among four types of machine clock dividing rates.

■ Generation of interrupt is allowed by counter value overflow.

■ Activation of expanded intelligent I/O service (EI²OS) is allowed by interrupt generation.

■ Counter value of 16-bit free-run timer is cleared to "0000$_H$" by either resetting or software-clearing with timer count clear bit (TCCS: CLR).

■ Counter value of 16-bit free-run timer is output to input capture, which is available as base time for capture operation.

Functions of Input Capture

The input capture, upon detecting an edge of a signal input to the input pin from external device, stores a counter value of 16-bit free-run timer at the time of detection into the input capture data register. The function includes the input capture data registers corresponding to four input pins, input capture control status register, and edge detection circuit.

■ Rising edge, falling edge, and both edges are selectable for detection.

■ Generating interrupt on CPU is allowed by detecting an edge of input signal.

■ Expanded intelligent I/O service (EI²OS) is activated by interrupt generation.

■ The four input capture input pins and input capture data registers allows monitoring of a maximum of four events.

16-bit Input/Output Timer Block Diagram
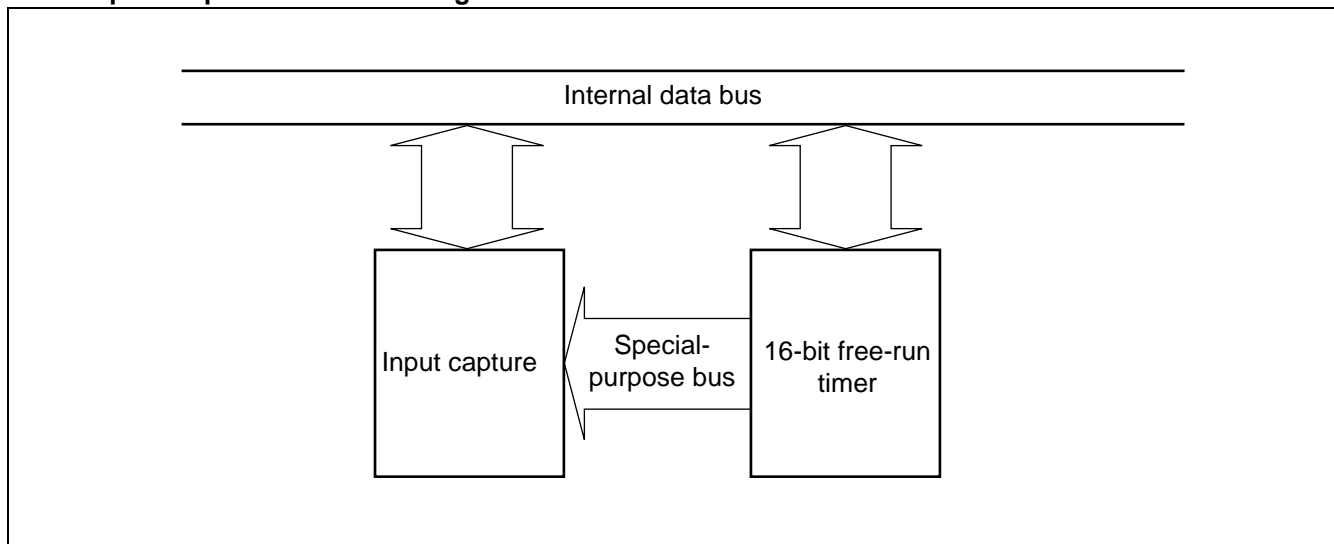
12.5 16-bit Reload Timer

The 16-bit reload timer has the following functions:

■ Count clock is selectable among 3 internal clocks and external event clock.

■ Activation trigger is selectable between software trigger and external trigger.

■ Generation of CPU interrupt is allowed upon occurrence of underflow on 16-bit timer register. Available as an interval timer using the interrupt function.

■ When underflow of 16-bit timer register (TMR) occurs, one of two reload modes is selectable between one-shot mode that halts counting operation of TMR, and reload mode that reloads 16-bit reload register value to TMR, continuing TMR counting operation.

■ The 16-bit reload timer is ready for expanded intelligent I/O service (EI²OS).

■ MB90385 series device has 2 channels of built-in 16-bit reload timer.

Operation Mode of 16-bit Reload Timer

Count Clock	Activation Trigger	Operation upon Underflow
Internal clock mode	Software trigger, external trigger	One-shot mode, reload mode
Event count mode	Software trigger	One-shot mode, reload mode

Internal Clock Mode

■ The 16-bit reload timer is set to internal clock mode, by setting count clock selection bit (TMCSR: CSL1, CSL0) to "00$_B$", "01$_B$", "10$_B$".

■ In the internal clock mode, the counter decrements in synchronization with the internal clock.

■ Three types of count clock cycles are selectable by count clock selection bit (TMCSR: CSL1, CSL0) in timer control status register.

■ Edge detection of software trigger or external trigger is specified as an activation trigger.

12.6 Watch Timer Outline

The watch timer is a 15-bit free-run counter that increments in synchronization with sub clock.

■ Interval time is selectable among 7 choices, and generation of interrupt request is allowed for each interval.

■ Provides operation clock to the subclock oscillation stabilizing wait timer and watchdog timer.

■ Always uses subclock as a count clock regardless of settings of clock selection register (CKSCR).

Interval Timer Function

■ In the watch timer, a bit corresponding to the interval time overflows (carry-over) when an interval time, which is specified by interval time selection bit, is reached. Then overflow flag bit is set (WTC: WTOF=1).

■ If an interrupt by overflow is permitted (WTC: WTIE=1), an interrupt request is generated upon setting an overflow flag bit.

■ Interval time of watch timer is selectable among the following seven choices:

Interval Time of Watch Timer

Sub Clock Cycle	Interval Time
1/SCLK (122 μs)	2^8/SCLK (31.25 ms)
	2^9/SCLK (62.5 ms)
	2^{10}/SCLK (125 ms)
	2^{11}/SCLK (250 ms)
	2^{12}/SCLK (500 ms)
	2^{13}/SCLK (1.0 s)
	2^{14}/SCLK (2.0 s)

SCLK: Sub clock frequency

Values in parentheses "( )" are calculation when operating with 8.192 kHz clock.

8/16-bit PPG Timer 1 Block Diagram
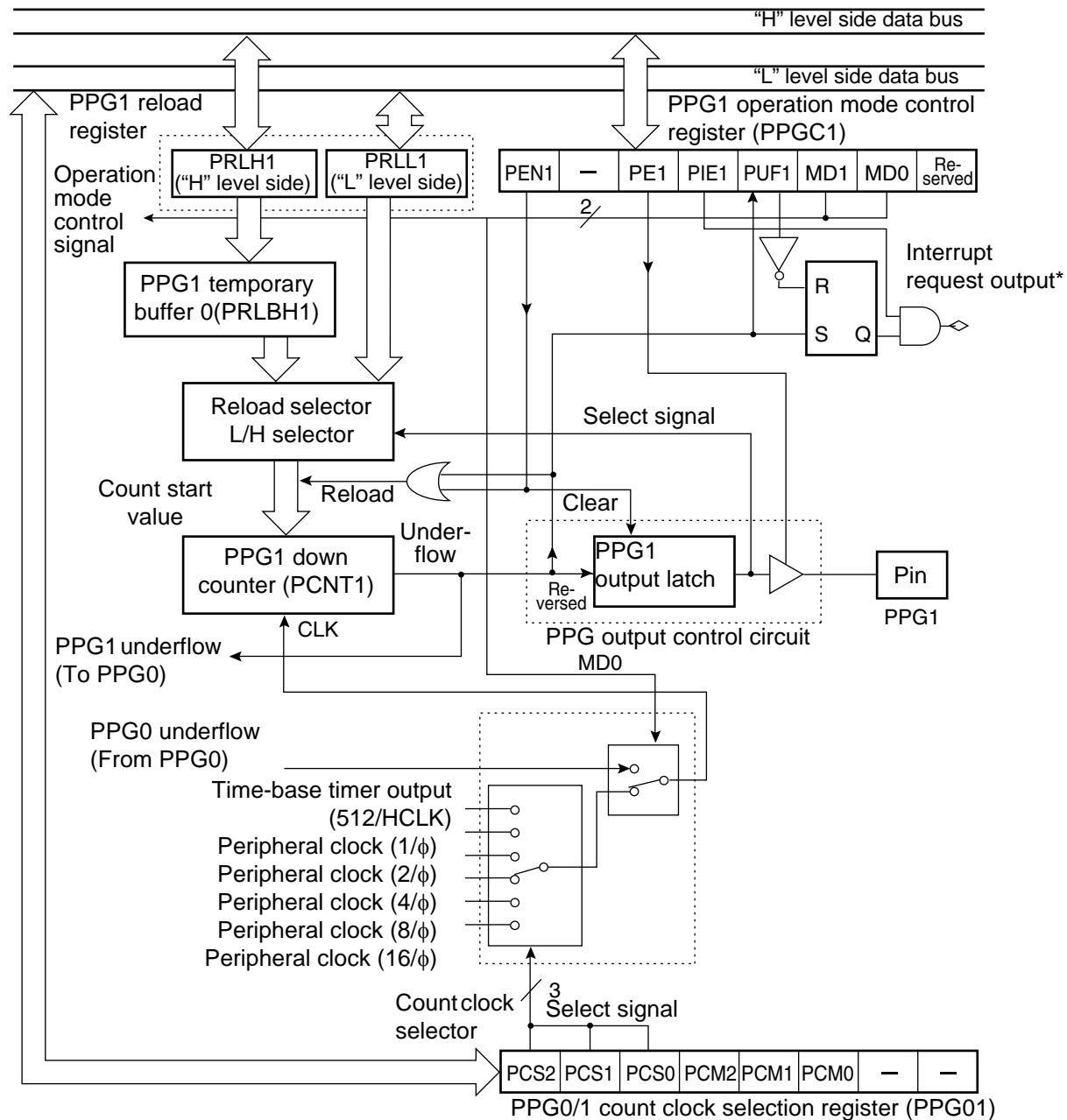
− : Undefined

Reserved: Reserved bit

HCLK : Oscillation clock frequency

φ : Machine clock frequency

* : Interrupt output of 8/16-bit PPG timer 1 is incorporated into one by the OR circuit against interrupt output of 8/16-bit PPG timer 0.

12.9 DTP/External Interrupt and CAN Wakeup Outline

DTP/external interrupt transfers an interrupt request generated by an external peripheral device or a data transmission request to CPU, generating external interrupt request and activating expanded intelligent I/O service. Input RX of CAN controller is used as external interrupt input.

DTP/External Interrupt and CAN Wakeup Function

An interrupt request input from external peripheral device to external input pins (INT7 to INT4) and RX pin, just as interrupt request of peripheral device, generates an interrupt request. The interrupt request generates an external interrupt and activates expanded intelligent I/O service (EI^2OS).

If the expanded intelligent I/O service (EI^2OS) has been disabled by interrupt control register (ICR: ISE=0), external interrupt function is enabled and branches to interrupt processing.

If the EI^2OS has been enabled, (ICR: ISE=1), DTP function is enabled and automatic data transmission is performed by EI^2OS. After performing specified number of data transmission processes, the process branches to interrupt processing.

Table 12-2. DTP/External Interrupt and CAN Wakeup Outline

	External Interrupt	DTP Function
Input pin	5 pins (RX, and INT4 to INT7)	
Interrupt cause	Specify for each pin with detection level setting register (ELVR).	
	Input of "H" level/"L" level/rising edge/falling edge.	Input of "H" level/ "L" level
Interrupt number	#15 ($0F_H$), #24 (18_H), #27 ($1B_H$)	
Interrupt control	Enabling or disabling output of interrupt request, using DTP/external interrupt permission register (ENIR).	
Interrupt flag	Retaining interrupt cause with DTP/external interrupt cause register (EIRR).	
Process selection	Disable EI^2OS (ICR: ISE=0)	Enable EI^2OS (ICR: ISE=1)
Process	Branch to external interrupt process	After automatic data transmission by EI^2OS for specified number of times, branch to interrupt process.

12.11 UART Outline

UART is a general-purpose serial data communication interface for synchronous and asynchronous communication using external devices.

■ Provided with bi-directional communication function for both clock-synchronous and clock-asynchronous modes.

■ Provided with master/slave communication function (multi-processor mode). (Only master side is available.)

■ Interrupt request is generated upon completion of reception, completion of transmission and detection of reception error.

■ Ready for expanded intelligent service, EI^{2}OS.

Table 12-3. UART Functions

	Description
Data buffer	Full-duplex double buffer
Transmission mode	Clock synchronous (No start/stop bit, no parity bit) Clock asynchronous (start-stop synchronous)
Baud rate	Built-in special-purpose baud-rate generator. Setting is selectable among 8 values. Input of external values is allowed. Use of clock from external timer (16-bit reload timer 0) is allowed.
Data length	7 bits (only asynchronous normal mode) 8 bits
Signaling system	Non Return to Zero (NRZ) system
Reception error detection	Framing error Overrun error Parity error (not detectable in operation mode 1 (multi-processor mode))
Interrupt request	Receive interrupt (reception completed, reception error detected) Transmission interrupt (transmission completed) Ready for expanded intelligent I/O service (EI^{2}OS) in both transmission and reception
Master/slave communication function (asynchronous, multi-processor mode)	Communication between 1 (master) and n (slaves) are available (usable as master only).

Note: Start/stop bit is not added upon clock-synchronous transmission. Data only is transmitted.

Table 12-4. UART Operation Modes

Operation Mode		Data Length		Synchronization	Stop Bit Length
		With Parity	Without Parity		
0	Asynchronous mode (normal mode)	7-bit or 8-bit		Asynchronous	1- bit or 2-bit *2
1	Multi processor mode	8+1*1	–	Asynchronous	
2	Synchronous mode	8	–	Synchronous	No

−: Disallowed

1: "+1" is an address/data selection bit used for communication control (bit 11 of SCR1 register: A/D).

2: Only 1 bit is detected as a stop bit on data reception.

12.12 CAN Controller

The Controller Area Network (CAN) is a serial communication protocol compliant with CANVer2.0A and Ver2.0B. The protocol allows data transmission and reception in both standard frame format and expanded frame format.
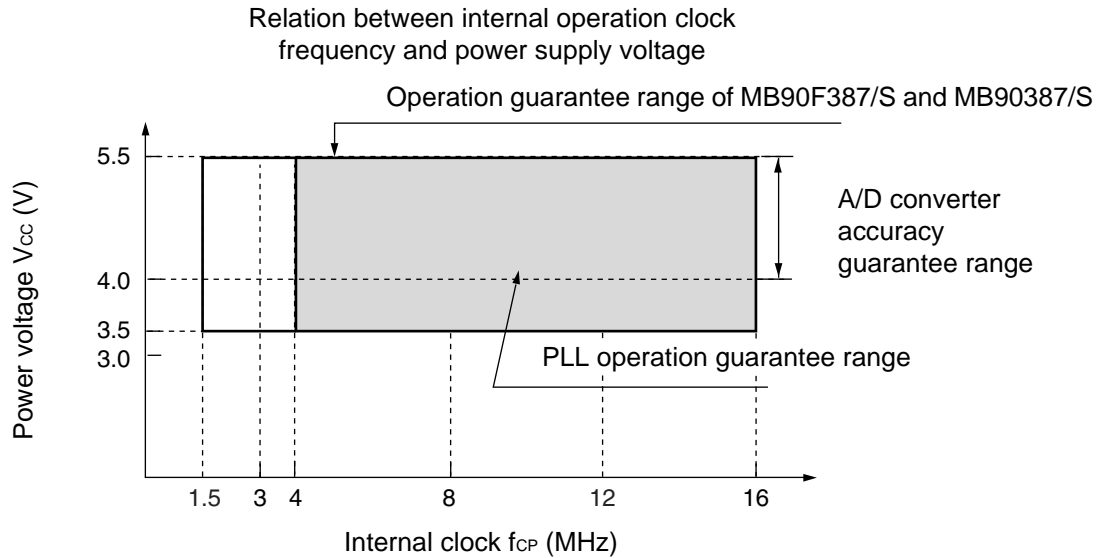
Features of CAN Controller

■ CAN controller format is compliant with CANVer2.0A and Ver2.0B.

■ The protocol allows data transmission and reception in standard frame format and expanded frame format.

■ Automatic transmission of data frame by remote frame reception is allowed.

■ Baud rate ranges from 10 kbps to 1 Mbps (with 16-MHz machine clock).
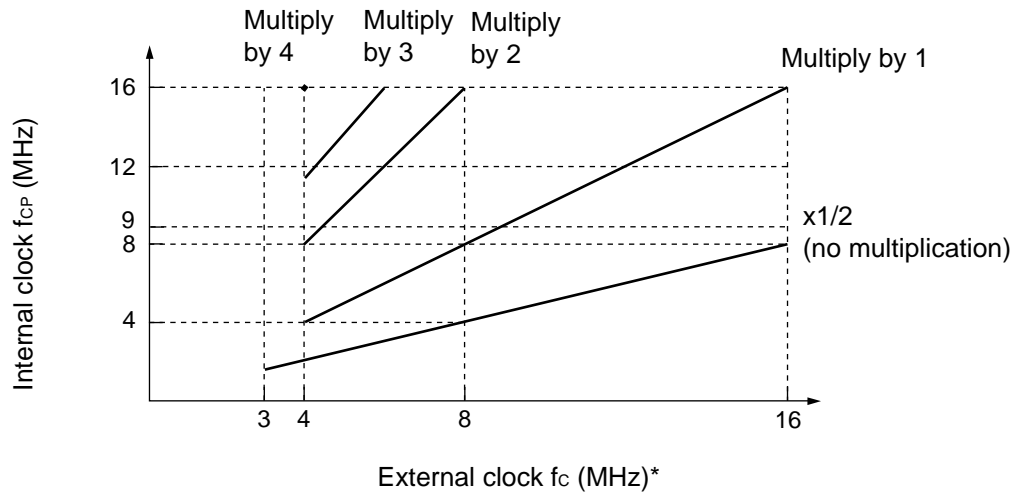
Table 12-5. Data Transmission Baud Rate

Machine Clock	Baud Rate (Max)
16 MHz	1 Mbps
12 MHz	1 Mbps
8 MHz	1 Mbps
4 MHz	500 kbps
2 MHz	250 kbps

■ Provided with 8 transmission/reception message buffers.

■ Transmission/reception is allowed at ID 11 bit in standard format, and at ID 29 bit in expanded frame format.

■ Specifying 0 byte to 8 bytes is allowed in message data.

■ Multi-level message buffer configuration is allowed.

■ CAN controller has two built-in acceptance masks. Mask settings are independently allowed for the two acceptance masks on reception IDs.

■ The two acceptance masks allow reception in standard frame format and expanded frame format.

■ For types of masking, all-bit comparison, all-bit masking, and partial masking with acceptance mask register 0/1, are specifiable.

• PLL operation guarantee range

Relation between internal operation clock
frequency and power supply voltage

Operation guarantee range of MB90F387/S and MB90387/S

A/D converter
accuracy
guarantee range

PLL operation guarantee range

Power voltage V_{CC} (V)

Internal clock f_{CP} (MHz)

Relation among external clock frequency and internal clock frequency

Multiply by 4 Multiply by 3 Multiply by 2

Multiply by 1

x1/2
(no multiplication)

Internal clock f_{CP} (MHz)

External clock f_C (MHz)*

*: fc is 8 MHz at maximum when crystal or ceramic resonator circuit is used.

13.7 Notes on A/D Converter Section

Use the device with external circuits of the following output impedance for analog inputs:

Recommended output impedance of external circuits are: Approx. 3.9 kΩ or lower (4.5 V ≤ AVcc ≤ 5.5 V) (sampling period=2.00 μs at 16 MHz machine clock), Approx. 11 kΩ or lower (4.0 V ≤ AVcc < 4.5 V) (sampling period=8.0 μs at 16 MHz machine clock).

If an external capacitor is used, in consideration of the effect by tap capacitance caused by external capacitors and on-chip capacitors, capacitance of the external one is recommended to be several thousand times as high as internal capacitor.

If output impedance of an external circuit is too high, a sampling period for an analog voltage may be insufficient.

- Analog input circuit model
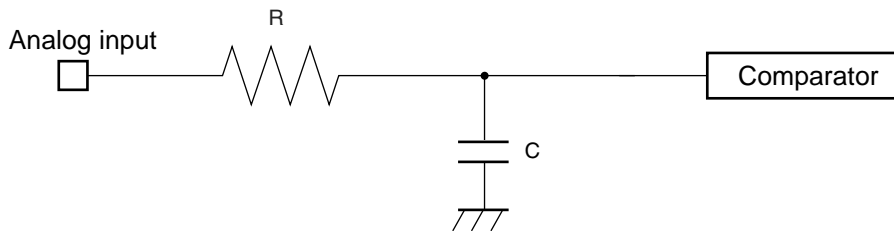
MB90F387/S, MB90387/S
4.5 V ≤ AVcc ≤ 5.5 V   R ≅ 2.35 kΩ, C ≅ 36.4 pF
4.0 V ≤ AVcc < 4.5 V   R ≅ 16.4 kΩ, C ≅ 36.4 pF

Note: Use the values in the figure only as a guideline.

About errors

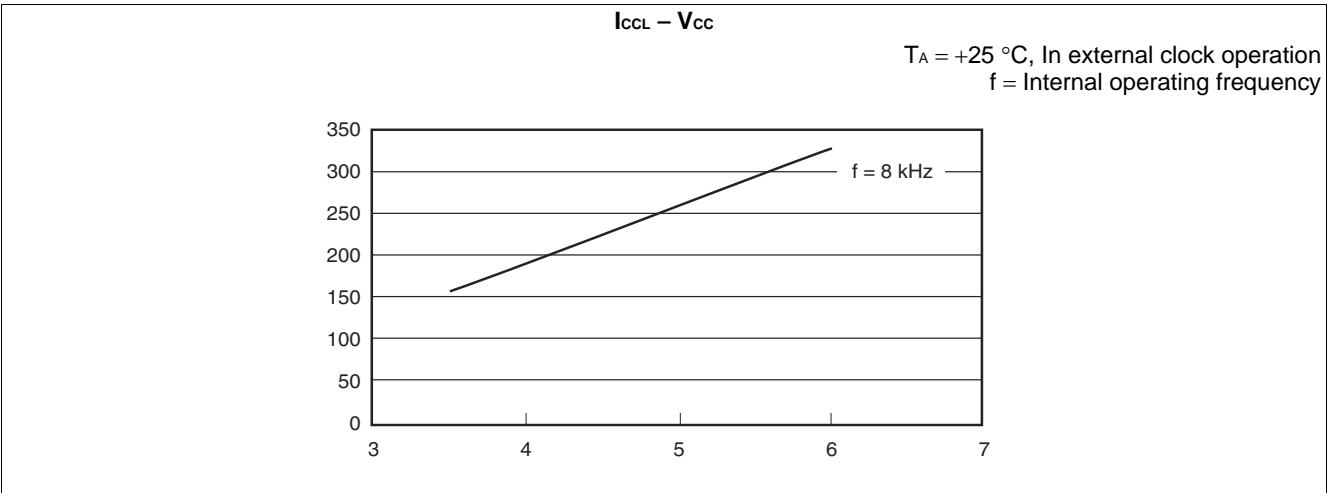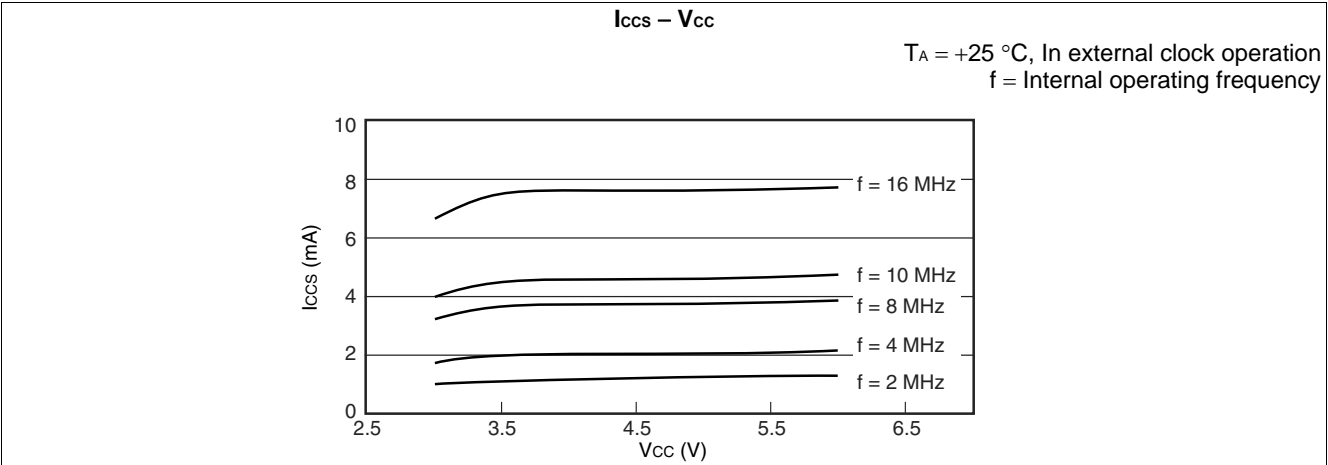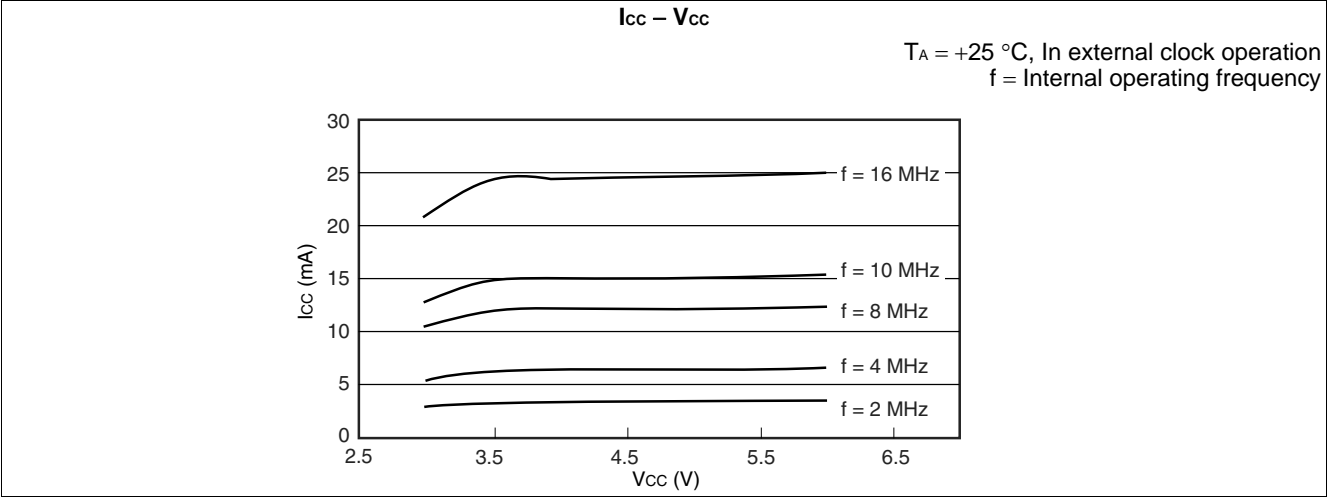As [AVR-AVss] become smaller, values of relative errors grow larger.

13.8 Flash Memory Program/Erase Characteristics

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	$T_A = +25\ °C$ $V_{CC} = 5.0\ V$	–	1	15	s	Excludes 00H programming prior to erasure
Chip erase time		–	4	–	s	Excludes 00H programming prior to erasure
Word (16-bit width) programming time		–	16	3,600	μs	Except for the over head time of the system
Program/Erase cycle	–	10,000	–	–	cycle	
Flash Data Retention Time	Average $T_A = +85\ °C$	20	–	–	Year	*

*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C).

14. Example Characteristics

MB90F387

I_{CC} – V_{CC}

T_A = +25 °C, In external clock operation
f = Internal operating frequency

I_{CCS} – V_{CC}

T_A = +25 °C, In external clock operation
f = Internal operating frequency

I_{CCL} – V_{CC}

T_A = +25 °C, In external clock operation
f = Internal operating frequency

(Continued)

MB90387

I$_{CC}$ – V$_{CC}$

T$_A$ = +25 °C, In external clock operation
f = Internal operating frequency

I$_{CCS}$ – V$_{CC}$

T$_A$ = +25 °C, In external clock operation
f = Internal operating frequency

I$_{CCL}$ – V$_{CC}$

T$_A$ = +25 °C, In external clock operation
f = Internal operating frequency

(Continued)

15. Ordering Information

Part Number	Package	Remarks
MB90F387PMT MB90387PMT MB90F387SPMT MB90387SPMT	48-pin plastic LQFP (LQA048)	

16. Package Dimension

TOP VIEW

BOTTOM VIEW

SIDE VIEW

DETAIL A

SECTION A-A'
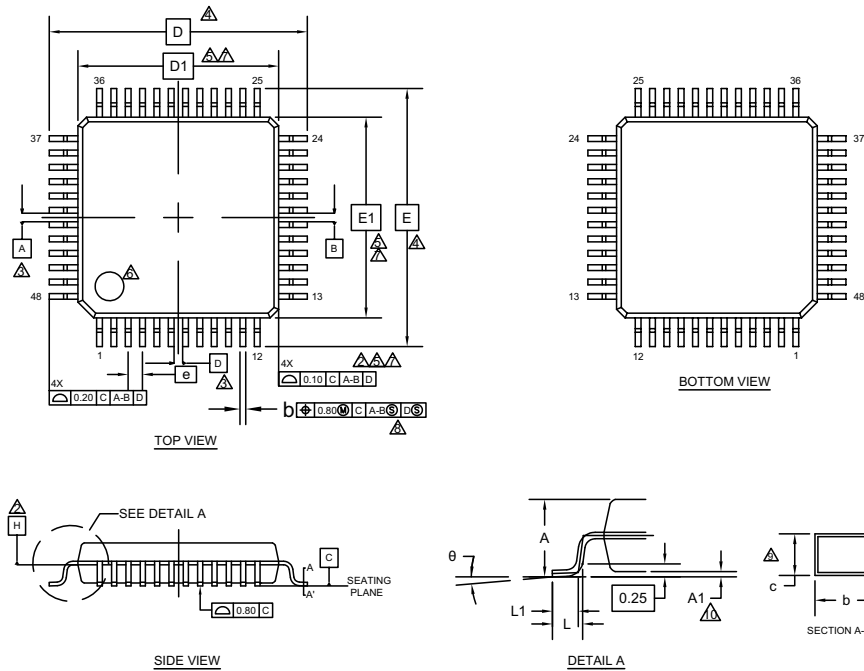
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.15	—	0.27
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.50 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.

2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.

3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.

4. TO BE DETERMINED AT SEATING PLANE C.

5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.

7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.

8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.

9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.

10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13731 **

PACKAGE OUTLINE, 48 LEAD LQFP
7.0X7.0X1.7 MM LQA048 REV**